UNH–IOL
NVMe Testing Service

Test Plan for NVMe Conformance
Version 910.0
Target Specification: NVMe 1.3
Technical Document

NOTICE: This is a living document. All contents are subject to change. Individual tests and/or test groups may be added/deleted/renumbered in forthcoming revisions. General feedback and comments are welcome through the NVMe Consortium at UNH–IOL.

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- OF = Out-of-Order Events (OF)
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   David Woolf: Updates to tests 2.1 and 2.4.

2013 December 16 (Version 1.1 DRAFT)
   David Woolf: Updates to tests 1.1, 1.2, 1.3, 1.5, 2.1, 2.2, 2.3, 2.4, 2.5, 4.3, 4.4, 4.5, 4.6, 4.7, and 4.8. Most of the changes involve clarifying or removing observable results that could not be easily observed.

2013 December 19 (Version 1.1)
   David Woolf: Added Appendix C with information about potential test tools. Removed references to conformance testing of NVMe Hosts, as this is not currently a requirement for including NVMe Hosts on the NVMe Integrators List.

2014 May 27 (Version 1.1)
   David Woolf: Edited procedures to test 1.2 and 4.5 to make them easier to perform.

2014 June 5 (Version 1.1)
   David Woolf: Corrected test numbering in Group 5 and Group 6. Clarified that tests 3.1, 3.2, and 4.6 are optional. Corrected reference in test 5.3.

2014 July 7 (Version 1.1)
   David Woolf: Added test 6.4.

2014 July 10 (Version 1.1)
   David Woolf: Added test 2.7, modified procedure to test 2.1.

2014 July 14 (Version 1.1b)
   David Woolf: Change specification references to 1.1b revision of specification.

2014 August 14 (Version 1.1b)
   David Woolf: Added Group 7 tests for Reservations.

2014 September 18 (Version 1.1b)
David Woolf: Added notes Group 7 tests for Reservations to indicate that these tests are only applicable to device which support reservations.

2014 September 29 (Version 1.1b)
Mike Bogochow: Updated references and fixed errata.

2014 October 16 (Version 1.1b)
David Woolf: Clarification on Mandatory and Optional tests in Group 2.

2015 April 9 (Version 1.2)
David Woolf: Prepared document for 1.2 revisions.

2015 April 13 (Version 1.2)
David Woolf: Added tests 8.1 and 8.2.

2015 June 24 (Version 1.2.1)
Mike Bogochow: Fixed errata and updated references, procedures, and observable results for all tests in groups 1–6.

2015 November 23 (Version 1.2.1)
Mike Bogochow: Added Group 9 Tests.

2015 March 2 (Version 1.2.2)
Mike Bogochow: Fixed errata, clarified language, and updated procedures and observable results of various existing tests.

2016 March 21 (Version 1.3.0)
Mike Bogochow: Rewrote Groups 7 and 8. Added Test 1.7 - Asynchronous Events. Added Test 1.4 - Case 2: Full Queue Condition. Fixed Purpose wording for most tests.

2016 May 19 (Version 6.0 r01)
David Woolf: Adopted new document numbering scheme, rather than using numbers that are close to the current specification release, test suites will follow a numbering scheme based on the Integrators List version, which is incremented with each plugfest.

2016 May 24 (Version 6.0 r02)
David Woolf: Added tags to titles of FYI tests to help readers determine what tests were mandatory versus FYI. Added Appendix outlining which tests were Mandatory, Optional (dependent on feature support), and FYI. Previously this information was in the NVMe Integrators List Policy Document.

2016 May 26 (Version 6.0 r03)
David Woolf: Added requirement to tests 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 2.3, 2.4, 2.6 that all Reserved fields be checked and that they are set to 0.

2016 June 9 (Version 6.0 r04)
David Woolf: Added tests 1.8,1.9, 2.8, 2.9, 3.4, 3.5, 4.18, 8.3.

2016 June 13 (Version 6.0 r05)
David Woolf: Added tests 2.10, 10.1. Added Case 2 to test 2.9 to address the case where Atomic Boundaries are supported.

2016 June 27 (Version 6.0 r06)
David Woolf: Added new subtests to 1.1, 1.2, 1.3, 1.6, 2.1, 2.3, 2.4, 2.5, 2.6, 2.7. Added checking of CSTS.NSSRO to test 6.4.
2016 June 28 (Version 6.0 r07)
David Woolf: Added new subtests to 1.4. Added Mandatory, Optional, FYI designations to all Tests and Cases within Tests. Edited Appendix D for a clearer description of the meaning of Mandatory, Optional, and FYI test designations and NVMe Integrators List requirements.

2016 July 5 (Version 6.0 r08)
David Woolf: Added Case 9 in Test 1.4, added Case 11 in Test 2.3, added Case 11 in Test 2.4. Added Case 4 and 5 to Test 2.2.

2016 July 7 (Version 6.0 r09)
David Woolf: replaced “Optional” indication with “Mandatory if Supported” in all test titles and Appendix D. Flagged ‘Test 1.6 – Format NVM’ as “Mandatory if Supported”, previously it had been indicated as “Mandatory”. Replaced ‘optional’ with “Mandatory if Supported” in the ‘Possible Problems’ section of several tests.

2016 July 7 (Version 6.0 r10)
David Woolf: Adjusted procedure of Case 2 of test 2.6. Fixed typos in Test 1.6 Test Cases 2 and 3.

2016 July 14 (Version 6.0 r11)
David Woolf: Adjusted procedure of subtest cases in Tests 2.1, 2.3, 2.4, 2.5, 2.6, 2.7 dealing with Invalid Namespace ID Errors.

2016 July 21 (Version 6.0 r12)
David Woolf: Adjusted procedure of Case 1 in Tests 9.2 to check both the case where number of Namespaces is exceeded and the Namespace size is exceeded. Corrected typos in Test Procedure for Test 2.4 cases 8, 9, 10,11 and Test 2.3 case 11. Adjusted procedure in Test 1.3 Cases 7 and 8 so that enough bytes are read to increment the Data Units Read/Written value. Adjusted procedure in Test 2.5 Case 2, 3, 4, 5 and Test 2.7 case 5.

2016 July 21 (Version 6.0 r13)
David Woolf: Adjusted procedures to Test 1.3 Case 1 and 4 to only check Mandatory values. Test 1.3 Case 5 was updated to check that error log entries properly increment. Clarified Test 1.3 Case 4.

2016 August 30 (Version 6.0)

2016 September 26 (Version 6.1 r01)
David Woolf:
- Added indication to several tests Group 7, that some cases are only applicable to Dual Port Devices.
- Updated Test 7.1 Case 2 Observable results steps 3 and 7.
- Updated Test 7.2 Case 3 Procedure step 1.b.vi.
- Separated Test 9.2 Case 1 into 2 separate cases, now Test 9.2 Case 1 addressing having too many Namespaces, and Case 3 addressing having insufficient capacity.
- Modified Test 1.3 Case 4 to accommodate for changes between specs 1.2a and 1.2.1.
- Modified Test 2.3 Case 3 and Test 2.4 Case 3.

January 17, 2017 (Version 7.0 r01)
David Woolf:
- Changed indication of FYI to Mandatory or In Progress for many tests based on results of Plugfest #6.
- Corrected Observable Results for Test 1.3 Case 2 and 3 to expect ‘Invalid Log Page’ rather than ‘Invalid Field in Command’.
- Fixed typo in Test 1.5.
• Updated Test 2.5 Case 5 and Test 2.7 Case 5 per ECN 003 of NVMe Specification v1.2.1. This ECN alters behavior expected in earlier versions. Now the expected behavior is each case is that the device report status of Successful.

January 24, 2017 (Version 7.0 r02)
David Woolf:
• Changed indication of FYI to Mandatory or In Progress for tests 3.4 Case 2, and 6.2 based on NVMe Interop and Compliance Committee direction.

February 9, 2017 (Version 7.0 r03)
David Woolf:
• Added FYI Test 1.4 Case 10.

March 22, 2017 (Version 7.0)
David Woolf:
• Final version published to UNH-IOL site ahead of May 2017 NVMe Plugfest #7.

June 17, 2017 (Version 7.0a)
David Woolf:
• Test requirements relaxed in tests 1.1 Case 4, 2.7 Case 9, 2.8 Case 1, 7.1 Case 2, 7.2, and 9.2 Case 3, due to discoveries during May 2017 plugfest. Test Procedure clarified for Test 1.4 Case 7.

August 14, 2017 (Version 8.0)
David Woolf:
• Test requirements relaxed in tests 1.1 Case 4, 2.7 Case 9, 2.8 Case 1, 7.1 Case 2, 7.2, and 9.2 Case 3, due to discoveries during May 2017 plugfest. Test Procedure clarified for Test 1.4 Case 7.
• Clarification in procedure for test 1.2 Case 4.
• Tests 2.3 and 2.4 Case 4 (NLB>MDTS) modified to be ‘Mandatory if Supported’, as these tests are only applicable if MDTS is not equal to 0.
• Tests 2.3 and 2.4 Case 7 modified to be ‘Mandatory if Supported’, as these tests are only applicable if NN is not equal to 0xFFFFFFFF.
• Test 1.3 Case 4 modified to be Mandatory if Supported depending on whether MDTS=0 or not. Test modified to expect “Invalid Field in Command” if MDTS conflicts with NUMD/NUMDU/NUMDL.
• Added Test Case 1.3 Case 10.
• Modified Test 2.1 to perform compares using a known sequence rather than the Identify Log Page data to simplify test implementation.
• Clarified Test 2.9 Case 1 that both NABSN and NADSPF need to be set to zero for the test to applicable.
• Clarified Test 2.9 Case 2 that either NABSN and NADSPF need to be set to non-zero values for the test to applicable.
• Modified Test 5.5 to make each condition tested into a separate test case. Most test procedures were not modified and so remain Mandatory, with the exception of case 6 which had the procedure modified and is marked FYI.
• Modified Table in Test 5.5 to clarify which status codes were tested and which were not.
• Modified Appendix D to show abbreviations for test case requirements.
• Modified Test 5.5 Case 5, to indicate that if no features are indicated as ‘Not Changeable’ then the test case does not apply.
• Moved Abbreviations from Appendix D to a new section near the beginning of the document, named ‘Abbreviations’.
• Tests 2.5 Case 5, 2.7 Case 5, 3.4 Case 1, 7.3 Case 1, 1.4 Case 9 had status changed from FYI to Mandatory or Mandatory if Supported.
• Tests 1.1 Case 4, 1.7 Case 1, 2.2 Case 3, 4, 5, 2.7 Case 9, 2.9 Case 2, 7.1 Case 2 and 7.2 had status changed from In Progress to FYI.

September 12, 2017 (Version 8.0a)
David Woolf:
- Updated Appendix C.

October 24, 2017 (Version 8.0b)
David Woolf:
- Updated Appendix D to clarify test requirements designations for NVMeoF products.

November 14, 2017 (Version 9.0 draft)
David Woolf:
1. Updated Target Specification on cover page to be NVMe v1.3
2. Updated Default Test Setup diagram in Appendix A.
3. Updated Test 1.3 Case 5 to check the M bit.
4. Fixed error in Test 2.4 Case 3, where Step 1 was referred to in the Test Procedure rather than Step 2, also corrected the Status Code expected in Observable Result step 2 from 0x0A to 0x80. Also updated test to allow for DUT to report status code 0x81, since the status reported would be dependent on which check is performed first, accounting for NVMe v1.3 ECN 002.
5. Fixed error in Test 2.4 Case 6 where a Read command was indicated instead of a Write command.
6. Fixed error in Test 2.4 Case 6 where Step 1 was referred to in the Test Procedure rather than Step 2.
7. Fixed error in Test 2.4 Case 7 where a Read command was indicated instead of a Write command.
8. Fixed error in Test 2.4 Case 7 where Step 1 was referred to in the Test Procedure rather than Step 2.
9. Fixed error in Test 2.3 Case 2, 3, 4, 5, 6, 7 where a data pattern was written, this step was not necessary.
10. Updated Test 4.18 to allow devices to report support for NVMe v1.3. Added check to ensure that VER value from Identify Controller Data structure matches the value in VS.CAP.
11. Updated Test 2.1 Case 4 to match new requirements in NVMe 1.3 ECN 002, which eliminated the requirement for a DUT to report the lowest numerical value status code first.
12. Updated Test 2.3 Case 4 to match new requirements in NVMe 1.3 ECN 002, which eliminated the requirement for a DUT to report the lowest numerical value status code first.
13. Updated Test 2.3 Case 7 to match new requirements in NVMe 1.3 ECN 002, which eliminated the requirement for a DUT to report the lowest numerical value status code first.
14. Updated Test 2.4 Case 4 to match new requirements in NVMe 1.3 ECN 002, which eliminated the requirement for a DUT to report the lowest numerical value status code first.
15. Updated Test 2.4 Case 7 to match new requirements in NVMe 1.3 ECN 002, which eliminated the requirement for a DUT to report the lowest numerical value status code first.
16. Updated Test 2.7 Case 3 to match new requirements in NVMe 1.3 ECN 002, which eliminated the requirement for a DUT to report the lowest numerical value status code first.
17. Updated Test 2.7 Case 4 to ensure that final READ command returns all 0’s.
18. Updated Test 2.1 Case 3 to better match the wording in NVMe 1.3 Figure 32.

Removed steps in Test Procedure and Observable Results for Test 2.4 Cases 2-7 where a Read command was used to double check that a Write command had not caused data to be written, since those Read commands themselves could not be performed successfully, and those cases are also checked in Test 2.3

November 28, 2017 (Version 9.0 draft)
David Woolf:
1. Updated Test 1.2 Cases 1-4 Test Procedures and Observable Results to be more complete.
2. Updated Abbreviations section to stop using the ‘Mandatory if Supported’ nomenclature.
3. Updated Test 1.3 Case 4 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for MDTS value at the beginning of the test to determine if the test is applicable to the DUT or not.
4. Updated Test 1.6 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for OACS field at the beginning of the test to determine if the test is applicable to the DUT or not.
5. Updated Test 2.1 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for ONCS field at the beginning of the test to determine if the test is applicable to the DUT or not.
6. Updated Test 2.2 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for ONCS field at the beginning of the test to determine if the test is applicable to the DUT or not.
7. Updated Test 2.3 Case 4 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for MDTS value at the beginning of the test to determine if the test is applicable to the DUT or not.
8. Updated Test 2.3 Case 7 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for NN value at the beginning of the test to determine if the test is applicable to the DUT or not.
9. Updated Test 2.3 Case 6 to include a check for NN value at the beginning of the test to determine if the test is applicable to the DUT or not.
10. Updated Observable Results of Test 2.3 Case 6 to check for status code ‘Invalid Namespace or Format (0BH).
11. Updated Test 2.4 Case 4 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for MDTS value at the beginning of the test to determine if the test is applicable to the DUT or not.
12. Updated Test 2.4 Case 7 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for NN value at the beginning of the test to determine if the test is applicable to the DUT or not.
13. Updated Test 2.5 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for ONCS field at the beginning of the test to determine if the test is applicable to the DUT or not. Added checks for MDTS and NN values where appropriate.
14. Updated Test 2.7 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for ONCS field at the beginning of the test to determine if the test is applicable to the DUT or not. Added checks for MDTS and NN values where appropriate.
15. Updated Test 2.7 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for NABSN field at the beginning of the test to determine if the test is applicable to the DUT or not.
16. Updated Test 3.1 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for Metadata Size field at the beginning of the test to determine if the test is applicable to the DUT or not.
17. Updated Test 3.2 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for DPC field at the beginning of the test to determine if the test is applicable to the DUT or not.
18. Updated Test 3.4 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check for HMPRE field at the beginning of the test to determine if the test is applicable to the DUT or not.
19. Updated Test 4.13 to be ‘Mandatory’ instead of ‘Mandatory if Supported’.
20. Updated Test 5.5 Case 3 to be ‘Mandatory’ instead of ‘Mandatory if Supported’.
21. Updated Test 6.4 to be ‘Mandatory’ instead of ‘Mandatory if Supported’.
22. Updated all tests in Group 7 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check in all tests of the ONCS field to determine of the controller supports reservations.
23. Updated all tests in Group 9 to be ‘Mandatory’ instead of ‘Mandatory if Supported’. Added a check in all tests of the OACS field to determine of the controller supports Namespace Management.
24. Updated Appendix D to remove all references to ‘Mandatory if Supported’.
25. Updated Table in Test 1.2 to contain new Features: Timestamp, Keep Alive Timer, Host Controller Thermal Management, Non-Operational Power State Config.
26. Updated Test 2.4 Cases 8, 9, 10 to remove redundant READ operation in Test Procedure.

December 4, 2017 (Version 9.0 draft)
David Woolf:
1. Updated Test 2.5 Case 5 to include more than 1 READ command to be performed after the Write Uncorrectable command in order to ensure that all LBAs affected by the Write Uncorrectable command are affected.
2. Updated Test 2.7 Case 5 to include more than 1 READ command to be performed after the Write Zeroes command in order to ensure that all LBAs affected by the Write Zeroes command are affected.

December 6, 2017 (Version 9.0 draft)
David Woolf:
1. Updated Test 1.6 Case 3 to include a check of FNA Bit 2, to determine if the test case is applicable or not.
2. Updated Test 1.1 Case 5, to show that CNS reserved value testing should check only FFh.

December 12, 2017 (Version 9.0 draft)
David Woolf:
1. Updated Test 1.3 Case 3 to only check LID 7Fh.
2. Updated Test 1.2 Case 5 to only check SEL 111b.
3. Updated Test 2.2 Case 3, Case 4, and Case 5 to be Mandatory for NVMe Drives.
4. Updated Test 1.4 Case 10 to be Mandatory for NVMe Drives.
5. Updated Test 1.7 Case 1 to be Mandatory for NVMe Drives.
6. Updated Test 2.3 Case 11 to be Mandatory for NVMe Drives.
7. Updated Test 2.4 Case 11 to be Mandatory for NVMe Drives.
8. Updated Test 2.7 Case 9 to be Mandatory for NVMe Drives.
9. Updated Test 2.9 Case 2 to be Mandatory for NVMe Drives.
10. Updated Test 5.5 Case 6 to be Mandatory for NVMe Drives.

December 14, 2017 (Version 9.0 draft)
David Woolf:
1. Added Test 1.1 Case 6.
2. Added Test 1.10 Cases 1-8
3. Added Test 1.11 Cases 1-8
4. Added Test 1.12 Cases 1-5
5. Added Test 1.13 Cases 1-4

December 21, 2017 (Version 9.0 draft)
David Woolf:
1. Updated Observable Results in Test 3.4 Case 2 to eliminate items that can not be observed. Changed the test status to FYI.
2. Updated Observable Results in Test 3.4 Case 3 to eliminate items that can not be observed. Changed the test status to FYI.

January 4, 2018 (Version 9.0 draft)
David Woolf:
1. Updated all references in Group 9 from 8.11 to 8.12 to match NVMe v1.3 specification.

January 22, 2018 (Version 9.0 draft)
Colin Dorsey:
1. Added tests 8.4, 8.5, 8.6, 8.7, 8.8. Updated test procedures for test 8.2

January 23, 2018 (Version 9.0 draft)
David Woolf:
1. Updated following tests from OF-FYI to OF to indicate that they are now mandatory for NVMe-oF products, per ICC decision: 1.1 Cases 1-2, 1.3 Cases 1-2, 1.7 Case 2, 2.5 all cases, 2.6 Case 2, 2.8, 3.3 Cases 1-4, 4.1, 4.2, 4.3, 4.4, 4.6, 4.7, 4.9, 4.10, 4.11, 4.12, 4.13, 4.14, 4.15, 4.16, 4.17, 4.18, 5.1.

February 1, 2018 (Version 9.0 draft)
David Woolf:
1. Updated test 4.13 test procedure for clarity.
2. Updated test 3.4 Case 3 test procedure for clarity and completeness.

February 5, 2018 (Version 9.0 draft)
David Woolf:
1. Modified Case 6 to Test 1.1 to cover Namespace Identification Descriptors.
2. Added Test 1.3 Cases 11, 12, 13, 14, 15 to address Telemetry Log Pages.

March 15, 2018 (Version 9.0 draft)
David Woolf:
1. Modified Case 3 of Test 1.2 for clarity.
2. Modified Test 7.1 Case 2 and Test 7.2 Case 3 to include the step of performing a Reservation Acquire command.
3. Modified Test 1.2 Case 4, there was a typo indicated DWord 10 rather than DWord 0.

May 21, 2018 (Version 10.0 draft)
David Woolf:
1. Corrected typo in Test 2.2 Case 2
David Woolf:
1. 10.0 Release
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INTRODUCTION

The University of New Hampshire’s InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards-based products by providing a neutral environment where a product can be tested against other implementations of a common standard, both in terms of interoperability and conformance. This particular suite of tests has been developed to help implementers evaluate the NVMe functionality of their products. This test suite is aimed at validating products in support of the work being directed by the NVMe Promoters Group.

These tests are designed to determine if a product conforms to specifications defined in the NVM Express Revision 1.2 specification, hereafter referred to as the “NVMe Specification”). Successful completion of these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many NVMe environments.

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A two-number, dot-notated naming system is used to catalog the tests. This format allows for the addition of future tests in the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

**Purpose**

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

**References**

This section specifies all reference material external to the test suite, including the specific references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g., [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the test suite document itself (e.g., “Appendix 5.A”, or “Table 5.1.1–1”).

**Resource Requirements**

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

**Last Modification**

This specifies the date of the last modification to this test.

**Discussion**

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here as well.

**Test Setup**

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section (next).

**Procedure**

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results. These procedures should be the ideal test methodology, independent of specific tool limitations or restrictions.

**Observable Results**
This section lists the specific observable items that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems
This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or other external sources that may provide more detail regarding these issues.
REFERENCES

The following documents are referenced in this text:

1. NVM Express Revision 1.3 Specification (May 1, 2017)
2. NVM Express Management Interface Revision 1.0a Specification (April 8, 2017)
**ABBREVIATIONS**

The following abbreviations are applied to the test titles of each of the tests described in this document for indicating the status of test requirements.

- **M** - Mandatory
- **FYI** - FYI
- **IP** - In Progress

The following abbreviations applied to the test titles of each of the tests described in this document for indicating what product types a test may apply to. It is assumed that all tests apply to base NVMe products using PCIe.

- **OF** – Test applies to NVMeoF products
Group 1: Admin Command Set

Overview:
This section describes a method for performing conformance verification for NVMe products implementing the Admin Command Set.

Notes:
The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 1.1 – Identify Command (M, OF)

Purpose: To verify that an NVMe Controller can properly execute an Identify command.

References:
[1] NVMe Specification 5.15

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: February 5, 2018

Discussion: The Identify command returns a data buffer that describes the NVM subsystem, the controller or the namespace(s). The data structure is 4096 bytes in size. The host indicates as a command parameter whether to return the controller or namespace specific data structure. For the namespace data structure, the definition of the structure is specific to the I/O command set selected for use.

The data structure returned, defined in Table 1, is based on the Controller or Namespace Structure (CNS) field. If there are fewer namespace identifiers or controller identifiers to return for a Namespace List or Controller List, respectively, then the unused portion of the list is zero filled. Controllers that support Namespace Management shall support CNS values of 10h–13h.

The Identify command uses the PRP Entry 1, PRP Entry 2, and Command Dword 10 fields. All other Command specific fields are reserved.

A completion queue entry is posted to the Admin Completion Queue when the Identify data structure has been posted to the memory buffer indicated in PRP Entry 1.

Test Setup: See Appendix A.

Case 1: Identify Namespace Data Structure (M, OF)

Test Procedure:
1. For each namespace in the NVM subsystem, configure the NVMe Host to issue an Identify command specifying CNS value 00h to the controller in order to receive back an Identify Namespace data structure for the specified namespace.

Observable Results:
1. Verify that the requested data structure is posted to the memory buffer indicated in PRP Entry 1, PRP Entry 2, and Command Dword 10, and that a command completion queue entry is posted to the Admin Completion Queue.
2. Verify all received responses have all Reserved fields set to 0.
3. Verify that the requested data structure is zero filled.

Case 2: Identify Controller Data Structure (M, OF)

Test Procedure:
1. Configure the NVMe Host to issue an Identify command specifying CNS value 01h to the controller in order to receive back an Identify Controller data structure.

Observable Results:
1. Verify that the requested data structure is posted to the memory buffer indicated in PRP Entry 1, PRP Entry 2, and Command Dword 10, and that a command completion queue entry is posted to the Admin Completion Queue.
2. Verify that all received responses have all Reserved fields set to 0.
3. If the DUT claims support for NVMe Version 1.2 or higher, verify that the value reported for Version support in the CAP register (VS Offset 08h), matches the value reported in the Identify Controller Data Structure VER field (83:80) and is non-zero.
4. Verify that any power state descriptors not supported (i.e. Power States beyond the number reported in the NPSS value (263) in the Identify Controller Data Structure) are set to 0.
5. Verify that any values that are reported as ASCII strings (specifically Serial Number – SN, Model Number – MN, and Firmware Revision – FR) are left justified and padded with spaces (ASCII 20h character) to the right.

### Table 1 – Identify – Data Structure Returned

<table>
<thead>
<tr>
<th>CNS Value</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>The Identify Namespace data structure is returned to the host for the namespace specified in the Namespace Identifier (CDW1.NSID) field if it is an active namespace ID. If the specified namespace is an inactive namespace ID, then the controller returns a zero filled data structure.</td>
</tr>
<tr>
<td></td>
<td>If the controller supports Namespace Management and CDW1.NSID is set to FFFFEFFFFh, the controller returns an Identify Namespace data structure that specifies capabilities that are common across namespaces.</td>
</tr>
<tr>
<td>01h</td>
<td>The Identify Controller data structure is returned to the host for this controller.</td>
</tr>
<tr>
<td>02h</td>
<td>A list of 1024 namespace IDs is returned containing active namespace IDs attached to this controller in increasing order that are greater than the value specified in the Namespace Identifier (CDW1.NSID) field of the command. The data structure returned is a Namespace List (refer to section 4.8).</td>
</tr>
<tr>
<td></td>
<td>Controllers that support specification revision 1.1 or later shall support this capability.</td>
</tr>
<tr>
<td>03h–0Fh</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>Namespace Management</td>
</tr>
<tr>
<td>10h</td>
<td>A list of up to 1024 namespace IDs is returned to the host containing namespaces that are present in the NVM subsystem with a namespace identifier greater than the value specified in the Namespace Identifier (CDW1.NSID) field. The namespaces may or may not be attached to controller(s).</td>
</tr>
<tr>
<td>11h</td>
<td>The Identify Namespace data structure is returned to the host for the namespace specified in the Namespace Identifier (CDW1.NSID) field. The namespace may or may not be attached to this controller. If the specified namespace is invalid then the controller shall fail the command with a status code of Invalid Namespace or Format.</td>
</tr>
<tr>
<td>12h</td>
<td>A Controller List of up to 2047 controller identifiers is returned containing a controller identifier greater than or equal to the value specified in the Controller Identifier (CDW10.CNTID) field. The list contains controller identifiers that are attached to the namespace specified in the Namespace Identifier (CDW1.NSID) field.</td>
</tr>
<tr>
<td>13h</td>
<td>A Controller List of up to 2047 controller identifiers is returned containing a controller identifier greater than or equal to the value specified in the Controller Identifier (CDW10.CNTID) field. The list contains controller identifiers in the NVM subsystem that may or may not be attached to the namespace(s).</td>
</tr>
<tr>
<td>14h–1Fh</td>
<td>Reserved</td>
</tr>
<tr>
<td>20h–FFh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### Future Definition

**Case 3: Namespace List (M, OF-FYI)**

**Test Procedure:**
1. Configure the NVMe Host to issue an Identify command specifying CNS value 02h and CDW1.NSID value 0 to the controller in order to receive back a Namespace List containing active namespace IDs.
2. For each namespace ID returned in the Namespace List, configure the host to issue an Identify command specifying CNS value 00h to the controller in order to receive back an Identify Namespace data structure for the specified namespace.

Observable Results:
1. Verify that the requested Namespace List is posted to the memory buffer indicated in PRP Entry 1, PRP Entry 2, and Command Dword 10, and that a command completion queue entry is posted to the Admin Completion Queue.
2. For each Identify command in step 2, verify that the returned data structure is not zero filled since each namespace ID in the Namespace List should be active.
3. Verify that all received responses have all Reserved fields set to 0.

Case 4: Identify to invalid Controller ID (FYI, OF-IP)

Test Procedure:
1. For each namespace in the NVM subsystem, configure the NVMe Host to issue an Identify command specifying an invalid CNTID in Command Dword 10.

Observable Results:
1. Verify that the command returns status ‘Invalid Field in Command’ 02h.

Case 5: Identify to reserved CNS Value (M, OF-IP)

Test Procedure:
1. For each namespace in the NVM subsystem, configure the NVMe Host to issue an Identify command specifying a CNS of FFh.

Observable Results:
1. Verify that the command returns status ‘Invalid Field in Command’ 02h.

Possible Problems: None.

Case 6: Namespace Identification Descriptors (FYI, OF-FYI)

Test Procedure:
1. Check the Identify Controller Data Structure to determine what version of the NVMe specification the product under test claims to support. If the product under test does not support NVMe v1.3 or higher, this test is not applicable.
2. For each namespace in the NVM subsystem, configure the NVMe Host to issue an Identify command specifying CNS value 03h to the controller in order to receive back the Namespace Identification Descriptor data structure for the specified namespace.

Observable Results:
1. Verify that the command returns one or more Namespace Identification Descriptor structures that fit into the 4096 byte Identify payload.
2. Verify that the controller does not return multiple descriptors with the same Namespace Identification Descriptor Type (NIDT).

Possible Problems: None.
**Test 1.2 – Set/Get Features Commands (M, OF-FYI)**

**Purpose:** To verify that an NVMe Controller can properly execute a Get Features command. Also to verify that the NVMe Controller properly sets feature values after the NVMe Host issues a Set Features command.

**References:**
[1] NVMe Specification 5.13, 5.21

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 28, 2017

**Discussion:** The Get Features command retrieves the attributes of the Feature indicated. The Get Features command uses the PRP Entry 1, PRP Entry 2, and Command Dword 10 fields. All other command specific fields are reserved.

The Set Features command specifies the attributes of the Feature indicated. The Set Features command uses the PRP Entry 1, PRP Entry 2, Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15 fields. All other command specific fields are reserved.

The desired feature is specified in the Feature Identifier (FID) field of CDW10. Valid Feature Identifiers are described in Table 2 and Table 3.

**Table 2 – Feature Identifiers**

<table>
<thead>
<tr>
<th>Feature Identifier</th>
<th>Optional/ Mandatory</th>
<th>Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>N/A</td>
<td>Reserved</td>
</tr>
<tr>
<td>01h</td>
<td>Mandatory</td>
<td>Arbitration</td>
</tr>
<tr>
<td>02h</td>
<td>Mandatory</td>
<td>Power Management</td>
</tr>
<tr>
<td>03h</td>
<td>Optional</td>
<td>LBA Range Type</td>
</tr>
<tr>
<td>04h</td>
<td>Mandatory</td>
<td>Temperature Threshold</td>
</tr>
<tr>
<td>05h</td>
<td>Mandatory</td>
<td>Error Recovery</td>
</tr>
<tr>
<td>06h</td>
<td>Optional</td>
<td>Volatile Write Cache</td>
</tr>
<tr>
<td>07h</td>
<td>Mandatory</td>
<td>Number of Queues</td>
</tr>
<tr>
<td>08h</td>
<td>Mandatory</td>
<td>Interrupt Coalescing</td>
</tr>
<tr>
<td>09h</td>
<td>Mandatory</td>
<td>Interrupt Vector Configuration</td>
</tr>
<tr>
<td>0Ah</td>
<td>Mandatory</td>
<td>Write Atomicity Normal</td>
</tr>
<tr>
<td>0Bh</td>
<td>Mandatory</td>
<td>Asynchronous Event Configuration</td>
</tr>
<tr>
<td>0Ch</td>
<td>Optional</td>
<td>Autonomous Power State Transition</td>
</tr>
<tr>
<td>0Dh</td>
<td>Optional</td>
<td>Host Memory Buffer</td>
</tr>
<tr>
<td>0Eh</td>
<td>Optional</td>
<td>Timestamp</td>
</tr>
</tbody>
</table>
A completion queue entry is posted to the Admin Completion Queue when the controller has completed returning any attributes associated with the Feature. Depending on the Feature Identifier, Dword 0 of the completion queue entry may contain feature information.

**Test Setup:** See Appendix A.

**Case 1: SEL = 000b (M, OF-FYI)**

**Test Procedure:**

1. For each of the features described in Table 2 and Table 3, perform the following:
   a. Configure the NVMe Host to issue a Get Features command with SEL field set to 000b indicating the specified FID value in CDW10 to the controller.
   b. Configure the NVMe Host to issue a Set Features command indicating the specified FID value in CDW10 setting valid values for any features indicated as changeable by the controller.
   c. Configure the NVMe Host to issue a second Get Features command with SEL field set to 000b indicating the specified FID value in CDW10 to the controller.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that the controller returns the Feature Information for each FID as specified in of the NVMe Specification for each Get Features command issued by the NVMe Host.
3. Verify that the Feature Information returned in the second Get Features command matches the values which were set by the NVMe Host using the Set Features command, if that feature is changeable.
4. Verify that all received responses have all Reserved fields set to 0.

**Case 2: SEL = 001b (M, OF-FYI)**

**Test Procedure:**
1. Check the Bit 4 of the ONCS field to determine if the DUT supports setting the Save field in a Set Features command to a non-zero value and the Select field of the Get Features command to a non-zero value. If Bit 4 is set to 0, this test is not applicable.

2. For each of the features described in Table 2 and Table 3, perform the following:
   a. Configure the NVMe Host to issue a Get Features command with SEL field set to 000b indicating the specified FID value in CDW10 to the controller.
   b. Configure the NVMe Host to issue a Get Features command with SEL field set to 001b indicating the specified FID value in CDW10 to the controller.
   c. Configure the NVMe Host to issue a Set Features command indicating the specified FID value in CDW10 changing the feature values for the feature to the controller, if that feature is changeable.
   d. Configure the NVMe Host to issue a Get Features command with SEL field set to 000b indicating the specified FID value in CDW10 to the controller.

Configure the NVMe Host to issue a Get Features command with SEL field set to 001b indicating the specified FID value in CDW10 to the controller.

**Observed Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that the controller returns the Feature Information for each FID as specified in section 5.12 of the NVMe Specification for each Get Features command issued by the NVMe Host.
3. Verify that features values returned in Step b and d have changed.
4. Verify that feature values returned in step c and e have not changed.
5. Verify that all received responses have all Reserved fields set to 0.

**Case 3: SEL = 010b (M, OF-FYI)**

**Test Procedure:**

1. Check the Bit 4 of the ONCS field to determine if the DUT supports setting the Save field in a Set Features command to a non-zero value and the Select field of the Get Features command to a non-zero value. If Bit 4 is set to 0, this test is not applicable.

2. For each of the features described in Table 2 and Table 3, perform ensure that the feature is supported as saveable by the DUT. If the DUT does not support any features as saveable, this Test Case is not applicable. If the DUT does support certain features as saveable, perform the following:
   a. Configure the NVMe Host to issue a Get Features command with SEL set to 000b indicating the specified FID value in CDW10 to the controller.
   b. Configure the NVMe Host to issue a Set Features command with the SV bit set to 1 indicating the specified FID value in CDW10 setting changed values for the feature to the controller, for all changeable values.
   c. Configure the NVMe Host to issue a second Get Features command with SEL=010b indicating the specified FID value in CDW10 to the controller.
   d. Perform a Controller reset.
   e. Configure the NVMe Host to issue a second Get Features command with SEL=010b indicating the specified FID value in CDW10 to the controller.

**Observed Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that the controller returns the Feature Information for each FID as specified in section 5.12 of the NVMe Specification for each Get Features command issued by the NVMe Host.
3. Verify that the Feature Information returned in the second Get Features command matches the values which were set by the NVMe Host using the Set Features command, and were saved across the reset event.
4. Verify that all received responses have all Reserved fields set to 0.

**Case 4: SEL = 011b (M, OF-FYI)**
Test Procedure:
1. Check the Bit 4 of the ONCS field to determine if the DUT supports setting the Save field in a Set Features command to a non-zero value and the Select field of the Get Features command to a non-zero value. If Bit 4 is set to 0 this test is not applicable.
2. For each of the features described in Table 2 and Table 3, perform the following:
   a. Configure the NVMe Host to issue a Get Features command with SEL=011b indicating the specified FID value in CDW10 to the controller. Record the value of Dword 0 bits 0, 1, and 2 returned in the Completion Entry.
   b. Perform a Set Feature command with the SV field set to 1 for the specified FID.
   c. Perform a Get Feature command with the SEL field set to 000b, with NSID set to 1.
   d. Perform a Get Feature command with the SEL field set to 000b, with NSID set to 0.
Perform a valid Get Feature command with SEL set to 000b, followed by a valid Set Feature command with a new value for the specified FID.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that in step b, if bit 0 of Dword 0 of the completion entry is set to 0, the controller returns Invalid Field in Command. If bit 0 of Dword 0 of the completion entry is set to 1, verify that the command completes successfully.
3. Verify that in step c, if bit 1 of Dword 0 of the completion entry is set to 0, the DUT returns Invalid Namespace. If bit 1 of Dword 0 of the completion entry is set to 1, the command completes successfully.
4. Verify that in step d, if bit 1 of Dword 0 of the completion entry is set to 0, the command completes successfully. If bit 1 of Dword 0 of the completion entry is set to 1, the DUT returns Invalid Namespace.
5. Verify that in step e, if bit 2 of Dword 0 of the completion entry is set to 0, the controller returns Feature not Changeable for the Set Features command. If bit 2 of Dword 0 of the completion entry is set to 1, the command completes successfully.

Case 5: SEL = Reserved Value (M, OF-FYI)

Test Procedure:
1. For each of the features described in Table 2 and Table 3, perform a Get Features command with the SEL field set to 111b.

Observable Results:
1. Verify that after the completion of each command, the controller returns Error Status 02h, Invalid Field in command.

Possible Problems: None.
Test 1.3 – Get Log Page Command (M, OF)

**Purpose:** To verify that an NVMe Controller can properly execute a Get Log Page command.

**References:**
[1] NVMe Specification 5.14

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** February 5, 2018

**Discussion:** The Get Log Page command returns a data buffer that contains the log page requested. The Get Log Page command uses the PRP Entry 1, PRP Entry 2, and Command Dword 10 fields. All other command specific fields are reserved.

The desired log page is specified in the Log Page Identifier (LID) field of CDW10. Valid Log Identifiers are described in Table 4 and Table 5.

<table>
<thead>
<tr>
<th>Log Identifier</th>
<th>Optional/Mandatory</th>
<th>Log Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>N/A</td>
<td>Reserved</td>
</tr>
<tr>
<td>01h</td>
<td>Mandatory</td>
<td>Error Information</td>
</tr>
<tr>
<td>02h</td>
<td>Mandatory</td>
<td>SMART / Health Information</td>
</tr>
<tr>
<td>03h</td>
<td>Mandatory</td>
<td>Firmware Slot Information</td>
</tr>
<tr>
<td>04h</td>
<td>Optional</td>
<td>Changed Namespace List</td>
</tr>
<tr>
<td>05h</td>
<td>Optional</td>
<td>Command Effects Log</td>
</tr>
<tr>
<td>06h</td>
<td>Optional</td>
<td>Device Self Test</td>
</tr>
<tr>
<td>07h</td>
<td>Optional</td>
<td>Telemetry Host-Initiated</td>
</tr>
<tr>
<td>08h</td>
<td>Optional</td>
<td>Telemetry Controller Initiated</td>
</tr>
<tr>
<td>09h – 6Fh</td>
<td>N/A</td>
<td>Reserved</td>
</tr>
<tr>
<td>70h</td>
<td></td>
<td>Discovery</td>
</tr>
<tr>
<td>71h-7Fh</td>
<td></td>
<td>Reserved for NVMe over Fabrics</td>
</tr>
<tr>
<td>80h – BFh</td>
<td>N/A</td>
<td>I/O Command Set Specific</td>
</tr>
<tr>
<td>CFh – FFh</td>
<td>N/A</td>
<td>Vendor Specific</td>
</tr>
</tbody>
</table>

**Table 4 – Log Page Identifiers**

<table>
<thead>
<tr>
<th>Log Identifier</th>
<th>Optional/Mandatory</th>
<th>Log Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>80h</td>
<td>Optional</td>
<td>Reservation Notification</td>
</tr>
<tr>
<td>81h</td>
<td>Optional</td>
<td>Sanitize Status</td>
</tr>
<tr>
<td>82h – BFh</td>
<td>N/A</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

A completion queue entry is posted to the Admin Completion Queue when the log has been posted to the memory buffer indicated in PRP Entry 1.

**Test Setup:** See Appendix A.
Case 1: Supported LIDs (M, OF)

Test Procedure:
1. Configure the NVMe Host to issue a Get Log Page command specifying each of the Mandatory Log Page Identifiers described in Table 4 and 5 above, to the NVMe Controller.

Observable Results:
1. Verify that a completion queue entry is posted to the Admin Completion Queue when the log has been posted to the memory buffer indicated in PRP Entry 1.
2. In each case verify that the information returned in the Log Page information is formatted according to the respective descriptions for the log pages in section 5.14 of the NVMe Specification.
3. Verify that all received responses have all Reserved fields set to 0.

Case 2: Unsupported Vendor Specific LIDs (M, OF)

Test Procedure:
1. Configure the NVMe Host to issue a Get Log Page command specifying a vendor specific log identifier not supported by the NVMe Controller.

Observable Results:
1. Verify that each command completes with an error code of Invalid Log Page 09h.
2. Verify that all received responses have all Reserved fields set to 0.

Case 3: Reserved LIDs (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue a Get Log Page command specifying log identifiers of 00h, and 7fh.

Observable Results:
1. Verify that each command completes with an error code of Invalid Log Page 09h.
2. Verify that all received responses have all Reserved fields set to 0.

Case 4: NUMD/MDTS Conflict (M, OF-FYI)

Test Procedure:
1. Check the MDTS value reported by the DUT in the Identify Controller Data Structure. If MDTS is set to 0 (i.e. unlimited) then this test is not applicable.
2. Check the NVME Specification version supported by DUT using the value reported in the Identify Controller Data Structure VER field (83:80). If the DUT supports v1.2.1 or higher go to step 2. If the DUT supports v1.2a or lower (or VER is set to 0, go to step 3).
3. Set the NUMDU and NUMDL values to be greater than the MDTS value provided by the DUT in the Identify Controller Data Structure. Configure the NVMe Host to issue a Get Log Page command specifying each of the Mandatory Log Page Identifiers described in Figure 77 and 78.
4. Set the NUMD values to be greater than the MDTS value provided by the DUT in the Identify Controller Data Structure. Configure the NVMe Host to issue a Get Log Page command specifying each of the Mandatory Log Page Identifiers described in Figure 77 and 78. If MDTS is set to 0 (i.e. unlimited) then this test is not applicable.

Observable Results:
1. Verify that NVMe Controller returns “Invalid Field in Command Error” in response to the received Get Log Page command.

Case 5: Get Error Information after Error (FYI, OF-FYI)
Test Procedure:
1. Configure the NVMe Host to issue a Get Log Page command to LID 01h, Error Information, and record the number of Error log entries.
2. Configure the NVMe Host to issue an Identify Command with a Reserved CNS value.
3. Check that the M bit is set in the Status Field of the completion queue entry associated with the Identify Command. If the M bit is not set to 1, this test is not applicable.
4. Configure the NVMe Host to issue a Get Log Page command to LID 01h, Error Information, and record the number of Error log entries.
5. Configure the NVMe Host to issue an Identify Command with a Reserved CNS value.
6. Check that the M bit is set in the Status Field of the completion queue entry associated with the Identify Command. If the M bit is not set to 1, this test is not applicable.
7. Configure the NVMe Host to issue a Get Log Page command to LID 01h, Error Information, and record the number of Error log entries.

Observable Results:
1. If the M bit is set, verify that NVMe Controller reported an error condition in the Error Information log, and the number of Error Log Entries is incremented by one or more. The reported error condition may or may not be directly related to the Identify Command with Reserved CNS value.

Case 6: SMART Temperature Threshold (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue a Set Feature command to set the Critical Temperature Threshold below the current temperature of the DUT.
2. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h).

Observable Results:
1. Verify that NVMe Controller reported the Critical Temperature warning in the SMART/Health Information Log.

Case 7: Data Units Read (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h). and record the Data Units Read value.
2. Perform 1000 NVMe READ command of 512 bytes.
3. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h). and record the Data Units Read value, which is expected to increase by 1.
4. Perform 1000 NVMe Compare command of 512 bytes.
5. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h). and record the Data Units Read value, which is expected to increase by 1.

Observable Results:
1. Verify that NVMe Controller reported the Data Units Read value that increased by 2 in accord with the NVMe READ and Compare commands that were performed.

Case 8: Data Units Written (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h). and record the Data Units Written value.
2. Perform 2000 NVMe Write command of 512 bytes.
3. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h). and record the Data Units Written value, which is expected to increase by 2.
5. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h), and record the Data Units Written value, which is expected to not increase.

Observable Results:
1. Verify that NVMe Controller reported the Data Units Written value that increased by 2 in accord with the NVMe Write Command only, and that the Write Uncorrectable command did not impact the Data Units Written value.

Case 9: Power Cycle Count (IP)

Test Procedure:
1. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h) and record the Power Cycles value.
2. Power Cycle the DUT.
3. Configure the NVMe Host to issue a Get Log Page command to LID 02h, SMART/Health Information (02h) and record the Power Cycles value.

Observable Results:
1. Verify that NVMe Controller reported the Power Cycles value, and that the value incremented properly after performed a power cycle.

Case 10: NUMD Greater than Log Page Conflict (FYI)

Test Procedure:
1. Check the NVMe Specification version supported by DUT using the value reported in the Identify Controller Data Structure VER field (83:80). If the DUT supports v1.2.1 or higher go to step 2. If the DUT supports v1.2a or lower (or VER is set to 0, go to step 3).
2. Set the NUMDU and NUMDL values to be greater than the Log Page Size required for each of the Mandatory Log Page Identifiers described in Figure 77 and 78.
3. Set the NUMD values to be greater than the Log Page Size required for each of the Mandatory Log Page Identifiers described in Figure 77 and 78.

Observable Results:
1. Verify that NVMe Controller sends the requested Log Page, and that the size of the Log Page is defined by NUMD or NUMDU/NUMDL. Verify that valid data exists only between bytes 0 to the Log Page Size. Verify that bytes beyond MDTS up to NUMD or NUMDU/NUMDL are filled with undefined data.

Case 11: Telemetry Host Initiated Valid Offset Create=1 (FYI)

Test Procedure:
1. Check the Bit 3 of the LPA field Identify Controller Data Structure to determine of the DUT supports Telemetry Host-Initiated and Telemetry Controller-Initiated log pages. If Bit 3 is set to 0 this test is not applicable.
2. Configure the NVMe Host to issue a Get Log Page command specifying Telemetry Host-Initiated Log Page to the NVMe Controller with a Log Page Offset Lower value that is a multiple of 512 bytes, and the Create Telemetry Host-Initiated Data bit is set to 1.

Observable Results:
1. Verify that NVMe Controller sends the requested Log Page following the Telemetry Host-Initiated Log Page format defined in Figure 101 of the NVMe specification.

Case 12: Telemetry Host Initiated Valid Offset Create=0 (FYI)

Test Procedure:
1. Check the Bit 3 of the LPA field Identify Controller Data Structure to determine of the DUT supports Telemetry Host-Initiated and Telemetry Controller-Initiated log pages. If Bit 3 is set to 0 this test is not applicable.
2. Configure the NVMe Host to issue a Get Log Page command specifying Telemetry Host-Initiated Log Page to the NVMe Controller with a Log Page Offset Lower value that is a multiple of 512 bytes, and the Create Telemetry Host-Initiated Data bit is set to 1.
3. Configure the NVMe Host to issue a Get Log Page command specifying Telemetry Host-Initiated Log Page to the NVMe Controller with a Log Page Offset Lower value that is a multiple of 512 bytes, and the Create Telemetry Host-Initiated Data bit is set to 0.
4. Configure the NVMe Host to issue a Get Log Page command specifying Telemetry Host-Initiated Log Page to the NVMe Controller with a Log Page Offset Lower value that is a multiple of 512 bytes, and the Create Telemetry Host-Initiated Data bit is set to 1.

**Observable Results:**
1. Verify that in steps 2, 3, and 4 the NVMe Controller sends the requested Log Page following the Telemetry Host-Initiated Log Page format defined in Figure 101 of the NVMe specification.
2. Verify that the Log Page delivered by the NVMe Controller in Step 3 was not updated from the Log Page delivered by the Controller in Step 2.

**Case 13: Telemetry Host Initiated Invalid Offset (FYI)**

**Test Procedure:**
1. Check the Bit 3 of the LPA field Identify Controller Data Structure to determine of the DUT supports Telemetry Host-Initiated and Telemetry Controller-Initiated log pages. If Bit 3 is set to 0 this test is not applicable.
2. Configure the NVMe Host to issue a Get Log Page command specifying Telemetry Host-Initiated Log Page to the NVMe Controller with a Log Page Offset Lower value that is not a multiple of 512 bytes.

**Observable Results:**
1. Verify that NVMe Controller responds to the Get Log Page command with an error of Invalid Field in Command.

**Case 14: Telemetry Controller Initiated Valid Offset (FYI)**

**Test Procedure:**
1. Check the Bit 3 of the LPA field Identify Controller Data Structure to determine of the DUT supports Telemetry Host-Initiated and Telemetry Controller-Initiated log pages. If Bit 3 is set to 0 this test is not applicable.
2. Configure the NVMe Host to issue a Get Log Page command specifying Telemetry Controller-Initiated Log Page to the NVMe Controller with a Log Page Offset Lower value that is a multiple of 512 bytes.

**Observable Results:**
1. Verify that NVMe Controller sends the requested Log Page following the Telemetry Controller-Initiated Log Page format defined in Figure 102 of the NVMe specification.

**Case 15: Telemetry Controller Initiated Invalid Offset (FYI)**

**Test Procedure:**
1. Check the Bit 3 of the LPA field Identify Controller Data Structure to determine of the DUT supports Telemetry Host-Initiated and Telemetry Controller-Initiated log pages. If Bit 3 is set to 0 this test is not applicable.
2. Configure the NVMe Host to issue a Get Log Page command specifying Telemetry Controller-Initiated Log Page to the NVMe Controller with a Log Page Offset Lower value that is not a multiple of 512 bytes.
Observable Results:
1. Verify that NVMe Controller responds to the Get Log Page command with an error of Invalid Field in Command.

Possible Problems: None.
Test 1.4 – Create/Delete I/O Submission and Completion Queue Commands (M)

Purpose: To verify that an NVMe Controller can properly create and delete I/O Submission and Completion Queues.

References:
[1] NVMe Specification 5.3, 5.4, 5.5, 5.6

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: August 29, 2017

Discussion: The Create I/O Completion Queue command is used to create I/O Completion Queues while the Delete I/O Completion Queue command is used to delete I/O Submission Queues. Likewise, the Create I/O Submission Queue command is used to create I/O Submission Queues while the Delete I/O Submission Queue command is used to delete I/O Submission Queues. Host software shall ensure that any associated I/O Submission Queue is deleted prior to deleting a Completion Queue.

The Create I/O Submission Queue and Create I/O Completion Queue commands use the PRP Entry 1, Command Dword 10, and Command Dword 11 fields. The Delete I/O Submission Queue and Delete I/O Completion Queue commands use the Command Dword 10. All other command specific fields are reserved.

A completion queue entry is posted to the Admin Completion Queue when the specified queue has been created or deleted.

Test Setup: See Appendix A.

Case 1: Basic Operation (M)

Test Procedure:
1. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller.
2. Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller.
3. Configure the NVMe Host to issue 10 Read commands assigned to the queues created in steps 1 and 2 to the controller.
4. Configure the NVMe Host to issue a Delete I/O Submission Queue command specifying the Submission Queue ID of the queue created in step 2 to the controller.
5. Configure the NVMe Host to issue a Delete I/O Completion Queue command specifying the Completion Queue ID of the queue created in step 1 to the controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the queues are properly created and deleted by reading the completion queue entries posted for each command issued by the NVMe Host (all statuses should be Success).
3. Verify that all received responses have all Reserved fields set to 0.

Case 2: Create I/O Completion Queue with QID=0h, exceeds Number of Queues reported, Identifier Already in Use (M)

Test Procedure:
1. Configure the NVMe Host to issue a Get Features command for the Feature Identifier 07h, Number of Queues, record the value reported.
2. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller, with QID=0h.
3. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller with QID=greater than the value reported in the Number of Queues field in the Get Feature response. If the DUT supports the maximum possible number of Queues than this test case is not applicable.
4. Configure the NVMe Host to issue 2 Create I/O Completion Queue commands with identical QID. The first command is expected to complete successfully, the second is expected to return an error of Invalid Queue Identifier.

Observable Results:
1. Verify that after the completion of each command, the controller returns an error of Invalid Queue Identifier

Case 3: Delete I/O Completion Queue before deleting Corresponding Submission Queue (M)

Test Procedure:
1. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller.
2. Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller.
3. Configure the NVMe Host to issue 10 Read commands assigned to the queues created in steps 1 and 2 to the controller.
4. Configure the NVMe Host to issue a Delete I/O Completion Queue command specifying the Completion Queue ID of the queue created in step 1 to the controller.
5. Configure the NVMe Host to issue a Delete I/O Submission Queue command specifying the Submission Queue ID of the queue created in step 2 to the controller.
6. Configure the NVMe Host to issue a Delete I/O Completion Queue command specifying the Completion Queue ID of the queue created in step 1 to the controller.

Observable Results:
1. Verify that the Delete I/O Completion Queue command in step 4, caused the controller to returns an error of Invalid Queue Deletion.

Case 4: Create I/O Completion Queue with Invalid Queue Size (M)

Test Procedure:
1. Configure the NVMe Host to read the Capabilities Register CAP.MQES field to obtain the Maximum Queue Size supported by the DUT. Record the value.
2. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller with a QSIZE of 0h.
3. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller with a QSIZE of greater than the Queue size (MQES) supported by the DUT.

Observable Results:
1. Verify that in each case the Create I/O Completion Queue, caused the controller to returns an error of Invalid Queue Size.

Case 5: Create I/O Submission Queue with Invalid Queue Size (M)

Test Procedure:
1. Configure the NVMe Host to read the Capabilities Register CAP.MQES field to obtain the Maximum Queue Size supported by the DUT. Record the value.
2. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller.
3. Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller with a QSIZE of 0h.
4. Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller with a QSIZE of greater than the Queue size (MQES) supported by the DUT.
Observable Results:
1. Verify that in each case the Create I/O Submission Queue, caused the controller to returns an error of Invalid Queue Size.

Case 6: Create I/O Submission Queue Physically Contiguous (M)

Test Procedure:
1. Configure the NVMe Host to read the Capabilities Register CAP.CQR field. If CAP.CQR is set to zero, this test case is not applicable. If CAP.CQR is set to 1, proceed to the next step.
2. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller.
3. Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller with the PC bit set to 0.

Observable Results:
1. Verify that the transmitted Create I/O Submission Queue, caused the controller to returns an error of Invalid Field in Command (See Figure 56 in NVMe Specification).

Case 7: Create I/O Submission Queue Invalid CQID (M)

Test Procedure:
1. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller.
2. Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller with the CQID set to 0h.
3. Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller with the CQID set an invalid value (i.e. not 0h, and also not the CQID of the Completion Queue created step 1, 3h is used is some test implementations).

Observable Results:
1. Verify that the transmitted Create I/O Submission Queue with CQID of 0h, caused the controller to returns an error of 1h - Invalid Queue Identifier (See Figure 56 in NVMe Specification).
2. Verify that the transmitted Create I/O Submission Queue with CQID with an invalid value (3h is used in some test implementations), caused the controller to returns an error of 0h - Completion Queue Invalid (See Figure 56 in NVMe Specification).

Case 8: Create I/O Completion Queue Invalid Interrupt Vector (M)

Test Procedure:
1. Configure the NVMe Host to read the MSICAP.MC.MME field and the MSIXCAP.MXC.TS.
2. Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller with an Interrupt Vector (IV) value greater than the number of messages supported by the DUT as indicated in either MSICAP.MC.MME or MSIXCAP.MXC.TS.

Observable Results:
1. Verify that the transmitted Create I/O Completion Queue, caused the controller to return an error of Invalid Interrupt Vector (See Figure 52 in NVMe Specification).

Case 9: Create I/O Completion Queue Invalid Queue Address Offset (M)

Test Procedure:
1. Configure the NVMe Host to read the CC.MPS register.
   Configure the NVMe Host to issue a Create I/O Completion Queue command to the controller with a first PRP List Entry that is not QWord aligned.

Observable Results:
1. Verify that the transmitted Create I/O Completion Queue, caused the controller to return an error of Invalid PRP Offset.

Case 10: Create I/O Submission Queue Invalid Queue Address Offset (M)

Test Procedure:
1. Configure the NVMe Host to read the CC.MPS register.
   Configure the NVMe Host to issue a Create I/O Submission Queue command to the controller with a first PRP List Entry that is not QWord aligned.

Observable Results:
1. Verify that the transmitted Create I/O Submission Queue, caused the controller to return an error of Invalid PRP Offset.

Possible Problems: None.
Test 1.5 – Abort Command (M)

Purpose: To determine the conditions under which an NVMe system can successfully abort a given command.

References:
[1] NVMe Specification 5.1

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 2, 2016

Discussion: The Abort command is used to abort a specific command previously issued to the Admin Submission Queue or an I/O Submission Queue. Host software may have multiple Abort commands outstanding, subject to the constraints of the Abort Command Limit indicated in the Identify Controller data structure. An abort is a best effort command; the command to abort may have already completed, currently be in execution, or may be deeply queued. It is implementation specific if/when a controller chooses to complete the command when the command to abort is not found. Whether the command was successfully aborted or not is determined by examining bit 0 of command Dword 0 of the completion queue entry for the Abort command. If the command was successfully aborted, then bit 0 of Dword 0 is cleared to ‘0’. If the command was not aborted, then bit 0 of Dword 0 is set to ‘1’. The completion queue entry for the Abort command is only posted to the Admin Completion Queue after the completion queue entry for the command specified in the Abort command has been posted to its corresponding Admin or I/O Completion Queue.

The Abort command uses the Command Dword 10 field. All other command specific fields are reserved.

Since the Abort Command is a best effort command, this test is designed to determine under what conditions a command can successfully be aborted, and is therefore considered an informative test.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to issue 10 Read commands to the controller.
2. Configure the NVMe Host to issue an Abort command to the controller specifying the CID of one of the issued Read commands.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that after the NVMe Controller posts a completion queue entry to the Admin Completion Queue for the Abort command, that a completion queue entry has been posted to the I/O Completion Queue for the Read command specified in the Abort command.
3. Determine whether the requested command was successfully aborted by examining bit 0 of Dword 0 of the completion queue entry for the Abort command. If the command was successfully aborted, verify that the status of the aborted command is Command Abort Requested (07h).
4. Verify that all received responses have all Reserved fields set to 0.

Possible Problems: cannot test ABORT Limit Exceeded execution time limit (there's a chance the 1st ABORT finishes before the last one)
Test 1.6 – Format NVM Command (M, OF-FYI)

**Purpose:** To verify that an NVMe Controller can properly execute the Format NVM command.

**References:**
- [1] NVMe Specification 5.15

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 28, 2017

**Discussion:** The Format NVM command is used to low level format the NVM media. This is used when the host wants to change the LBA data size and/or metadata size. A low level format may destroy all data and metadata associated with all namespaces or only the specific namespace associated with the command. After the Format NVM command successfully completes, the controller shall not return any user data that was previously contained in an affected namespace.

The settings specified in the Format NVM command are reported as part of the Identify Namespace data structure. If the controller supports multiple namespaces, then the host may specify the value of FFFFFFFFh for the namespace in order to apply the format operation to all namespaces accessible by the controller regardless of the value of the Format NVM Attribute field in the Identify Controller data structure.

The Format NVM command uses the Command Dword 10 field. All other command specific fields are reserved.

**Test Setup:** See Appendix A.

**Case 1: Valid LBAF, SES=000b (M, OF-FYI)**

**Test Procedure:**
1. Check the OACS field of the Identify Controller Data structure to determine if the DUT supports the Format NVM command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to an LBA range.
3. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
4. Configure the NVMe Host to issue a Format NVM Command with LBAF Supported by the DUT, SES=000b and FFFFFFFFh for the namespace ID.
5. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
6. Verify that all received responses have all Reserved fields set to 0.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the same data pattern which was written to the NVM in step 1 is read from the NVM in step 3.
3. Verify that the data pattern written in step 1 is not returned by the controller in step 5.

**Case 2: Valid LBAF, SES=001b (M, OF-FYI)**

**Test Procedure:**
1. Check the OACS field of the Identify Controller Data structure to determine if the DUT supports the Format NVM command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to an LBA range.
3. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
4. Configure the NVMe Host to issue a Format NVM Command with an LBAF Supported by the DUT, SES=001b and FFFFFFFFh for the namespace ID.
5. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
6. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the same data pattern which was written to the NVM in step 1 is read from the NVM in step 3.
3. Verify that the data pattern written in step 1 is not returned by the controller in step 5.

Case 3: Valid LBAF, SES=010b (M, OF-FYI)

Test Procedure:
1. Check the OACS field of the Identify Controller Data structure to determine if the DUT supports the Format NVM command. If the command is not supported this test is not applicable.
2. Check Bit 2 of the FNA field of the Identify Controller Data structure to determine if the DUT supports cryptographic erase. If the DUT does not support cryptographic erase this test case is not applicable.
3. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to an LBA range.
4. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
5. Configure the NVMe Host to issue a Format NVM Command with an LBAF Supported by the DUT, SES=010b and FFFFFFFFh for the namespace ID.
6. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
7. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the same data pattern which was written to the NVM in step 1 is read from the NVM in step 3.
3. Verify that the data pattern written in step 1 is not returned by the controller in step 5.

Case 4: Valid LBAF, SES=111b (reserved value) (M, OF-FYI)

Test Procedure:
1. Check the OACS field of the Identify Controller Data structure to determine if the DUT supports the Format NVM command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to an LBA range.
3. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
4. Configure the NVMe Host to issue a Format NVM Command with an LBAF Supported by the DUT, SES=111b and FFFFFFFFh for the namespace ID.
5. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
6. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the same data pattern which was written to the NVM in step 1 is read from the NVM in step 3.
3. Verify that the data pattern written in step 1 is returned by the controller in step 5.
4. Verify that the Format NVM command completes with error status code Invalid Field (02h).

Case 5: Invalid LBAF, SES=000b (M, OF-FYI)

Test Procedure:
1. Check the OACS field of the Identify Controller Data structure to determine if the DUT supports the Format
   NVM command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern
to an LBA range.
3. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which
   was written in step 1.
4. Configure the NVMe Host to issue a Format NVM Command with an invalid LBAF.
5. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which
   was written in step 1.
6. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the ap-
   propriate Completion Queue indicating the status for the command.
2. Verify that the same data pattern which was written to the NVM in step 1 is read from the NVM in step 3.
3. Verify that the data pattern written in step 1 is returned by the controller in step 5.
4. Verify that the Format NVM command completes with error status code Invalid Field (02h).

Case 6: Invalid LBAF, SES=111b (reserved value) (M, OF-FYI)

Test Procedure:
1. Check the OACS field of the Identify Controller Data structure to determine if the DUT supports the Format
   NVM command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern
to an LBA range.
3. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which
   was written in step 1.
4. Configure the NVMe Host to issue a Format NVM Command with an invalid LBAF and SES=111b.
5. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which
   was written in step 1.
6. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the ap-
   propriate Completion Queue indicating the status for the command.
2. Verify that the same data pattern which was written to the NVM in step 1 is read from the NVM in step 3.
3. Verify that the data pattern written in step 1 is returned by the controller in step 5.
4. Verify that the Format NVM command completes with error status code Invalid Field (02h) and not Invalid
   Format (0Ah).

Case 7: Valid LBAF, SES=000b, PI is non-zero (M)

Test Procedure:
1. Check the OACS field of the Identify Controller Data structure to determine if the DUT supports the Format
   NVM command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern
to an LBA range.
3. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which
   was written in step 1.
4. Configure the NVMe Host to issue a Format NVM Command with LBAF Supported by the DUT, SES=000b and FFFFFFFFh for the namespace ID, and PI=001b.
5. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA range which was written in step 1.
6. Verify that all received responses have all Reserved fields set to 0.
7. Repeat for PI=010b and PI=011b.

**Observable Results:**
1. If End to End Data Protection is supported:
   a. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
   b. Verify that the same data pattern which was written to the NVM in step 1 is read from the NVM in step 3.
   c. Verify that the data pattern written in step 1 is not returned by the controller in step 5.
2. If End to End Data Protection is not supported, verify that the command completed with error status code Invalid Field (02h).

**Possible Problems:** This is only Mandatory if the device claims support for the Format NVM command according to the OACS field of the Identify Controller data structure.
Test 1.7 – Asynchronous Events (M, OF)

Purpose: To verify that an NVMe Controller can properly report asynchronous events to the host.

References:

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: August 29, 2017

Discussion: Asynchronous events are used to notify host software of status, error, and health information as these events occur. To enable asynchronous events to be reported by the controller, host software needs to submit one or more Asynchronous Event Request commands to the controller. The controller specifies an event to the host by completing an Asynchronous Event Request command. Host software should expect that the controller may not execute the command immediately; the command should be completed when there is an event to be reported.

Test Setup: See Appendix A.

Case 1: Asynchronous Event Request Command (M)
The Asynchronous Event Request command is submitted by host software to enable the reporting of asynchronous events from the controller. This command has no timeout. The controller posts a completion queue entry for this command when there is an asynchronous event to be reported to the host. If Asynchronous Event Request commands are outstanding when the controller is reset, the commands are aborted.

Host software may submit multiple Asynchronous Event Request commands to reduce event reporting latency. The total number of simultaneously outstanding Asynchronous Event Request commands is limited by the Asynchronous Event Request Limit specified in the Identify Controller data structure.

If the controller needs to report an event and there are no outstanding Asynchronous Event Request commands, the controller should send a single notification of that Asynchronous Event Type when an Asynchronous Event Request command is received. If a Get Log Page command clears the event prior to receiving the Asynchronous Event Request command or if a power off condition occurs, then a notification is not sent.

The following event types are defined in the NVMe Specification:
- Error Event
- SMART / Health Event
- Notice Events
- I/O Command Set Specification (NVM Command Set) Events:
  - Reservation Log Page Available Event
- Vendor Specific Events

All command specific fields are reserved.

Test Procedure:
1. For each event type described above:
   a. Configure the NVMe Host to issue an Asynchronous Event Request command to the NVMe Controller.
   b. Configure the NVMe Host to cause conditions for generating the event for the NVMe Controller as described in the NVMe Specification.

Observable Results:
1. Verify that the NVMe Controller does not post a completion queue entry to the Admin Completion Queue for the Asynchronous Event Request command until after the event is generated.
2. Verify that the completion queue entry for the Asynchronous Event Request command is properly formatted and contains information appropriate for the event in Dword 0 as described in the NVMe Specification.
3. Verify that all received responses have all Reserved fields set to 0.
4. 

**Case 2: Outstanding Commands Aborted after Reset (M, OF)**

If Asynchronous Event Request commands are outstanding when the controller is reset, the commands are aborted.

**Test Procedure:**
1. Configure the NVMe Host to issue an Asynchronous Event Request command to the NVMe Controller.
2. Configure the NVMe Host to initiate a Controller Level Reset for the NVMe Controller.

**Observable Results:**
1. Verify that after the Controller Level Reset is initiated, a completion queue entry is posted by the NVMe Controller to the Admin Completion Queue and the status for the command indicates that the command was aborted.
2. Verify that all received responses have all Reserved fields set to 0.

**Case 3: Clearing Events (IP)**

If the controller needs to report an event and there are no outstanding Asynchronous Event Request commands, the controller should send a single notification of that Asynchronous Event Type when an Asynchronous Event Request command is received. If a Get Log Page command clears the event prior to receiving the Asynchronous Event Request command or if a power off condition occurs, then a notification is not sent.

When the controller posts a completion queue entry for an outstanding Asynchronous Event Request command and thus reports an asynchronous event, subsequent events of that event type are automatically masked by the controller until the host clears that event. An event is cleared by reading the log page associated with that event using the Get Log Page command.

**Test Procedure:**
1. For each event type associated with a log page:
   a. Configure the NVMe Host to cause conditions for generating the event for the NVMe Controller as described in the NVMe Specification.
   b. Configure the NVMe Host to issue a Get Log Page command to the NVMe Controller for the log page associated with the event in order to clear that event.
   c. Configure the NVMe Host to issue an Asynchronous Event Request command to the NVMe Controller.
   d. After a timeout period of 2 seconds, configure the NVMe Host to clear the outstanding Asynchronous Event Request command by initiating a Controller Level Reset for the NVMe Controller.

**Observable Results:**
1. Verify that after the completion of each Get Log Page command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the NVMe Controller does not post a completion queue entry to the Admin Completion Queue for the Asynchronous Event Request command until after the Controller Level Reset and that the status indicates that the command was aborted and contains no information about the event in Dword 0.
3. Verify that all received responses have all Reserved fields set to 0.
Case 4: Masking Events (M, OF-FYI)
The Asynchronous Event Configuration feature controls the events that trigger an asynchronous event notification to the host. This Feature may be used to disable reporting events in the case of a persistent condition. The attributes are indicated in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes specified in Command Dword 11 of the Set Features command are returned in Dword 0 of the completion queue entry for that command.

Test Procedure:
1. For each event which may be disabled with the Asynchronous Event Configuration feature:
   a. Configure the NVMe Host to issue a Set Features command to the NVMe Controller with feature identifier 0Bh (Asynchronous Event Configuration) and formatted to disable the event.
   b. Configure the NVMe Host to issue an Asynchronous Event Request command to the NVMe Controller.
   c. Configure the NVMe Host to cause conditions for generating the event for the NVMe Controller as described in the NVMe Specification.
   d. After a timeout period of 2 seconds, configure the NVMe Host to clear the outstanding Asynchronous Event Request command by initiating a Controller Level Reset for the NVMe Controller.

Observable Results:
1. Verify that after the completion of each Set Features command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the NVMe Controller does not post a completion queue entry to the Admin Completion Queue for the Asynchronous Event Request command until after the Controller Level Reset and that the status indicates that the command was aborted and contains no information about the event in Dword 0.
3. Verify that all received responses have all Reserved fields set to 0.

Possible Problems: Some events are optional as reported by the Optional Asynchronous Events Supported (OAES) field of the Identify Controller data structure or by other means and are therefore only tested if those features are supported.
Test 1.8 – Get Feature Select (M)

**Purpose:** To verify that an NVMe Controller can properly execute a Get Features command with the Select Field set.

**References:**

[1] NVMe Specification 5.9.1

**Resource Requirements:**

Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 9, 2016

**Discussion:**

A Select field set to 000b (i.e., current) returns the current operating attribute value for the Feature Identifier specified. A Select field set to 001b (i.e., default) returns the default attribute value for the Feature Identifier specified. A Select field set to 010b (i.e., saved) returns the last saved attribute value for the Feature Identifier specified (i.e., the last Set Features command completed without error, with the Save bit set to ‘1’ for the Feature Identifier specified.) A Select field set to 011b (i.e., supported capabilities) returns the capabilities supported for this Feature Identifier. The capabilities supported are returned in Dword 0 of the completion entry of the Get Features command.

A completion queue entry is posted to the Admin Completion Queue when the controller has completed returning any attributes associated with the Feature. Depending on the Feature Identifier, Dword 0 of the completion queue entry may contain feature information.

**Test Setup:** See Appendix A.

**Test Procedure:**

1. For each of the features described in Table 2 and Table 3 (see Test 1.2):
   a. Configure the NVMe Host to issue a Get Features command indicating a Select Field of 000b.
   b. Configure the NVMe Host to issue a Get Features command indicating a Select Field of 001b.
   c. Configure the NVMe Host to issue a Set Features command, to specify a new value for each FID. Next, configure the NVMe Host to issue a Get Features command indicating a Select Field of 010b.
   d. Configure the NVMe Host to issue a Get Features command indicating a Select Field of 011b.

**Observable Results:**

1. For Step 1a, verify that the DUT returns the current operating attribute value for the Feature Identifier specified.
2. For Step 1b, verify that the DUT returns the the default attribute value for the Feature Identifier specified.
3. For Step 1c, verify that the DUT returns the last saved attribute value for the Feature Identifier specified. This must match the value assigned in Step 1c.
4. For Step 1d, verify that the DUT returns returns the capabilities supported for this Feature Identifier. The capabilities supported are returned in Dword 0 of the completion entry of the Get Features command.

**Possible Problems:** None.
Test 1.9 – Feature Saved Across Reset (M)

**Purpose:** To verify that an NVMe Controller can properly save a Feature value set by a Host across a reset.

**References:**
[1] NVMe Specification 7.8

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 9, 2016

**Discussion:**
If bit 4 is set to ‘1’ in the Optional NVM Command Support field of the Identify Controller data structure, then for each Feature, there are three settings: default, saveable, and current.

The saveable value is the value that the Feature has after a power on or reset event. The controller may not support a saveable value for a Feature; this is discovered by using the ‘supported capabilities’ value in the Select field in Get Features. If the controller does not support a saveable value for a Feature, then the default value is used after a power on or reset event. The current value is the value actively in use by the controller for a Feature after a Set Features command completes.

This test is only applicable to devices which set the Save field (Bit 4) of the ONCS field to 1.

**Test Setup:** See Appendix A.

**Test Procedure:**

1. Check bit 4 of the ONCS field. If bit 4 is set to 1, proceed to the next step. If not the test cannot be performed.
2. For each of the features described in Table 2 and Table 3 (see Test 1.2):
   a. Configure the NVMe Host to issue a Get Features command indicating a Select Field of 000b, to obtain the current operating value of the Feature.
   b. Configure the NVMe Host to issue a Set Features command, to specify a new value for each FID.
   c. Configure the NVMe Host to issue a Get Features command indicating a Select Field of 000b, to obtain the current operating value of the Feature.
   d. Perform an NVMe Subsystem Reset (NSSR).
   e. Configure the NVMe Host to issue a Get Features command indicating a Select Field of 000b, to obtain the current operating value of the Feature.

**Observable Results:**
1. For each Feature tested, verify that the value reported in Step 2e, matches the value set by the Host in Step 2b, prior to the reset.

**Possible Problems:** Not all devices will support NSSR, and other reset methods may be necessary.
Test 1.10 – Device Self-test Short Operation (FYI, OF-FYI)

Purpose: To verify that an NVMe Controller can properly perform a Device Self-test Short Operation.

References:
[1] NVMe Specification 5.8

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: December 14, 2017

Discussion: The Device Self-test command is used to start a device self-test operation or abort a device self-test Operation. The device self-test operation is performed by the controller that the Device Self-test command was submitted to.

Test Setup: See Appendix A.

Case 1: Namespace Test Action = 00000000h, STC=1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Device Self-test command with Namespace Test Action set to 00000000h and STC set to 1h (Short device self-test operation).
4. Before the Device Self-test operation completes, send a Get Log Page command to LID 06h (Device Self-test).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.
2. Verify that the Device Self-test command completes successfully.
3. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
4. Verify that all received responses have all Reserved fields set to 0.

Case 2: Namespace Test Action = 00000001h-FFFFFFFEh, STC=1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to all value between 00000001h and FFFFFFFEh that represent a valid Namespace on the DUT, with STC set to 1h (Short device self-test operation).
4. Before each Device Self-test operation completes, send a Get Log Page command to LID 06h (Device Self-test).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.
2. Verify that the Device Self-test command completes successfully.
3. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
4. Verify that all received responses have all Reserved fields set to 0.

Case 3: Namespace Test Action = FFFFFFFH, STC=1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to FFFFFFFH, with STC set to 1h (Short device self-test operation).
4. Before the Device Self-test operation completes, send a Get Log Page command to LID 06h (Device Self-test).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.
2. Verify that the Device Self-test command completes successfully.
3. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
4. Verify that all received responses have all Reserved fields set to 0.

Case 4: Namespace Test Action = Invalid Namespace, STC=1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to an Invalid Namespace, with STC set to 1h (Short device self-test operation).
4. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

Observable Results:
1. Verify that the Device Self-test command returns status Invalid Field in Command.
2. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.

Case 5: Namespace Test Action = Inactive Namespace, STC=1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to an Inactive Namespace, with STC set to 1h (Short device self-test operation).
4. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

Observable Results:
1. Verify that the Device Self-test command returns status Invalid Field in Command.
2. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.

Case 6: Test in Progress, Namespace Test Action = 00000000h, STC=1h and 1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Device Self-test command with Namespace Test Action set to 00000000h and STC set to 1h (Short device self-test operation).
4. Before the first Device Self-test operation completes, send a second Device Self-test command with Namespace Test Action set to 00000000h and STC set to 1h (Short device self-test operation).
5. Once a command completion is received for the first Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.
2. Verify that the first Device Self-test command completes successfully.
3. Verify that the second Device Self-test command completes with status “Device Self-test in Progress”.
4. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
5. Verify that all received responses have all Reserved fields set to 0.

Case 7: Test in Progress, Namespace Test Action = 00000001h-FFFFFFFEh, STC=1h and 1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a value between 00000001h and FFFFFFFEh that represent a valid Namespace on the DUT, with STC set to 1h (Short device self-test operation).

4. Before the first Device Self-test operation completes, send a second Device Self-test command with Namespace Test Action set to the same value as in the previous step, and STC set to 1h (Short device self-test operation).

5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

**Observable Results:**

1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.

2. Verify that the first Device Self-test command completes successfully.

3. Verify that the second Device Self-test command completes with status “Device Self-test in Progress”.

4. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.

5. Verify that all received responses have all Reserved fields set to 0.

**Case 8: Test in Progress, Namespace Test Action = FFFFFFFFh, STC=1h (FYI, OF-FYI)**

**Test Procedure:**

1. Ensure that no Device Self-test operation is currently in progress.

2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.

3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to FFFFFFFFh, with STC set to 1h (Short device self-test operation).

4. Before the first Device Self-test operation completes, send a second Device Self-test command with Namespace Test Action set to the same value as in the previous step, and STC set to 1h (Short device self-test operation).

5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

**Observable Results:**

1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.

2. Verify that the first Device Self-test command completes successfully.

3. Verify that the second Device Self-test command completes with status “Device Self-test in Progress”.

4. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.

5. Verify that all received responses have all Reserved fields set to 0.

**Possible Problems:** None known.
Test 1.11 – Device Self-test Extended Operation (FYI, OF-FYI)

**Purpose:** To verify that an NVMe Controller can properly perform a Device Self-test Extended Operation.

**References:**
[1] NVMe Specification 5.8

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** December 14, 2017

**Discussion:** The Device Self-test command is used to start a device self-test operation or abort a device self-test Operation. The device self-test operation is performed by the controller that the Device Self-test command was submitted to.

**Test Setup:** See Appendix A.

**Case 1: Namespace Test Action = 00000000h, STC=2h (FYI, OF-FYI)**

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Device Self-test command with Namespace Test Action set to 00000000h and STC set to 2h (Extended device self-test operation).
4. Before the Device Self-test operation completes, send a Get Log Page command to LID 06h (Device Self-test).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

**Observable Results:**
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 2h when the operation was processing.
2. Verify that the Device Self-test command completes successfully.
3. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
4. Verify that all received responses have all Reserved fields set to 0.

**Case 2: Namespace Test Action = 0000001h-FFFFFFFFEh, STC=2h (FYI, OF-FYI)**

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to all value between 0000001h and FFFFFFFEh that represent a valid Namespace on the DUT, with STC set to 2h (Extended device self-test operation).
4. Before each Device Self-test operation completes, send a Get Log Page command to LID 06h (Device Self-test).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 2h when the operation was processing.
2. Verify that the Device Self-test command completes successfully.
3. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
4. Verify that all received responses have all Reserved fields set to 0.

Case 3: Namespace Test Action = FFFFFFFFh, STC=2h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to FFFFFFFFh, with STC set to 2h (Extended device self-test operation).
4. Before the Device Self-test operation completes, send a Get Log Page command to LID 06h (Device Self-test).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 2h when the operation was processing.
2. Verify that the Device Self-test command completes successfully.
3. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
4. Verify that all received responses have all Reserved fields set to 0.

Case 4: Namespace Test Action = Invalid Namespace, STC=2h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to an Invalid Namespace, with STC set to 2h (Short device self-test operation).
4. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

Observable Results:
1. Verify that the Device Self-test command returns status Invalid Field in Command.
2. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.

Case 5: Namespace Test Action = Inactive Namespace, STC=2h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to an Inactive Namespace, with STC set to 2h (Extended device self-test operation).
4. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

Observable Results:
1. Verify that the Device Self-test command returns status Invalid Field in Command.
2. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.

Case 6: Test in Progress, Namespace Test Action = 00000000h, STC=2h and 2h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Device Self-test command with Namespace Test Action set to 00000000h and STC set to 2h (Extended device self-test operation).
4. Before the first Device Self-test operation completes, send a second Device Self-test command with Namespace Test Action set to 00000000h and STC set to 2h (Extended device self-test operation).
5. Once a command completion is received for the first Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.
2. Verify that the first Device Self-test command completes successfully.
3. Verify that the second Device Self-test command completes with status “Device Self-test in Progress”.
4. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
5. Verify that all received responses have all Reserved fields set to 0.

Case 7: Test in Progress, Namespace Test Action = 0000001h-FFFFFFFEh, STC=1h and 1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a value between 00000001h and FFFFFFFEh that represent a valid Namespace on the DUT, with STC set to 2h (Extended device self-test operation).
4. Before the first Device Self-test operation completes, send a second Device Self-test command with Namespace Test Action set to the same value as in the previous step, and STC set to 2h (Extended device self-test operation).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.
2. Verify that the first Device Self-test command completes successfully.
3. Verify that the second Device Self-test command completes with status “Device Self-test in Progress”.
4. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
5. Verify that all received responses have all Reserved fields set to 0.

Case 8: Test in Progress, Namespace Test Action = FFFFFFFFh, STC=1h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to FFFFFFFFh, with STC set to 2h (Extended device self-test operation).
4. Before the first Device Self-test operation completes, send a second Device Self-test command with Namespace Test Action set to the same value as in the previous step, and STC set to 2h (Extended device self-test operation).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).
6. Report to the user the time elapsed between sending of the Device Self-test command and its associated completion arriving.

Observable Results:
1. Using the Log Page info returned in response to the first Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 1h when the operation was processing.
2. Verify that the first Device Self-test command completes successfully.
3. Verify that the second Device Self-test command completes with status “Device Self-test in Progress”.
4. Using the Log Page info returned in response to the second Get Log Page command, verify that the NVMe Controller set the Current Device Self-test Status field in the Device Self-test Log to 0h when the operation was completed.
5. Verify that all received responses have all Reserved fields set to 0.

Possible Problems: None known.
**Test 1.12 – Abort Device Self-test Short Operation (FYI, OF-FYI)**

**Purpose:** To verify that an NVMe Controller can properly perform an abort on a Device Self-test Short Operation.

**References:**
[1] NVMe Specification 5.8, 8.11

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** December 14, 2017

**Discussion:** The Device Self-test command is used to start a device self-test operation or abort a device self-test Operation. The device self-test operation is performed by the controller that the Device Self-test command was submitted to.

**Test Setup:** See Appendix A.

**Case 1: Namespace Test Action = 00000000h, STC=1h (FYI, OF-FYI)**

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Get Log Page command to LID 06h (Device Self-test).
4. Before the Device Self-test operation completes, send a Device Self-test command with Namespace Test Action set to 00000000h and STC set to 1h (Short device self-test operation).
5. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

**Observable Results:**
1. Verify that the first Device Self-test command, with STC=1h, completes with status Abort.
2. Verify that the second Device Self-test command, with STC=Fh, completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self Test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

**Case 2: Test Action = 00000001h-FFFFFFFFEh, STC=1h (FYI, OF-FYI)**

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Get Log Page command to LID 06h (Device Self-test).
4. Before the Device Self-test operation completes, send a Device Self-test command with Namespace Test Action set to a value between 00000001h and FFFFFFFEh that represent a valid Namespace on the DUT, with STC set to 1h (Short device self-test operation).
5. Before the Device Self-test operation completes, send a Device Self-test command with Namespace Test Action set the same value as the previous step, and STC set to Fh (Abort device self-test), to the same controller as in the previous test.
6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

**Observable Results:**
1. Verify that the first Device Self-test command, with STC=1h, completes with status Abort.
2. Verify that the second Device Self-test command, with STC=Fh, completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self-test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

**Case 3: Test Action = FFFFFFFh, STC=1h (FYI, OF-FYI)**

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host send a Get Log Page command to LID 06h (Device Self-test).
4. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a value of FFFFFFFh, with STC set to 1h (Short device self-test operation).
5. Before the Device Self-test operation completes, send a Device Self-test command with Namespace Test Action set the same value as the previous step, and STC set to Fh (Abort device self-test), to the same controller as in the previous test.
6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

**Observable Results:**
1. Verify that the first Device Self-test command, with STC=1h, completes with status Abort.
2. Verify that the second Device Self-test command, with STC=Fh, completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self-test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

**Case 4: Aborted by Format NVM Command**

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host send a Get Log Page command to LID 06h (Device Self-test).
4. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a valid Namespace ID value, with STC set to 1h (Short device self-test operation).
5. Before the Device Self-test operation completes, send a Format NVM command with the name Namespace ID as in the previous step.
6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

**Observable Results:**
1. Verify that the first Device Self-test command, with STC=1h, completes with status Abort.
2. Verify that the Format NVM command completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self-test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

Case 5: Aborted by Controller Level Reset

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Get Log Page command to LID 06h (Device Self-test).
4. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a valid Namespace ID value, with STC set to 1h (Short device self-test operation).
5. Configure the NVMe Host to perform a Controller Level Reset.
6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

Observable Results:
1. Verify that the first Device Self-test command, with STC=1h, completes with status Abort.
2. Verify that the Controller Level Reset completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self-test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

Possible Problems: None known.
Test 1.13 – Abort Device Self-test Extended Operation (FYI, OF-FYI)

Purpose: To verify that an NVMe Controller can properly perform an abort on a Device Self-test Extended Operation.

References:
[1] NVMe Specification 5.8, 8.11

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: December 14, 2017

Discussion: The Device Self-test command is used to start a device self-test operation or abort a device self-test Operation. The device self-test operation is performed by the controller that the Device Self-test command was submitted to.

Test Setup: See Appendix A.

Case 1: Namespace Test Action = 00000000h, STC=2h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host send a Get Log Page command to LID 06h (Device Self-test).
4. Configure the NVMe Host to send a Device Self-test command with Namespace Test Action set to 00000000h and STC set to 2h (Extended device self-test operation).
5. Before the Device Self-test operation completes, send a Device Self-test command with Namespace Test Action set to 00000000h and STC set to Fh (Abort device self-test), to the same controller as in the previous test.
6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

Observable Results:
1. Verify that the first Device Self-test command, with STC=2h, completes with status Abort.
2. Verify that the second Device Self-test command, with STC=Fh, completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self Test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

Case 2: Test Action = 00000001h-FFFFFFFEh, STC=22h (FYI, OF-FYI)

Test Procedure:
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host send a Get Log Page command to LID 06h (Device Self-test).
4. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a value between 00000001h and FFFFFFFEh that represent a valid Namespace on the DUT, with STC set to 2h (Extended device self-test operation).
5. Before the Device Self-test operation completes, send a Device Self-test command with Namespace Test Action set the same value as the previous step, and STC set to Fh (Abort device self-test), to the same controller as in the previous test.

6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

**Observable Results:**
1. Verify that the first Device Self-test command, with STC=2h, completes with status Abort.
2. Verify that the second Device Self-test command, with STC=Fh, completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self-test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

**Case 3:** Test Action = FFFFFFFFh, STC=2h (FYI, OF-FYI)

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Get Log Page command to LID 06h (Device Self-test).
4. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a value of FFFFFFFFh, with STC set to 2h (Extended device self-test operation).
5. Before the Device Self-test operation completes, send a Device Self-test command with Namespace Test Action set the same value as the previous step, and STC set to Fh (Abort device self-test), to the same controller as in the previous test.
6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

**Observable Results:**
1. Verify that the first Device Self-test command, with STC=2h, completes with status Abort.
2. Verify that the second Device Self-test command, with STC=Fh, completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self-test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

**Case 4:** Aborted by Format NVM Command

**Test Procedure:**
1. Ensure that no Device Self-test operation is currently in progress.
2. Check Bit 4 of the OACS field in the Identify Controller Data Structure. If Bit 4 is not set to 1, this test is not applicable.
3. Configure the NVMe Host to send a Get Log Page command to LID 06h (Device Self-test).
4. Configure the NVMe Host to send Device Self-test commands with Namespace Test Action set to a valid Namespace ID value, with STC set to 2h (Extended device self-test operation).
5. Before the Device Self-test operation completes, send a Format NVM command with the name Namespace ID as in the previous step.
6. Once a command completion is received for the Device Self-test command, send a Get Log Page command to LID 06h (Device Self-test).

**Observable Results:**
1. Verify that the first Device Self-test command, with STC=1h, completes with status Abort.
2. Verify that the Format NVM command completes successfully.
3. Compare the Device Self Test Log received in steps 3 and 6 and verify that that the second received Device Self Test Log contains a new log entry in the Newest Self-test Results Data Structure in the Device Self-test Log.
4. Verify that the second received Device Self-test Log has the Current Device Self-test Status field set to 0h.
5. Verify that all received responses have all Reserved fields set to 0.

Possible Problems: None known.
Test 1.14 – NVMe-MI Send/Receive (FYI, OF-FYI)

Purpose: To verify that an NVMe Controller can properly perform an NVMe-MI Send and Receive operation.

References:
[1] NVMe Specification 5.17, 5.18

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: February 5, 2018

Discussion: The NVMe-MI Send command is used to transfer an NVMe-MI Request Message to the controller.

NVMe-MI Receive command transfers an NVMe-MI Response Message from the controller to the host that corresponds to an NVMe-MI Request Message that was previously submitted to the controller.

Refer to the NVM Express Management Interface (NVMe-MI) specification for the format and servicing of the NVMe-MI Request and Response Messages.

Test Setup: See Appendix A.

Case 1: Request and Response  (FYI, OF-FYI)

Test Procedure:
1. Check Bit 6 of the OACS field in the Identify Controller Data Structure. If Bit 6 is not set to 1, this test is not applicable.
2. Configure the Testing Station to issue an NVMe-MI Send Command containing a pointer to a properly formatted NVMe-MI Request for Read NVMe-MI Data Structure with DTYP = 00h – NVM Subsystem Information.
3. Configure the Testing Station to issue an NVMe-MI Receive Command to receive the NVMe-MI Response associated with the NVMe-MI Request in the previous step.

Observable Results:
1. Verify that for both the NVMe-MI Send and Receive commands that a command completion queue entry is posted to the Admin Completion Queue.
2. Verify that the Controller sent a properly formatted NVMe-MI Response to the NVMe-MI Request for Read NVMe-MI Data Structure with DTYP = 00h – NVM Subsystem Information, with a properly formatted NVM Subsystem Information data structure.

Possible Problems: None known.
Group 2: NVM Command Set

Overview:

This section describes a method for performing conformance verification for NVMe products implementing the NVM Command Set.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 2.1 – Compare Command (M, OF-FYI)

**Purpose:** To verify that an NVMe Controller can properly execute the Compare command.

**References:**

[1] NVMe Specification 6.6

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 28, 2017

**Discussion:** The Compare command reads the logical blocks specified by the command from the medium and compares the data read to a comparison data buffer transferred as part of the command. If the data read from the controller and the comparison data buffer are equivalent with no miscompares, then the command completes successfully. If there is any miscompare, the command completes with an error of Compare Failure. If metadata is provided, then a comparison is also performed for the metadata.

The command uses Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 14, and Command Dword 15. If the command uses PRPs for the data transfer, then the Metadata Pointer, PRP Entry 1, and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the Metadata SGL Segment Pointer and SGL Entry 1 fields are used. All other command specific fields are reserved.

**Test Setup:** See Appendix A.

**Case 1: Valid SLBA (M, OF-FYI)**

**Test Procedure:**

1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports the Compare command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known sequence to the LBA 0000h.
3. Configure the NVMe Host to issue a Compare command comparing the known sequence to the LBA 0000h written to in Step 1.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the Compare command completes successfully.

**Case 2: SLBA Out of Range (M, OF-FYI)**

**Test Procedure:**

1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports the Compare command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known sequence to the LBA 0000h.
3. Configure the NVMe Host to issue a Compare command to an SLBA which is out of range of the DUT, comparing the known sequence to the LBA 0000h written to in Step 1.

**Observable Results:**

1. Verify that the Compare command completes with status code LBA Out of Range (80h).

**Case 3: SLBA In Range, NLB Goes out of range (M, OF-FYI)**

**Test Procedure:**
1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports the Compare command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known sequence to the LBA 0000h.
3. Configure the NVMe Host to issue a Compare command to the controller to an SLBA which is in range of the DUT, but an NLB value that will push the Compare Command past the size of the namespace, comparing the known sequence to the LBA 0000h written to in Step 1.

Observable Results:
1. Verify that the Compare command completes with status code LBA Out of Range (80h).

Case 4: SLBA Out of Range, NLB > MDTS (M, OF-FYI)

Test Procedure:
1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports the Compare command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known sequence to the LBA 0000h.
3. Configure the NVMe Host to issue a Compare command to the controller comparing the known sequence to the LBA 0000h written to in Step 1, to an SLBA which out of range of the DUT, and an NLB which is greater than MDTS. If MDTS is set to zero (unlimited), then this test case is not applicable.

Observable Results:
1. Verify that the Compare command completes with an error status code. The DUT can report any error status code.

Case 5: SLBA Out of Range, but Lower Dword = 00000000 (M, OF-FYI)

Test Procedure:
1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports the Compare command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known sequence to the LBA 0000h.
3. Configure the NVMe Host to issue a Compare command to the controller comparing the known sequence to the LBA 0000h written to in Step 1, with an SLBA of FFFFFFFF00000000h, which, when read as a 64 bit value is out of range of the DUT, and an NLB which is less than MDTS.

Observable Results:
1. Verify that the Compare command completes with status code LBA Out of Range (80h).

Case 6: Invalid Namespace ID (M, OF-FYI)

Test Procedure:
1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports the Compare command. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller in order to write a known sequence to the LBA 0000h.
3. Configure the NVMe Host to issue a Compare command to the controller comparing the known sequence to the LBA 0000h written to in Step 1, specifying an Invalid NSID outside of the controller specified range defined by NN (Number of Namespaces). If NN is the maximum possible value (0xFFFFFFFF) this sub test cannot be performed.

Observable Results:
1. Verify that the Compare command completes with status code Invalid Namespace or Format (8Bh).
Possible Problems: None.
Test 2.2 – Dataset Management Command (M, OF-FYI)

**Purpose:** To verify that an NVMe Controller can properly execute the Dataset Management command.

**References:**


**Resource Requirements:**

Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 28, 2017

**Discussion:** The Dataset Management command is used by the host to indicate attributes for ranges of logical blocks. This includes attributes like frequency that data is read or written, access size, and other information that may be used to optimize performance and reliability. This command is advisory; a compliant controller may choose to take no action based on information provided.

The command uses Command Dword 10 and Command Dword 11 fields. If the command uses PRPs for the data transfer, then the PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, the SGL Entry 1 field is used. All other command specific fields are reserved.

The data that the Dataset Management command provides is a list of ranges with context attributes. Each range consists of a starting LBA, a length of logical blocks that the range consists of and the context attributes to be applied to that range. The definition of the Dataset Management command Range field is specified in Table 6. The maximum case of 256 ranges is shown.

**Table 6 – Dataset Management Command Range Definition**

<table>
<thead>
<tr>
<th>Range</th>
<th>Byte</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range 0</td>
<td>03:00</td>
<td>Context Attributes</td>
</tr>
<tr>
<td></td>
<td>07:04</td>
<td>Length in logical blocks</td>
</tr>
<tr>
<td></td>
<td>15:08</td>
<td>Starting LBA</td>
</tr>
<tr>
<td>Range 1</td>
<td>19:16</td>
<td>Context Attributes</td>
</tr>
<tr>
<td></td>
<td>23:20</td>
<td>Length in logical blocks</td>
</tr>
<tr>
<td></td>
<td>31:24</td>
<td>Starting LBA</td>
</tr>
<tr>
<td>…</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Range 255</td>
<td>4083:4080</td>
<td>Context Attributes</td>
</tr>
<tr>
<td></td>
<td>4087:4084</td>
<td>Length in logical blocks</td>
</tr>
<tr>
<td></td>
<td>4095:4088</td>
<td>Starting LBA</td>
</tr>
</tbody>
</table>

**Test Setup:** See Appendix A.

**Case 1: Basic Operation (M, OF-FYI)**

**Test Procedure:**

1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports Dataset Management. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue the Dataset Management command that indicates attributes for ranges of logical blocks.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

**Case 2: Deallocate (M, OF-FYI)**

The Dataset Management command may also be used to deallocate ranges of logical blocks by setting the Attribute – Deallocate (AD) field of Command Dword 11 to ‘1’. When the controller receives a Dataset Management command with the AD field set to ‘1’, it may deallocate all provided ranges. If a read occurs to a deallocated range, the controller shall return all zeros, all ones, or the last data written to the associated LBA. If the deallocated or unwritten logical block error is enabled and a read occurs to a deallocated range, then the read shall fail with the Unwritten or Deallocated Logical Block status code.

An LBA that has been deallocated using the Dataset Management command is no longer deallocated when the LBA is written. Read operations do not affect the deallocation status of an LBA. The value returned by subsequent reads of that LBA shall be the same until a write occurs to that LBA.

**Test Procedure:**

1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports Dataset Management. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Write command to write a known data pattern to the controller.
3. Configure the NVMe Host to issue a Dataset Management command with the Attribute – Deallocate (AD) field set to ‘1’ and specifying the same LBA range written to in step 2 to the controller.
4. Configure the NVMe Host to issue a Read command to read the same LBA range written to in step 2.
5. Configure the NVMe Host to issue another Read command to the controller in order to read the same LBA range written to in step 2.
6. Configure the NVMe Host to issue a Write command to write a known data pattern (but different than the data pattern used in step 2) to the controller specifying the same LBA range previously deallocated.
7. Configure the NVMe Host to issue a Read command to the controller in order to read the same LBA range written to in step 6.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the data returned by the controller from the Read command in step 4 is either all zeros, all ones, or the data written to the associated LBA in step 2.
3. Verify that the data returned by the controller from the Read command in step 5 is identical to the data returned by the controller from the Read command in step 4.
4. Verify that the data returned by the controller from the Read command in step 7 matches the data written in step 6.

**Case 3: Deallocate Out of Range (M, OF-FYI)**

**Test Procedure:**

1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports Dataset Management. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Dataset Management command with the Attribute – Deallocate (AD) field set to ‘1’ and specifying an out of Range LBA range value.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the data returned by the controller from the Read command in step 4 is either all zeros, all ones, or the data written to the associated LBA in step 2.
3. Verify that the data returned by the controller from the Read command in step 5 is identical to the data returned by the controller from the Read command in step 4.
4. Verify that the data returned by the controller from the Read command in step 7 matches the data written in step 6.

**Case 4: NR Value is Maximum (M, OF-FYI)**

**Test Procedure:**

1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports Dataset Management. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Dataset Management command with the Attribute – Deallocate (AD) field set to ‘1’ and specifying an out of Range LBA range value.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command, and the Dataset Management command completes with status LBA out of Range (80h).
1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports Dataset Management. If the command is not supported this test is not applicable.
2. Configure the NVMe Host to issue a Dataset Management command with the Number of Ranges (NR) field set to all ‘1’s’.

**Observable Results:**
1. Verify that the command completes successfully.

**Case 5: Correct Range Deallocated (M, OF-FYI)**

**Test Procedure:**
1. Check the ONCS field of the Identify Controller Data structure to determine if the DUT supports Dataset Management. If the command is not supported this test is not applicable.
2. Write a known data pattern (e.g. ‘AAAA’) to three consecutive LBAs.
3. Configure the NVMe Host to issue a Dataset Management command with the Attribute – Deallocate (AD) field set to ‘1’ and specifying the middle LBA of the LBA written in step 1.
4. Perform a READ operation to each of the three LBAs.

**Observable Results:**
1. Verify that the Dataset Management command completes successfully.
2. Verify that the data returned for the READ command to the first and third LBAs is the known data pattern in step 1.
3. Verify that the data returned from the READ operation to the second LBA is either all zeros, all ones, or the known data pattern from step 1.

**Possible Problems:** This test is Mandatory if Supported, according to the ONCS field of the Identify Controller data structure.
Test 2.3 – Read Command (M, OF-FYI)

Purpose: To verify that an NVMe Controller can properly execute the Read command.

References:
[1] NVMe Specification 6.9, 9.4

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: November r 14, 2017

Discussion: The Read command reads data and metadata, if applicable, from the NVM controller for the LBAs indicated. The command may specify protection information to be checked as part of the read operation.

The command uses Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15 fields. If the command uses PRPs for the data transfer, then the Metadata Pointer, PRP Entry 1, and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the Metadata SGL Segment Pointer and SGL Entry 1 fields are used. If supported, this test may be performed using 4k sector sizes.

Regarding the reporting of error status codes, the NVMe specification states: “The status code of the completion queue entry should indicate an Internal Error status code (if multiple error conditions exist, the lowest numerical value is returned).”

Test Setup: See Appendix A.

Case 1: Valid Read, LR=0, FUA=0 (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to one LBA on the NVMe Device.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1, with LR=0, FUA=0.
3. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

Case 2: SLBA Out of Range (M)

Test Procedure:
1. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
2. Configure the NVMe Host to issue a Read command to the controller to an SLBA which is out of range of the DUT.

Observable Results:
1. Verify that the READ command completes with status code LBA Out of Range (80h).

Case 3: SLBA In Range, NLB Goes out of range (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
2. Configure the NVMe Host to issue a Read command to the controller to an SLBA which in range of the DUT, but an NLB value that will push the Read Command past the capacity of the DUT.

Observable Results:
1. Verify that the READ command completes with status code Invalid Field (02h) when the NLB value specifies a value that exceeds MDTS.
2. If NLB is out of range and does not exceed MDTS, verify that the READ command completes with status code LBA Out of Range (0x80).

Case 4: SLBA Out of Range, NLB > MDTS (M, OF-FYI)

Test Procedure:
1. Check the MDTS value reported by the DUT in the Identify Controller Data Structure. If MDTS is set to 0 (i.e. unlimited) then this test is not applicable.
2. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
3. Configure the NVMe Host to issue a Read command to the controller to an SLBA which is out of range of the DUT, and an NLB which is greater than MDTS.

Observable Results:
1. Verify that the READ command completes with status code either Invalid Field (02h) or LBA out of Range (80h).

Case 5: SLBA Out of Range, but Lower Dword = 00000000 (M)

Test Procedure:
1. If an SLBA of FFFFFFFF00000000h is within range of the DUT, then this test is not applicable.
2. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
3. Configure the NVMe Host to issue a Read command to the controller with an SLBA of FFFFFFFF00000000h ,which, when read as a 64 bit value is out of range of the DUT, and an NLB which is less than MDTS.

Observable Results:
1. Verify that the READ command completes with status code LBA Out of Range (80h).

Case 6: Invalid Namespace ID (M, OF-FYI)

Test Procedure:
1. Check the NN Value in the Identify Controller Data Structure. If NN is set to 0xFFFFFFFF, then this test Is not applicable.
2. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
3. Configure the NVMe Host to issue a Read command to the controller to the LBA 0000h.
4. Configure the NVMe Host to issue a READ command to the NVMe Controller specifying an Invalid NSID outside of the controller specified range defined by NN (Number of Namespaces).

Observable Results:
1. Verify that the READ command completes with status code Invalid Namespace or Format (0Bh).

Case 7: Invalid Namespace ID and SLBA Out of Range (M, OF-FYI)

Test Procedure:
1. Check the NN field in the Identify Controller Data Structure. If NN is the maximum possible value (0xFFFFFFFF) this sub test cannot be performed.
2. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
3. Configure the NVMe Host to issue a Read command to the LBA 0000h.
4. Configure the NVMe Host to issue a Read command to an invalid Namespace ID with an SLBA value that is beyond the capacity of the DUT. The READ command to the NVMe Controller specifying an Invalid NSID outside of the controller specified range defined by NN (Number of Namespaces).

Observable Results:
1. Verify that the READ command completes with status code of either Invalid Namespace or Format (0Bh), or LBA Out of Range (80h).

Case 8: Valid Read, LR=0, FUA=1 (M, OF-FYI)
Test Procedure:
1. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to one LBA on the NVMe Device.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1, with LR=0, FUA=1.
3. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

Case 9: Valid Read, LR=1, FUA=0 (M, OF-FYI)
Test Procedure:
1. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to one LBA on the NVMe Device.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1, with LR=1, FUA=0.
3. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

Case 10: Valid Read, LR=1, FUA=1 (M, OF-FYI)
Test Procedure:
1. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to one LBA on the NVMe Device.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1, with LR=1, FUA=1.
3. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

Case 11: Valid READ, Invalid PRP Address Offset (M)
Test Procedure:
1. Configure the NVMe Host to read the CC.MPS register.
2. Configure the NVMe Host to issue a READ command to the controller with a first PRP List Entry that is not QWord aligned.

**Observable Results:**
1. Verify that the transmitted READ command, caused the controller to return an error of “PRP Offset Invalid”.

**Possible Problems:** None.
Test 2.4 – Write Command (M, OF-FYI)

Purpose: To verify that an NVMe Controller can properly execute the Write command.

References:

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: November 14, 2017

Discussion: The Write command writes data and metadata, if applicable, to the NVM controller for the logical blocks indicated. The host may also specify protection information to include as part of the operation.

The command uses Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15 fields. If the command uses PRPs for the data transfer, then the Metadata Pointer, PRP Entry 1, and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the Metadata SGL Segment Pointer and SGL Entry 1 fields are used. If supported, this test may be performed using 4k sector sizes.

Regarding the reporting of error status codes, the NVMe specification states: “The status code of the completion queue entry should indicate an Internal Error status code (if multiple error conditions exist, the lowest numerical value is returned).”

Test Setup: See Appendix A.

Case 1: Valid Write, LR=0, FUA=0 (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue a Write command to the controller in order to write a known data pattern to one LBA on the NVMe Device, with LR=0, FUA=0.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1.
3. Verify that all received responses have all Reserved fields set to 0.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

Case 2: SLBA Out of Range (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
2. Configure the NVMe Host to issue a Write command with a known data pattern to an SLBA which is out of range of the DUT.

Observable Results:
1. Verify that the Write command completes with status code LBA Out of Range (80h).

Case 3: SLBA In Range, NLB Goes out of range (M, OF-FYI)

Test Procedure:
1. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.

2. Configure the NVMe Host to issue a Write command with a known data pattern to an SLBA which in range of the DUT, but an NLB value that will push the Write Command past the capacity of the DUT.

**Observable Results:**

1. Verify that the WRITE command completes with status code Invalid Field (02h) when the NLB value specifies a value that exceeds MDTS.

2. If NLB is out of range and does not exceed MDTS, verify that the WRITE command completes with status code LBA Out of Range (0x80) or Capacity Exceeded (0x81).

3. **Case 4: SLBA Out of Range, NLB > MDTS (M, OF-FYI)**

   **Test Procedure:**
   1. Check the MDTS value reported by the DUT in the Identify Controller Data Structure. If MDTS is set to 0 (i.e. unlimited) then this test is not applicable.

   2. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.

   3. Configure the NVMe Host to issue a Write command with a known data pattern to an SLBA which is out of range of the DUT, and an NLB which is greater than MDTS.

   **Observable Results:**

   1. Verify that the Write command completes with status code LBA Out of Range (80h) or Capacity Exceeded (0x81).

4. **Case 5: SLBA Out of Range, but Lower Dword = 00000000 (M, OF-FYI)**

   **Test Procedure:**
   1. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.

   2. Configure the NVMe Host to issue a Write command with a known data pattern with an SLBA of FFFFFFF00000000h, which, when read as a 64 bit value is out of range of the DUT, and an NLB which is less than MDTS.

   **Observable Results:**

   1. Verify that the Write command completes with status code LBA Out of Range (80h).

5. **Case 6: Invalid Namespace ID (M, OF-FYI)**

   **Test Procedure:**
   1. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.

   2. Configure the NVMe Host to issue a Write command with a known data pattern, to an invalid Namespace ID. The Write command to the NVMe Controller should specify an Invalid NSID outside of the controller specified range defined by NN (Number of Namespaces). If NN is the maximum possible value (0xFFFFFFFF) this sub test cannot be performed.

   **Observable Results:**

   1. Verify that the Write command completes with status code Invalid Namespace or Format (0Bh).

6. **Case 7: Invalid Namespace ID and SLBA Out of Range (M, OF-FYI)**

   **Test Procedure:**
   1. Check the NN field in the Identify Controller Data Structure. If NN is the maximum possible value (0xFFFFFFFF) this sub test cannot be performed.

   2. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.
3. Configure the NVMe Host to issue a Write command with a known data pattern, to an invalid Namespace ID with an SLBA value that is beyond the capacity of the DUT. The Write command to the NVMe Controller should specify an Invalid NSID outside of the controller specified range defined by NN (Number of Namespaces).

**Observable Results:**
1. Verify that the Write command completes with status code of either Invalid Namespace or Format (0Bh), or LBA Out of Range (80h).

**Case 8: Valid Write, LR=0, FUA=1 (M, OF-FYI)**

**Test Procedure:**
1. Configure the NVMe Host to issue a Write command with a known data pattern, to the controller in order to write a known data pattern to one LBA on the NVMe Device, with LR=0, FUA=1.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1.
3. Verify that all received responses have all Reserved fields set to 0.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

**Case 9: Valid Write, LR=1, FUA=0 (M)**

**Test Procedure:**
1. Configure the NVMe Host to issue a Write command with a known data pattern, to the controller in order to write a known data pattern to one LBA on the NVMe Device, with LR=1, FUA=0.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1.
3. Verify that all received responses have all Reserved fields set to 0.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

**Case 10: Valid Write, LR=1, FUA=1 (M, OF-FYI)**

**Test Procedure:**
1. Configure the NVMe Host to issue a Write command with a known data pattern, to the controller in order to write a known data pattern to one LBA on the NVMe Device, with LR=1, FUA=1.
2. Configure the NVMe Host to issue a Read command to the controller in order to read from the same LBA which was written to in step 1.
3. Verify that all received responses have all Reserved fields set to 0.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the known data pattern was read correctly from the NVMe Device exactly as it was written.

**Case 11: Write with Invalid PRP Address Offset (M)**

**Test Procedure:**
1. Configure the NVMe Host to read the CC.MPS register.
2. Configure the NVMe Host to issue a Write command to the controller with a first PRP List Entry that is not QWord aligned.
Observable Results:
1. Verify that the transmitted Write command, caused the controller to return an error of “PRP Offset Invalid”.

Possible Problems: None.
Test 2.5 – Write Uncorrectable Command (M, OF)

Purpose: To verify that an NVMe Controller can properly execute the Write Uncorrectable command.

References:
[1] NVMe Specification 6.15

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: August 29, 2017

Discussion: The Write Uncorrectable command is used to mark a range of logical blocks as invalid. When the specified logical block(s) are read after this operation, a failure is returned with Unrecovered Read Error status. To clear the invalid logical block status, a write operation is performed for those logical blocks.

The fields used are Command Dword 10, Command Dword 11, and Command Dword 12 fields. All other command specific fields are reserved.

Test Setup: See Appendix A.

Case 1: SLBA In Range, NLB Valid (M, OF)

Test Procedure:
1. Check the ONCS field to determine if the DUT supports the Write Uncorrectable command. If the DUT does not support the Write Uncorrectable command this test is not applicable.
2. Configure the NVMe Host to issue a Write Uncorrectable command to a particular LBA on the NVMe Device. Both the SLBA and NLB should be valid.
3. Configure the NVMe Host to issue a Read command for the LBA on which the Write Uncorrectable command was performed.
4. Configure the NVMe Host to issue a Write command for the LBA on which the Write Uncorrectable command was performed in order to clear the invalid logical block status.
5. Repeat step 3.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the completion queue entry returned for the first Read command indicates Unrecovered Read Error status.
3. Verify that the completion queue entry returned for the second Read command indicates Success status.

Case 2: SLBA Out of Range, NLB Valid (M, OF)

Test Procedure:
1. Check the ONCS field to determine if the DUT supports the Write Uncorrectable command. If the DUT does not support the Write Uncorrectable command this test is not applicable.
2. Configure the NVMe Host to issue a Write Uncorrectable command to a particular LBA on the NVMe Device. The SLBA should be for a value out of range for the DUT. NLB should be valid.
3. Configure the NVMe Host to issue a Read command for the LBA on which the Write Uncorrectable command was performed.

Observable Results:
1. Verify that the Write Uncorrectable Command returns status code LBA Out of Range 80h.
2. Verify that the completion queue entry returned for the first Read command indicates Status Code LBA out of Range and does not return status code Unrecovered READ error.
Case 3: SLBA Out of Range, NSID Invalid (M, OF)

Test Procedure:
1. Check the ONCS field to determine if the DUT supports the Write Uncorrectable command. If the DUT does not support the Write Uncorrectable command this test is not applicable.
2. Check the NN value reported by the DUT in the Identify Controller Data Structure. If NN is the maximum possible value (0xFFFFFFFF) this sub test cannot be performed.
3. Configure the NVMe Host to issue a Write Uncorrectable command to a particular LBA on the NVMe Device. The SLBA should be for a value out of range for the DUT, and the NSID should be invalid. The Write Uncorrectable command to the NVMe Controller should specify an Invalid NSID outside of the controller specified range defined by NN (Number of Namespaces).
4. Configure the NVMe Host to issue a Read command for the LBA on which the Write Uncorrectable command was performed.

Observable Results:
1. Verify that the Write Uncorrectable command completes with status code Invalid Namespace or Format (0Bh) and not LBA Out of Range (80h).
2. Verify that the completion queue entry returned for the first Read command indicates Status Code Invalid Namespace or Format and does not return status code Unrecovered READ error.

Case 4: SLBA Out of Range, but Lower Dword = 00000000 (M, OF)

Test Procedure:
1. Check the ONCS field to determine if the DUT supports the Write Uncorrectable command. If the DUT does not support the Write Uncorrectable command this test is not applicable.
2. Configure the NVMe Host to issue a Write Uncorrectable command to a particular LBA on the NVMe Device. The SLBA should be FFFFFFFF00000000h, which, when read as a 64 bit value is out of range of the DUT, and an NLB which is less than MDTS.
3. Configure the NVMe Host to issue a Read command for the LBA on which the Write Uncorrectable command was performed.

Observable Results:
1. Verify that the Write Uncorrectable command completes with status code LBA Out of Range (80h).
2. Verify that the completion queue entry returned for the first Read command indicates Status Code LBA Out of Range and does not return status code Unrecovered READ error.

Case 5: NLB greater than MDTS (M, OF)

Test Procedure:
1. Check the ONCS field to determine if the DUT supports the Write Uncorrectable command. If the DUT does not support the Write Uncorrectable command this test is not applicable.
2. Check the MDTS value reported by the DUT in the Identify Controller Data Structure. If MDTS is set to 0 (unlimited) then this test case is not applicable.
3. Configure the NVMe Host to issue a Write Uncorrectable command to a particular LBA on the NVMe Device. NLB should be greater than MDTS.
4. Configure the NVMe Host to issue Read commands for the LBAs on which the Write Uncorrectable command was performed. Ensure that the NVMe Host issues Read commands to all LBAs affected by the Write Uncorrectable command.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status of Successful for the Write Uncorrectable command. The DUT is expected to ignore the NLB/MDTS conflict since MDTS does not affect the Write Uncorrectable command.
2. Verify that the completion queue entry returned for the Read commands indicate Unrecovered READ Error status.
Possible Problems:

Case 5 is updated per ECN 003 of NVMe Specification v1.2.1. This ECN alters behavior expected in earlier versions.
Test 2.6 – Flush Command (M, OF)

Purpose: To verify that an NVMe Controller can properly execute the Flush command.

References:
[1] NVMe Specification 6.8

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: July 7, 2016

Discussion: The Flush command shall commit data and metadata associated with the specified namespace(s) to non-volatile media. The flush applies to all commands completed prior to the submission of the Flush command. The controller may also flush additional data and/or metadata from any namespace.

All command specific fields are reserved.

Test Setup: See Appendix A.

Case 1: Valid Namespace ID (M, OF-FYI)

Test Procedure:
1. For each active namespace, configure the NVMe Host to issue a Flush command to the NVMe Controller specifying the NSID of the specified namespace.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. If the VWC field Bit 0 of the Identify Controller data structure is cleared to 0, verify that the completion queue entry for each Flush command indicate success.
3. Verify that all received responses have all Reserved fields set to 0.

Case 2: Invalid Namespace ID (M, OF)

Test Procedure:
5. Configure the NVMe Host to issue a Flush command to the NVMe Controller specifying an Invalid NSID outside of the controller specified range defined by NN (Number of Namespaces). If NN is the maximum possible value (0xFFFFFFFF) this sub test cannot be performed.

Observable Results:
1. Verify that the Flush command completes with status code Invalid Namespace or Format (0Bh).

Possible Problems: None.
Test 2.7 – Write Zeroes Command (M, OF-FYI)

**Purpose:** To verify that an NVMe Controller can properly execute the Write Zeroes command.

**References:**
[1] NVMe Specification 6.16

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 28, 2017

**Discussion:** The Write Zeroes command is used to set a range of logical blocks to zero. After successful completion of this command, the value returned by subsequent reads of logical blocks in this range shall be zeroes until a write occurs to this LBA range. The metadata for this command shall be all zeroes and the protection information is updated based on CDW12 PRINFO.

The fields used are Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 14, and Command Dword 15 fields.

**Test Setup:** See Appendix A.

**Case 1: SLBA In Range, NLB Valid, LR=0, FUA=0 (M, OF-FYI)**

**Test Procedure:**
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not supported then this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller specifying a particular LBA on the NVMe Device. The written data should be either all 1’s, or an alternating pattern of 1’s and 0’s.
3. Configure the NVMe Host to issue a Write Zeroes command to the controller specifying the same LBA on the NVMe Device which was previously written to.
4. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA for which the Write Zeroes command was performed.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the data returned by the controller for the Read command after the Write Zeroes command returns data of zeroes only.

**Case 2: SLBA Out of Range, NLB Valid (M, OF-FYI)**

**Test Procedure:**
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not supported then this test is not applicable.
2. Configure the NVMe Host to issue a Write Zeroes command to the controller specifying SLBA which is out of range for the DUT.

**Observable Results:**
1. Verify that the Write Zeroes Command returns status code LBA Out of Range 80h.

**Case 3: SLBA Out of Range, NSID Invalid (M, OF-FYI)**

**Test Procedure:**
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not supported then this test is not applicable.
2. Check the NN value reported by the DUT in the Identify Controller Data Structure. If NN is the maximum possible value (0xFFFFFFFF) this sub test cannot be performed.
3. Configure the NVMe Host to issue a Write Zeroes command to the controller specifying SLBA which is out of range for the DUT, and an invalid NSID. The Write Zeroes command to the NVMe Controller should specify an Invalid NSID outside of the controller-specified range defined by NN (Number of Namespaces).

Observable Results:
1. Verify that the Write Zeroes command completes with status code or either Invalid Namespace or Format (0Bh or LBA Out of Range (80h)).

Case 4: SLBA Out of Range, but Lower Dword = 00000000 (M, OF-FYI)
Test Procedure:
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not support then this test is not applicable.
2. Configure the NVMe Host to issue a Write Zeroes command to a particular LBA on the NVMe Device. The SLBA should be FFFFFFFF00000000h, which, when read as a 64 bit value is out of range of the DUT, and an NLB which is less than MDTS.

Observable Results:
1. Verify that the Write Zeroes command completes with status code LBA Out of Range (80h).

Case 5: NLB greater than MDTS (M, OF-FYI)
Test Procedure:
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not support then this test is not applicable.
2. Check the MDTS value reported in the Identify Controller Data Structure. If MDTS is set to 0 (unlimited) then this test case is not applicable.
3. Configure the NVMe Host to issue a Write command to the controller specifying a particular LBA on the NVMe Device. The written data should be either all 1’s, or an alternating pattern of 1’s and 0’s.
4. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA for which the previous Write command was performed.
5. Configure the NVMe Host to issue a Write Zeroes command the same LBA on the NVMe Device as was written in Step 1. NLB should be greater than MDTS.
6. Configure the NVMe Host to issue Read commands to the controller specifying the same LBAs for which the Write Zeroes command was performed. Ensure that the NVMe Host issues Read commands to all LBAs affected by the Write Zeroes command.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command which should be ‘Successful’.
2. Verify that the data returned by the controller for the Read command after the Write command returns the data written in Step 1.
3. Verify that the data returned by the controller for the Read commands after the Write Zeroes command returns all 0’s.

Case 6: SLBA In Range, NLB Valid, LR=0, FUA=1 (M, OF-FYI)
Test Procedure:
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not support then this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller specifying a particular LBA on the NVMe Device. The written data should be either all 1’s, or an alternating pattern of 1’s and 0’s.
3. Configure the NVMe Host to issue a Write Zeroes command to the controller specifying the same LBA on the NVMe Device which was previously written to.
4. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA for which the Write Zeroes command was performed.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the data returned by the controller for the Read command after the Write Zeroes command returns data of zeroes only.

Case 7: SLBA In Range, NLB Valid, LR=1, FUA=0 (M, OF-FYI)
Test Procedure:
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not supported then this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller specifying a particular LBA on the NVMe Device. The written data should be either all 1’s, or an alternating pattern of 1’s and 0’s.
3. Configure the NVMe Host to issue a Write Zeroes command to the controller specifying the same LBA on the NVMe Device which was previously written to.
4. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA for which the Write Zeroes command was performed.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the data returned by the controller for the Read command after the Write Zeroes command returns data of zeroes only.

Case 8: SLBA In Range, NLB Valid, LR=1, FUA=1 (M, OF-FYI)
Test Procedure:
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not supported then this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller specifying a particular LBA on the NVMe Device. The written data should be either all 1’s, or an alternating pattern of 1’s and 0’s.
3. Configure the NVMe Host to issue a Write Zeroes command to the controller specifying the same LBA on the NVMe Device which was previously written to.
4. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA for which the Write Zeroes command was performed.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. Verify that the data returned by the controller for the Read command after the Write Zeroes command returns data of zeroes only.

Case 9: PRCHK is Non Zero (M, OF-FYI)
Test Procedure:
1. Check the ONCS field of the Identify Controller Data Structure. If the Write Zeroes Command is not supported then this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller specifying a particular LBA on the NVMe Device. The written data should be either all 1’s, or an alternating pattern of 1’s and 0’s.
3. Configure the NVMe Host to issue a Write Zeroes command to the controller specifying the same LBA on the NVMe Device which was previously written to, but the PRCHK value within the PRINFO field is non-zero.
4. Configure the NVMe Host to issue a Read command to the controller specifying the same LBA for which the Write Zeroes command was performed.
Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command, and that the Write Zeroes command completes with Status 02h, Invalid Field.
2. Verify that the data returned by the controller for the Read command after the Write Zeroes command returns the data pattern written in step 1.

Possible Problems: Case 5 is updated per ECN 003 of NVMe Specification v1.2.1. This ECN alters behavior expected in earlier versions.
Test 2.8 – Atomicity Parameters (M, OF)

**Purpose:** To verify that an NVMe Controller properly sets the Atomicity Parameters.

**References:**
1. NVMe Specification 6.4

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 28, 2017

**Discussion:** The NVMe specification sets certain restrictions on the Atomicity Parameters relative to one another, as reported in the Identify Controller and Identify Namespace data structures. This test seeks to ensure that those restrictions are followed. These restrictions apply to the AWUN, AWUPF, ACWU, NAWUN, NAWUPF, NACWU, NABSN, NABO, NABSPF values. Support for Atomic Writes is indicated in the NSFEAT and NAWUN fields. If the DUT does not support Atomic Writes this test is not applicable and does not need to be performed.

**Test Setup:** See Appendix A.

**Test Procedure:**
1. For each namespace in the NVM subsystem, configure the NVMe Host to issue an Identify command specifying CNS value 00h to the controller in order to receive back an Identify Namespace data structure for the specified namespace.
2. Configure the NVMe Host to issue an Identify command specifying CNS value 01h to the controller in order to receive back an Identify Controller data structure.
3. Parse the received data structures for the AWUN, AWUPF, ACWU, NAWUN, NAWUPF, NACWU, NABSN, NABO, NABSPF values.

**Observable Results:**
1. Determine if NABSN is set to a non-zero value. If not, this test case is not applicable.
2. Verify the following:
   a. AWUPF ≤ AWUN
   b. NAWUN ≥ AWUN
   c. NAWUPF ≥ AWUPF
   d. NAWUPF ≤ NAWUN
   e. NACWU ≥ ACWU
   f. NABSN ≥ NAWUN
   g. NABO ≤ NABSN
   h. NABO ≤ NABSPF
   i. NABSPF ≥ NAWUPF

**Possible Problems:** None.
Test 2.9 – AWUN/NAWUN (M)

Purpose: To verify that an NVMe Controller properly uses its Atomicity Parameters.

References:  
[1] NVMe Specification 6.4.1

Resource Requirements:  
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: August 29, 2017

Discussion: AWUN/NAWUN control the atomicity of command execution in relation to other commands. They impose inter-command serialization of writing of blocks of data to the NVM and prevent blocks of data ending up on the NVM containing partial data from one new command and partial data from one or more other new commands. If a write command is submitted with size less than or equal to the AWUN/NAWUN value and the write command does not cross an atomic boundary, then the host is guaranteed that the write command is atomic to the NVM with respect to other read or write commands. If a write command is submitted with size greater than the AWUN/NAWUN value or crosses an atomic boundary, then there is no guarantee of command atomicity. AWUN/NAWUN does not have any applicability to write errors caused by power failure or other error conditions.

Test Setup: See Appendix A.

Case 1: Atomic Boundaries Not Supported (NABSN/NABSPF = 0) (M)

Test Procedure:  
1. Ensure that both NABSN and NABSPF are set to 0. If not, this test case is not applicable and Case 2 below should be performed.
2. Configure the NVMe Host to issue 2 Write Commands, each with a length equal to 4 logical blocks. (i.e. if the logical block size is 512 bytes, the Write would be 2K in length. If the logical block size is 4K, the length of the Write would be 16K). The first command (Command A) will write Logical Blocks 0-3, with an FFFFh pattern. The second command (Command B) will write to Logical Blocks 1-4, with an AAAAh pattern.
3. Repeat for all supported Namespaces.

Observable Results:  
1. Verify that one of the following has occurred, any other outcome is a failure:  
   a. LBA 0-3 have an FFFFh pattern and LBA 4 has an AAAAh pattern.  
   b. LBA 0 has an FFFFh pattern and LBA 1-4 has an AAAAh pattern.

Case 2: Atomic Boundaries Supported (NABSN ≠ 0) (M)

Test Procedure:  
1. Determine if NABSN is set to a non-zero value. If not, this test case is not applicable and Case 1 above should be performed.
2. Configure the NVMe Host to issue 2 Write Commands, each with a length of half of NABSN. The first command (Command A) will write 4x sets of length NABSN, with an FFFFh pattern. The second command (Command B) will write 4x sets of length NABSN with an AAAAh pattern. Command B will be offset from Command A by half of NABSN. In total 5 sets of data with length ½ NABSN will be written.
3. Repeat for all supported Namespaces.

Observable Results:  
1. Verify that one of the following has occurred, any other outcome is a failure:  
   a. The first 4x NABSN of data is a FFFFh pattern and the last 1x NABSN of data is an AAAAh pattern.
b. The first 1x NABSN of data is a FFFFh pattern and the last 4x NABSN of data is an AAAAh pattern.

Possible Problems: For Case 2 above, NABSPF could be set to a non-zero value indicating support for Atomic Boundaries during a Power Failure. However, test capability has not been developed for testing Atomic Writes during Power Failure, so only the Normal condition is tested.
Test 2.10 – AWUPF/NAWUPF (IP)

Purpose: To verify that an NVMe Controller properly uses its Atomicity Parameters when a power failure occurs.

References:
[1] NVMe Specification 6.4.2

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 13, 2016

Discussion: AWUPF and NAWUPF indicate the behavior of the controller if a power fail or other error condition interrupts a write operation causing a torn write. A torn write is a write operation where only some of the logical blocks that are supposed to be written contiguously are actually stored on the NVM, leaving the target logical blocks in an indeterminate state in which some logical blocks contain original data and some logical blocks contain new data from the write operation.

If a write command is submitted with size less than or equal to the AWUPF/NAWUPF value and the write command does not cross an atomic boundary the controller guarantees that if the command fails due to a power failure or other error condition, then subsequent read commands for the logical blocks associated with the write command shall return one of the following:
- All old data (i.e. original data on the NVM in the LBA range addressed by the interrupted write), or
- All new data (i.e. all data to be written to the NVM by the interrupted write)

If a write command is submitted with size greater than the AWUPF/NAWUPF value or crosses an atomic boundary, then there is no guarantee of the data returned on subsequent reads of the associated logical blocks.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the DUT to use AWUPF/NAWUPF values to be greater than the size of 2 logical blocks.
2. Perform a READ operation to Logical Blocks 0-1.
3. Configure the NVMe Host to issue a Write Command, with a length equal to 2 logical blocks. (i.e. if the logical block size is 512 bytes, the Write would be 1K in length. If the logical block size is 4K, the length of the Write would be 8K). The command (Command A) will write Logical Blocks 0-1, with an AAAAh pattern.
   Before command completion, cause a Power Failure event.
4. Allow the PCIe link to reset, and for the NVMe Controller to return to the enabled state.
5. Perform a READ operation to Logical Blocks 0-1.

Observable Results:
1. Verify that one of the following has occurred, any other outcome is a failure:
   a. Contents of LBA 0-1 have an AAAAh pattern.
   b. Contents of LBA 0-1 are unchanged.

Possible Problems: Tools for reliably creating a power failure during a WRITE operation are not available. This test will remain an FYI test until such tools are available.
Group 3: NVM Features

Overview:

This section describes a method for performing conformance verification for NVMe products implementing NVM Features.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 3.1 – Metadata Handling (M)

**Purpose:** To verify that an NVMe Controller properly handles metadata.

**References:**
[1] NVMe Specification 8.2

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 28, 2017

**Discussion:** Metadata is additional data allocated on a per logical block basis. There is no requirement for how the host makes use of the metadata area. One of the most common usages for metadata is to convey end–to–end protection information. The metadata may be transferred by the controller to or from the host in one of two ways. The mechanism used is selected when the namespace is formatted.

One of the transfer mechanisms shall be selected for each namespace when it is formatted; transferring a portion of metadata with one mechanism and a portion with the other mechanism is not supported.

**Test Setup:** See Appendix A.

**Case 1: Extended LBA (M)**

The first mechanism for transferring the metadata is as a contiguous part of the logical block that it is associated with. The metadata is transferred at the end of the associated logical block, forming an extended logical block. This mechanism is illustrated in Figure 1. In this case, both the logical block data and logical block metadata are pointed to by the PRP1 and PRP2 pointers (or SGL Entry 1 if SGLs are used).

![Figure 1 – Contiguous Metadata with LBA Data, Forming Extended LBA](image)

**Test Procedure:**
1. Check the Metadata Size (MS) field in the Identify LBA Format Data Structure, which is within the Identify Namespace Data Structure. If MS is set to 0, then Metadata is not supported and this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller specifying an LBA in a namespace which has been formatted to allow metadata via extended LBAs with known data patterns for both the data and metadata.
3. Configure the NVMe Host to issue a Read command to the controller specifying the LBA which was previously written to.

**Observable Results:**
1. Verify that the data and metadata returned by the controller exactly match the data and metadata patterns which were written.

**Case 2: Separate Buffer (M)**

The second mechanism for transferring the metadata is as a separate buffer of data. This mechanism is illustrated in Figure 2. In this case, the metadata is pointed to with the Metadata Pointer, while the logical block data is pointed to by the Data Pointer. When a command uses PRPs for the metadata in the command, the metadata is required to be physically contiguous. When a command uses SGLs for the metadata in the command, the metadata is not required to be physically contiguous.
Test Procedure:
1. Check the Metadata Size (MS) field in the Identify LBA Format Data Structure, which is within the Identify Namespace Data Structure. If MS is set to 0, then Metadata is not supported and this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller specifying an LBA in a namespace which has been formatted to allow metadata via a separate buffer with known data patterns for both the data and metadata.
3. Configure the NVMe Host to issue a Read command to the controller specifying the LBA which was previously written to.

Observable Results:
1. Verify that the data and metadata returned by the controller exactly match the data and metadata patterns which were written.

Possible Problems: Support for each metadata transfer mechanism is indicated on a per namespace basis according to the FLBAS field Bit 4 of the Identify Namespace data structure. If there is no active namespaces which supports a specific transfer mechanism then tests utilizing that mechanism cannot be performed. If the NVMe Device targets NVMe Specification revision 1.2 or higher and the NVMe Controller Under Test supports the Namespace Management command, then the NVMe Host may create a new namespace which supports a specific transfer mechanism in order to perform procedure steps which require that transfer mechanism.
Test 3.2 – End-to-end Data Protection (M)

**Purpose:** To verify that an NVMe Controller can properly handle end-to-end data protection.

**References:**

[1] NVMe Specification 8.3

**Resource Requirements:**

Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** March 2, 2016

**Discussion:** To provide robust data protection from the application to the NVM media and back to the application itself, end-to-end data protection may be used. If this optional mechanism is enabled, then additional protection information (e.g. CRC) is added to the LBA that may be evaluated by the controller and/or host software to determine the integrity of the logical block.

This additional protection information, if present, is either the first eight bytes of metadata or the last eight bytes of metadata, based on the format of the namespace. For metadata formats with more than eight bytes, if the protection information is contained within the first eight bytes of metadata, then the CRC does not cover any metadata bytes. For metadata formats with more than eight bytes, if the protection information is contained within the last eight bytes of metadata, then the CRC covers all metadata bytes up to but excluding these last eight bytes.

**Test Setup:** See Appendix A.

**Test Procedure:**

1. Check the DPC field of the Identify Namespace Data Structure to determine if the DUT supports End to End Data Protection Capabilities. If DPC set to 0, this test is not applicable.
2. Configure the NVMe Host to issue a Write command to the controller with the PRACT bit cleared to ‘0’ and specifying an LBA in a namespace which has been formatted with protection information and also specifying properly formatted protection information with a known data pattern.
3. Configure the NVMe Host to issue a Write command to the controller with the PRACT bit cleared to ‘0’ and specifying an LBA in a namespace which has been formatted with protection information and also specifying improperly formatted protection information.
4. Configure the NVMe Host to issue a Write command to the controller with the PRACT bit set to ‘1’ and specifying an LBA in a namespace which has been formatted with protection information and also specifying a known data pattern.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. For steps 1 and 4, verify that the completion queue entry for each command indicates Success status.
3. For step 3, verify that the completion queue entry for the command indicates an appropriate status code (i.e., End–to–end Guard Check, End–to–end Application Tag Check or End–to–end Reference Tag Check depending on how the protection information was improperly formatted).

**Figure 3 – Write Command Protection Information Processing**

(a) No Protection Information

(b) Protection Information with PRACT bit cleared to ‘0’ (i.e., pass)

(c) Protection Information with PRACT bit set to ‘1’ (i.e., insert)

**Case 2: Read Command Processing (M)**

Figure 4 illustrates the protection information processing that may occur as a side effect of a Read command. The processing parallels Write command processing with the exception that logical block data flows in the opposite direction. When the PRACT bit is cleared to ‘0’ and the namespace was formatted with protection information, logical block data and metadata are transferred from NVM to the host and checked by the controller. When the PRACT bit is set to ‘1’ and the namespace was formatted with protection information, logical block data and metadata are transferred from the NVM to the controller. The controller checks the protection information and then removes it from the metadata before passing the LBA to the host. If the namespace format contains metadata beyond the protection information, then the protection information is not stripped regardless of the state of the PRACT bit (i.e., the metadata field remains the same size in the host as that in NVM).
Figure 4 – Read Command Protection Information Processing

(a) No Protection Information

(b) Protection Information with PRACT bit cleared to ‘0’ (i.e., pass)

(c) Protection Information with PRACT bit set to ‘1’ (i.e., strip)

Test Procedure:
1. Check the DPC field of the Identify Namespace Data Structure to determine if the DUT supports End to End Data Protection Capabilities. If DPC set to 0, this test is not applicable.
2. Configure the NVMe Host to issue a Read command to the controller with the PRACT bit cleared to ‘0’ and specifying the LBA which was written to in Case 1 step 1.
3. Configure the NVMe Host to issue a Read command to the controller with the PRACT bit cleared to ‘0’ and specifying the LBA which was written to in Case 1 step 4.
4. Configure the NVMe Host to issue a Write command to the controller with the PRACT bit set to ‘1’ and specifying the LBA which was written to in Case 1 step 1.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.
2. For step 1, verify that data returned by the controller exactly matches the data and metadata which was written.
3. For step 3, verify that the data returned by the controller exactly matches the data which was written and contains additional metadata containing properly formatted and correct protection information.
4. For step 4, verify that the data returned by the controller contains no protection information.

Possible Problems:
Case 2 requires reading the data which was written in Case 1. Therefore these test cases must be performed in succession or the data must be rewritten as part of the Case 2 test procedure implementation.
Test 3.3 – Power Management (M, OF)

Purpose: To verify that an NVMe Controller can properly handle power management.

References:
[1] NVMe Specification 8.4

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 24, 2015

Discussion: The power management capability allows the host to manage NVM subsystem power statically or dynamically. Static power management consists of the host determining the maximum power that may be allocated to an NVM subsystem and setting the NVM Express power state to one that consumes this amount of power or less. Dynamic power management is illustrated in Figure 5 and consists of the host modifying the NVM Express power state to best satisfy changing power and performance objectives. This power management mechanism is meant to complement and not replace autonomous power management performed by a controller.

Figure 5 – Dynamic Power Management

The number of power states implemented by a controller is returned in the Number of Power States Supported (NPSS) field in the Identify Controller data structure. A controller shall support at least one power state and may optionally support up to a total of 32 power states. Power states are contiguously numbered starting with zero such that each subsequent power state consumes less than or equal to the maximum power consumed in the previous state. Thus, power state zero indicates the maximum power that the NVM subsystem is capable of consuming.

Associated with each power state is a Power State Descriptor in the Identify Controller data structure. The descriptors for all implemented power states may be viewed as forming a table as shown in Table 7 which contains sample power state values for a controller with seven implemented power states.

Test Setup: See Appendix A.

Case 1: Relative Write Latency (M, OF)

Relative Write Latency (RWL): This field indicates the relative write latency associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means lower write latency.
Table 7 – Example Power State Descriptor Table

<table>
<thead>
<tr>
<th>Power State</th>
<th>Maximum Power (MP) (W)</th>
<th>Entry Latency (ENT-LAT) (µs)</th>
<th>Exit Latency (EXIT-LAT) (µs)</th>
<th>Relative Read Throughput (RRT)</th>
<th>Relative Write Throughput (RWT)</th>
<th>Relative Read Latency (RRL)</th>
<th>Relative Write Latency (RWL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>25</td>
<td>5</td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>18</td>
<td>5</td>
<td>7</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>18</td>
<td>5</td>
<td>8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>15</td>
<td>20</td>
<td>15</td>
<td>2</td>
<td>0</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>8</td>
<td>50</td>
<td>50</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>20</td>
<td>5000</td>
<td>4</td>
<td>3</td>
<td>5</td>
<td>1</td>
</tr>
</tbody>
</table>

Test Procedure:
1. Configure the NVMe Host to issue an Identify command specifying CNS value 01h to the controller in order to receive back an Identify Controller data structure.
2. For each power state supported by the controller as indicated by the NPSS field, read the RWL field of the associated Power State Descriptor.

Observable Results:
1. Verify that the relative write latency values are all less than the number of supported power states.

Case 2: Relative Write Throughput (M, OF)
Relative Write Throughput (RWT): This field indicates the relative write throughput associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means higher write throughput.

The amount of data an application can write to stable storage on the server over a period of time is a measurement of the write throughput of a distributed file system. Write throughput is therefore an important aspect of performance.

Test Procedure:
1. Configure the NVMe Host to issue an Identify command specifying CNS value 01h to the controller in order to receive back an Identify Controller data structure.
2. For each power state supported by the controller as indicated by the NPSS field, read the RWL field of the associated Power State Descriptor.

Observable Results:
1. Verify that the relative write throughput values are all less than the number of supported power states.

Case 3: Relative Read Latency (M, OF)
Relative Read Latency (RRL): This field indicates the relative read latency associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means lower read latency.

Test Procedure:
1. Configure the NVMe Host to issue an Identify command specifying CNS value 01h to the controller in order to receive back an Identify Controller data structure.
2. For each power state supported by the controller as indicated by the NPSS field, read the RWL field of the associated Power State Descriptor.

Observable Results:
1. Verify that the relative read latency values are all less than the number of supported power states.
Case 4: Relative Read Throughput (M, OF)

Relative Read Throughput (RRT): This field indicates the relative read throughput associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means higher read throughput.

Test Procedure:
1. Configure the NVMe Host to issue an Identify command specifying CNS value 01h to the controller in order to receive back an Identify Controller data structure.
2. For each power state supported by the controller as indicated by the NPSS field, read the RWL field of the associated Power State Descriptor.

Observable Results:
1. Verify that the relative read throughput values are all less than the number of supported power states.

Case 5: Power Management Feature (M, OF-FYI)

The host may dynamically modify the power state using the Set Features command and determine the current power state using the Get Features command. The host may directly transition between any two supported power states. The Entry Latency (ENTLAT) field in the power management descriptor indicates the maximum amount of time in microseconds that it takes to enter that power state and the Exit Latency (EXLAT) field indicates the maximum amount of time in microseconds that it takes to exit that state. The maximum amount of time to transition between any two power states is equal to the sum of the old state’s exit latency and the new state’s entry latency. The host is not required to wait for a previously submitted power state transition to complete before initiating a new transition.

Test Procedure:
1. Configure the NVMe Host to issue a Set Features command for the Power Management Feature for each of the supported Power State values supported by the NVMe Controller to the controller.
2. After each Set Features command completes, configure the NVMe Host to issue a Get Features command for the Power Management Feature to the controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. For each Get Features command, verify that the controller successfully transitioned to the selected power state.

Possible Problems: None.
Test 3.4 – Host Memory Buffer (M)

Purpose: To verify that an NVMe system can properly handle supports host memory buffer.

References:

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: December 21, 2017

Discussion: The Host Memory Buffer feature allows the controller to utilize an assigned portion of host memory exclusively. The use of the host memory resources is vendor specific. Host software may not be able to provide any or a limited amount of the host memory resources requested by the controller. The controller shall function properly without host memory resources. Refer to section 5.14.1.13 of the NVMe Specification.

During initialization, host software may provide a descriptor list that describes a set of host memory address ranges for exclusive use by the controller. The host memory resources assigned are for the exclusive use of the controller (host software should not modify the ranges) until host software requests that the controller release the ranges and the controller completes the Set Features command. The controller is responsible for initializing the host memory resources. Host software should request that the controller release the assigned ranges prior to a shutdown event, a Runtime D3 event, or any other event that requires host software to reclaim the assigned ranges. After the controller acknowledges that it is no longer using the ranges, host software may reclaim the host memory resources. In the case of Runtime D3, host software should provide the host memory resources to the controller again and inform the controller that the ranges were in use prior to the RTD3 event and have not been modified.

Test Setup: See Appendix A.

Case 1: Proper Structure (M)

Test Procedure:
1. Check the HMPRE field of the Identify Controller data structure to determine if the DUT supports Host Memory Buffer. If the HMPRE field is set to 0, this test is not applicable.
2. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Admin Completion Queue indicating the status for the command.
2. Verify that the Host Memory Buffer Preferred Size (HMPRE) field of the Identify Controller data structure is larger than or equal to the value indicated by the Host Memory Buffer Minimum Size (HMMIN) field.

Case 2: Configuration (FYI)
The Host Memory Feature controls the Host Memory Buffer. The attributes are indicated in Command Dword 11, Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15.

The Host Memory Buffer feature provides a mechanism for the host to allocate a portion of host memory for the controller to use exclusively. After a successful completion of a Set Features enabling the host memory buffer, the host shall not write to the associated host memory region, buffer size, or descriptor list until the host memory buffer has been disabled.

After a successful completion of a Set Features command that disables the host memory buffer, the
controller shall not access any data in the host memory buffer until the host memory buffer has been
enabled. The controller should retrieve any necessary data from the host memory buffer in use before
posting the completion queue entry for the Set Features command. Posting of the completion queue entry for the Set
Features command acknowledges that it is safe for the host software to modify the host memory buffer contents.
Refer to section 8.9 of the NVMe Specification.

Test Procedure:
1. Check the HMPRE field of the Identify Controller data structure to determine if the DUT supports Host
   Memory Buffer. If the HMPRE field is set to 0, this test is not applicable.
2. Configure the NVMe Host to issue a Set Features command for the Host Memory Buffer feature with the
   Enable Host Memory (EHM) bit set to ‘1’ to the NVMe Controller.
3. Configure the NVMe Host to issue a Get Features command for the Host Memory Buffer feature to the
   NVMe Controller.
4. Configure the NVMe Host to issue a Set Features command for the Host Memory Buffer feature with the
   Enable Host Memory (EHM) bit cleared to ‘0’ to the NVMe Controller.
5. Configured the NVMe Host to issue a Get Features command for the Host Memory Buffer feature to the
   NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the
   Admin Completion Queue indicating the status for the command.
2. Verify in each case that the value for EHM returned by the controller in response to the Get Feature
   command matches what was set by the Host in the Set Feature command.

Case 3: Reset Persistent (FYI)
The host memory resources are not persistent in the controller across a reset event. Host software should provide the
previously allocated host memory resources to the controller after the reset completes. If host software is providing
previously allocated host memory resources (with the same contents) to the controller, the Memory Return bit is set
to ‘1’ in the Set Features command. The controller shall ensure that there is no data loss or data corruption in the
event of a surprise removal while the Host Memory Buffer feature is being utilized.

Test Procedure:
1. Check the HMPRE field of the Identify Controller data structure to determine if the DUT supports Host
   Memory Buffer. If the HMPRE field is set to 0, this test is not applicable.
2. Configure the NVMe Host to issue a Get Features command for the Host Memory Buffer feature to the
   NVMe Controller.
3. Configure the NVMe Host to issue a Set Features command for the Host Memory Buffer feature with
   the Enable Host Memory (EHM) bit set to ‘1’ and Save (SV) set to 0, to the NVMe Controller.
4. Configure the NVMe Host to issue a Get Features command for the Host Memory Buffer feature to the
   NVMe Controller.
5. Configure the NVMe Host to issue a Controller Level Reset to the NVMe Controller.
6. Configure the NVMe Host to issue a Get Features command for the Host Memory Buffer feature to the
   NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the
   Admin Completion Queue indicating the status for the command.
2. Verify that the DUT responds to the Get Features command in step 4 with EHM set to 1.
3. Verify that after the controller reset, the controller responds to the Get Feature command with EHM set to
   0.

Possible Problems: None.
Test 3.5 – Replay Protected Memory Block (IP)

**Purpose:** To verify that an NVMe system can properly handle replay protected memory blocks.

**References:**
[1] NVMe Specification 8.10

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** April 28, 2016

**Discussion:** The Replay Protected Memory Block (RPMB) provides a means for the system to store data to a specific memory area in an authenticated and replay protected manner. This is provided by first programming authentication key information to the controller that is used as a shared secret. The system is not authenticated in this phase, therefore the authentication key programming should be done in a secure environment (e.g., as part of the manufacturing process). The authentication key is utilized to sign the read and write accesses made to the replay protected memory area with a Message Authentication Code (MAC). Use of random number (nonce) generation and a write count register provide additional protection against replay of messages where messages could be recorded and played back later by an attacker.

The controller may support multiple RPMB targets. RPMB targets are not contained within a namespace. Security Send and Security Receive commands for RPMB do not use the namespace ID field; NSID shall be cleared to 0h. Each RPMB target operates independently – there may be requests outstanding to multiple RPMB targets at once (where the requests may be interleaved between RPMB targets). In order to guarantee ordering the host should issue and wait for completion for one Security Send or Security Receive command at a time. Each RPMB target requires individual authentication and key programming. Each RPMB target may have its own unique Authentication Key.

The message types defined in Figure 223 of the NVMe Specification are used by the host to communicate with an RPMB target. Request Message Types are sent from the host to the controller. Response Message Types are sent to the host from the controller.

**Test Setup:** See Appendix A.

**Case 1: RPMB Operations (IP)**

The host sends a Request Message Type to the controller to request an operation by the controller or to deliver data to be written into the RPMB memory block. To deliver a Request Message Type, the host uses the Security Send command. If the data to be delivered to the controller is more than reported in Identify Controller data structure, the host sends multiple Security Send commands to transfer the entire data.

The host sends a Response Message Type to the controller to read the result of a previous operation request, to read the Write Counter, or to read data from the RPMB memory block. To deliver a Response Message Type, the host uses the Security Receive command. If the data to be read from the controller is more than reported in Identify Controller data structure, the host sends multiple Security Receive commands to transfer the entire data.

**Test Procedure:**
1. Configure the NVMe Host to issue a Security Send command with the feature ID set to Replay Protected Memory Blocks to the NVMe Controller.
2. Configure the NVMe Host to issue a Security Recieve command with the feature ID set to Replay Protected Memory Blocks to the NVMe Controller.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that the data received is correct, and if the data is larger than reported in the Identify Controller data structure the host sends multiple Security Receive commands to transfer the entire data.

Case 2: Authentication Key Programming (IP)
Authentication Key programming is initiated by a Security Send command to program the Authentication Key to the specified RPMB target, followed by a subsequent Security Send command to request the result, and lastly, the host issues a Security Receive command to retrieve the result.

Test Procedure:
1. Configure the NVMe Host to issue a Security Send command for the Replay Protected Memory Blocks Feature to the NVMe Controller, with the RPMB target set to a target to access, and the Mac/Key field set to the key to be programmed, and the Request/Response field set to “0001h”.
2. Configure the NVMe Host to issue a Security Send command for the Replay Protected Memory Blocks Feature to the NVMe Controller, with the RPMB target set to a target to access, and the Request/Response field set to “0005h”.
3. Configure the NVMe Host to issue a Security Receive command for the Replay Protected Memory Blocks Feature to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify the Security Receive command is populated correctly by the NVMe Controller.

Case 3: Read Write Counter Value (IP)
The Read Write Counter Value sequence is initiated by a Security Send command to request the Write Counter value, followed by a Security Receive command to retrieve the Write Counter result.

Test Procedure:
1. Configure the NVMe Host to issue a Security Send command for the Replay Protected Memory Blocks Feature to the NVMe Controller, with the RPMB target set to a target to access, and the Nonce field set to a specific Nonce generated by the host, and the Request/Response field set to “0002h”.
2. Configure the NVMe Host to issue a Security Receive command for the Replay Protected Memory Blocks Feature to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify the Security Receive command is populated correctly by the NVMe Controller.

Case 4: Authenticated Data Write (IP)
The success of programming the data should be checked by the host by reading the result register of the RPMB.
1. The host initiates the Authenticated Data Write verification process by issuing a Security Send command with delivery of a RPMB data frame containing the Request Message Type = 0005h.
2. The controller returns a successful completion of the Security Send command when the verification result is ready for retrieval.
3. The host should then retrieve the verification result by issuing a Security Receive command.
4. The controller returns a successful completion of the Security Receive command and returns the RPMB data frame containing the Response Message Type = 0300h, the incremented counter value, the data address, the MAC and result of the data programming operation.

Test Procedure:
1. Configure the NVMe Host to issue a Security Send command for the Replay Protected Memory Blocks Feature to the NVMe Controller, with the Mac/Key field set to a MAC generated by the host, and the RPMB target set to a target to access, and the Write Counter field set to the current write counter value, and the Address field set to the RPMB address, and the Sector Count field set the to the number of 512B blocks, and the Request/Response field set to “0003h”, and the Data field set to data to be written.

2. Configure the NVMe Host to issue a Security Send command for the Replay Protected Memory Blocks Feature to the NVMe Controller, with the RPMB target set to a target to access, and the Request/Response field set to “0005h”

3. Configure the NVMe Host to issue a Security Receive command for the Replay Protected Memory Blocks Feature to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify the Security Receive command is populated correctly by the NVMe Controller.

Case 5: Authenticated Data Read (IP)
The Authenticated Data Read sequence is initiated by a Security Send command. The RPMB data frame delivered from the host to the controller includes the Request Message Type = 0004h, Nonce, Address, and the Sector Count.

When the controller receives this RPMB Data Frame, it first checks the Address. If there is an error in the Address then the result is set to 0004h (address failure) and the data read is not valid. When the host receives a successful completion of the Security Send command from the controller, it should send a Security Receive command to the controller to retrieve the data. The controller returns an RPMB Data Frame with Response Message Type (0400h), the Sector Count, a copy of the Nonce received in the request, the Address, the Data, the controller calculated MAC, and the Result. Note: It is the responsibility of the host to verify the MAC returned on an Authenticated Data Read Request.

If the data transfer from the addressed location in the controller fails, the returned Result is 0006h (read failure). If the Address provided in the Security Send command is not valid, then the returned Result is 0004h (address failure). If another error occurs during the read procedure then the returned Result is 0001h (general failure).

Test Procedure:
1. Configure the NVMe Host to issue a Security Send command for the Replay Protected Memory Blocks Feature to the NVMe Controller, with the RPMB target set to a target to access, and the Nonce field set to a Nonce generated by the host, and the Address field set to the RPMB address, and the Sector Count set to the number of 512B blocks, and the Request/Response field set to “0004h”, and the Data field set to data to be written.

2. Configure the NVMe Host to issue a Security Receive command for the Replay Protected Memory Blocks Feature to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify the Security Receive command is populated correctly by the NVMe Controller.

Possible Problems: This is a Mandatory if Supported test, depending on device feature support according to the Replay Protected Memory Block Support (RPMBS) field of the Identify Controller data structure.
Group 4: Controller Registers

Overview:

This section describes a method for performing conformance verification for NVMe products implementing the NVMe Controller Registers.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 4.1 – Offset 00h: CAP – Memory Page Size Maximum (MPSMAX) (M, OF)

**Purpose:** To validate the MPSMAX field of the Controller Capabilities (CAP) register of an NVMe Controller.

**References:**
[1] NVMe Specification 3.1.1

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** This field indicates the maximum host memory page size that the controller supports. The maximum memory page size is \(2^{(12 + \text{MPSMAX})}\) (i.e. \(2^{12+\text{MPSMAX}}\)). Therefore, the maximum memory page size which a controller may support is 128MB. The host shall not configure a memory page size in CC.MPS that is larger than this value.

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to read the CAP.MPSMAX register field (bits 55:52) of the NVMe Controller.

**Observable Results:**
1. Verify that the value of the CAP.MPSMAX register field is greater than or equal to the value of the CAP.MPSMIN register field.

**Possible Problems:** None
Test 4.2 – Offset 00h: CAP – Memory Page Size Minimum (MPSMIN) (M, OF)

**Purpose:** To validate the MPSMIN field of the Controller Capabilities (CAP) register of an NVMe Controller.

**References:**
[1] NVMe Specification 3.1.1

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** This field indicates the minimum host memory page size that the controller supports. The minimum memory page size is \(2^{12+MPSMIN}\) (i.e. \(2^{12+MPSMIN}\)). Therefore, the minimum memory page size which a controller may support is 4KB. The host shall not configure a memory page size in CC.MPS that is smaller than this value.

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to read the CAP.MPSMIN register field (bits 51:48) of the NVMe Controller.

**Observable Results:**
1. Verify that the value of the CAP.MPSMAX register field is greater than or equal to the value of the CAP.MPSMIN register field.

**Possible Problems:** None.
Test 4.3 – Offset 00h: CAP – Command Sets Supported (CSS) (M, OF)

Purpose: To validate the Command Sets Supported (CSS) field of the Controller Capabilities (CAP) register of an NVMe Controller.

References:
[1] NVMe Specification 3.1.1

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: December 16, 2013

Discussion: This field indicates the I/O Command Set(s) that the controller supports. A minimum of one command set shall be supported. The field is bit significant (bit definitions can be found in Table 8). If a bit is set to ‘1’, then the corresponding I/O Command Set is supported. If a bit is cleared to ‘0’, then the corresponding I/O Command Set is not supported.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>37</td>
<td>NVM command set</td>
</tr>
<tr>
<td>38</td>
<td>Reserved</td>
</tr>
<tr>
<td>39</td>
<td>Reserved</td>
</tr>
<tr>
<td>40</td>
<td>Reserved</td>
</tr>
<tr>
<td>41</td>
<td>Reserved</td>
</tr>
<tr>
<td>42</td>
<td>Reserved</td>
</tr>
<tr>
<td>43</td>
<td>Reserved</td>
</tr>
<tr>
<td>44</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the CAP.CSS register field (bits 37:44) of the NVMe Controller.

Observable Results:
1. Verify that Bit 37 of the CAP.CSS register field is set to ‘1’ to indicate that the NVM Command Set is supported by the controller.

Possible Problems: None.
Test 4.4 – Offset 00h: CAP – Doorbell Stride (DSTRD) (M, OF)

Purpose: To validate the Doorbell Stride (DSTRD) field of the Controller Capabilities (CAP) register of an NVMe Controller.

References:
[1] NVMe Specification 3.1.1

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 2, 2016

Discussion: Each Submission Queue and Completion Queue Doorbell register is 32–bits in size. This register indicates the stride between doorbell registers. The stride is specified as \(2^{(2 + \text{DSTRD})}\) (i.e. \(2^{2+\text{DSTRD}}\)) in bytes. A value of 0h indicates a stride of 4 bytes, where the doorbell registers are packed without reserved space between each register.

Since there is no means to validate the value stored in this register field, this test is designed purely to determine the value the NVMe Controller returns when the register is read, and is therefore considered an informative test.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the CAP.DSTRD register field (bits 35:32) of the NVMe Controller.
2. Report the value of the CAP.DSTRD register field.

Observable Results: None.

Possible Problems: There are no required values for the CAP.DSTRD register field at any given time and so this test is run as informative with no pass/fail criteria.
Test 4.5 – Offset 00h: CAP – Timeout (TO) (M, OF-FYI)

**Purpose:** To validate the Timeout (TO) field of the Controller Capabilities (CAP) register of an NVMe Controller.

**References:**
[1] NVMe Specification 3.1.1

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** This is the worst case time that host software shall wait for CSTS.RDY to transition from:

a) ‘0’ to ‘1’ after CC.EN transitions from ‘0’ to ‘1’; or
b) ‘1’ to ‘0’ after CC.EN transitions from ‘1’ to ‘0’

This worst case time may be experienced after events such as an abrupt shutdown or activation of a new firmware image; typical times are expected to be much shorter. This field is in 500 millisecond units.

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to read the CAP.TO register field (bits 31:24) of the NVMe Controller.
2. Configure the NVMe Host to clear the CC.EN register field of the NVMe Controller to ‘0’ to initiate a controller reset.
3. Configure the NVMe Host to query the CSTS.RDY register field every 100 milliseconds until it transitions from ‘1’ to ‘0’.
4. Configure the NVMe Host to set the CC.EN register field of the NVMe Controller to ‘1’ to re-enable the controller (be sure to set required registers field prior to re-enabling the controller).
5. Configure the NVMe Host to query the CSTS.RDY register field every 100 milliseconds until it transitions from ‘0’ to ‘1’.

**Observable Results:**
1. Determine the elapsed time it takes for the CSTS.RDY register field value to transition after toggling the value of the CC.EN field. Verify that this value is less than or equal to the timeout value calculated from the CAP.TO register field read from the NVMe Controller.

**Possible Problems:** None
Test 4.6 – Offset 00h: CAP – Arbitration Mechanism Supported (AMS)(M, OF)

Purpose: To validate the Arbitration Mechanism Supported (AMS) field of the Controller Capabilities (CAP) register of an NVMe Controller.

References:
[1] NVMe Specification 3.1.1

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 24, 2015

Discussion: This field is bit significant (bit definitions can be found in Table 9) and indicates the optional arbitration mechanisms supported by the controller. If a bit is set to ‘1’, then the corresponding arbitration mechanism is supported by the controller. Refer to section 4.11 of the NVMe Specification for arbitration details.

Table 9 – CAP.AMS Bit Definitions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>Weighted Round Robin with Urgent Priority Class</td>
</tr>
<tr>
<td>18</td>
<td>Vendor Specific</td>
</tr>
</tbody>
</table>

The round robin arbitration mechanism is not listed since all controller shall support this arbitration mechanism.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the CAP.AMS register field (bits 18:17) of the NVMe Controller.
2. For each arbitration mechanism supported by the NVMe Controller as indicated by the CAP.AMS register field, configure the NVMe Host to set the CC.AMS register field to the corresponding value.

Observable Results:
1. For each supported arbitration mechanism, verify that the NVMe Host is able to successfully set the CC.AMS register field to the corresponding value.

Possible Problems: The weighted Round Robin with Urgent and Vendor Specific arbitration mechanisms are optional to support. Therefore, it is valid for both bits of the CAP.AMS field to be cleared to ‘0’.
Test 4.7 – Offset 00h: CAP – Contiguous Queues Required (CQR) (M, OF)

**Purpose:**
To validate the Contiguous Queues Required (CQR) field of the Controller Capabilities (CAP) register of an NVMe Controller.

**References:**
[1] NVMe Specification 3.1.1

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:**
March 2, 2016

**Discussion:**
This field is set to ‘1’ if the controller requires that I/O Submission Queues and I/O Completion Queues are required to be physically contiguous. This field is cleared to ‘0’ if the controller supports I/O Submission Queues and I/O Completion Queues that are not physically contiguous. If this field is set to ‘1’, then the Physically Contiguous bit (CDW11.PC) in the Create I/O Submission Queue and Create I/O Completion Queue commands shall be set to ‘1’.

Since there is no means to validate the value stored in this register field, this test is designed purely to determine the value the NVMe Controller returns when the register is read, and is therefore considered an informative test.

**Test Setup:**
See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to read the CAP.CQR register field (bit 16) of the NVMe Controller.
2. Report the value of the CAP.CQR register field.

**Observable Results:**
None.

**Possible Problems:**
There are no required values for the CAP.CQR register field at any given time and so this test is run as informative with no pass/fail criteria.
Test 4.8 – Offset 00h: CAP – Maximum Queue Entries Supported (MQES) (M, OF-FYI)

Purpose: To validate the Maximum Queue Entries Supported (MQES) field of the Controller Capabilities (CAP) register of an NVMe Controller.

References:
[1] NVMe Specification 3.1.1

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 24, 2015

Discussion: This field indicates the maximum individual queue size that the controller supports. This value applies to each of the I/O Submission Queues and I/O Completion Queues that host software may create. This is a 0’s based value. The maximum value is 1h, indicating two entries.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the CAP.MQES register field (bits 15:00) of the NVMe Controller.

Observable Results:
1. Verify that the value of the CAP.MQES register field is 1h or greater indicating 2 or more queue entries.

Possible Problems: None.
Test 4.9 – Offset 0Ch–10h: INTMS – Interrupt Mask Set and INTMC – Interrupt Mask Clear (M, OF)

**Purpose:** To validate the Interrupt Mask Set (INTMS) and Interrupt Mask Clear (INTMC) register of an NVMe Controller.

**References:**
[1] NVMe Specification 3.1.3, 3.1.4

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** The INTMS register is used to mask interrupts when using pin-based interrupts, single message MSI, or multiple message MSI. When using MSI–X, the interrupt mask table defined as part of MSI–X should be used to mask interrupts. Host software shall not access this register when configured for MSI–X; any accesses when configured for MSI–X is undefined.

The INTMC register is used to unmask interrupts when using pin-based interrupts, single message MSI, or multiple message MSI. When using MSI–X, then interrupt mask table defined as part of MSI–X should be used to unmask interrupts. Host software shall not access this register when configure for MSI–X; any accesses when configured for MSI–X is undefined.

The INTMS and INTMC registers both have a single field each: the Interrupt Vector Mask Set (IVMS) and Interrupt Vector Mask Clear (IVMC) fields respectively. Both fields are bit significant. If a ‘1’ is written to a bit in the IVMS field, then the corresponding interrupt vector is masked from generating an interrupt or reporting a pending interrupt in the MSI Capability Structure. If a ‘1’ is written to a bit in the IVMC field, then the corresponding interrupt vector is unmasked. Writing a ‘0’ to a bit has no effect. When read, these fields return the current interrupt mask value within the controller (not the value of their register). If a bit has a value of ‘1’, then the corresponding interrupt vector is masked. If a bit has a value of ‘0’, then the corresponding interrupt vector is not masked.

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to read the INTMS and INTMC registers of the NVMe Controller.
2. Configure the NVMe Host to write all zeros to both the INTMS and INTMC registers of the NVMe Controller.
3. Configure the NVMe Host to read the INTMS and INTMC registers of the NVMe Controller once again.

**Observable Results:**
1. Verify that the values returned by the registers do not change on subsequent reads after writing zeroes to their bits.

**Possible Problems:** None
Test 4.10 – Offset 14h: CC – I/O Completions Queue Entry Size (IOCQES) (M, OF)

**Purpose:** To validate the I/O Completion Queue Entry Size (IOCQES) field of the Controller Configuration (CC) register of an NVMe Controller.

**References:**

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** This field defines the I/O Completion Queue entry size that is used for the selected I/O Command Set. The required and maximum values for this field are specified in the Identify Controller data structure for each I/O Command Set. The value is in bytes and is specified as a power of two ($2^n$) (i.e. $2^y$).

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to read the CC.IOCQES register field (bits 23:20) of the NVMe Controller.

**Observable Results:**
1. Verify that the sizes of I/O completion queue entries are equal to 2 to the power of the value of the CC.IOCQES register field.

**Possible Problems:** None
Test 4.11 – Offset 14h: CC – I/O Submission Queue Entry Size (IOSQES) (M, OF)

Purpose: To validate the I/O Submission Queue Entry Size (IOCQES) field of the Controller Configuration (CC) register of an NVMe Controller.

References:

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 24, 2015

Discussion: This field defines the I/O Submission Queue entry size that is used for the selected I/O Command Set. The required and maximum values for this field are specified in the Identify Controller data structure for each I/O Command Set. The value is in bytes and is specified as a power of two \( (2^m) \) (i.e. \( 2^n \)).

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the CC.IOSQES field (bits 19:16) of the NVMe Controller.

Observable Results:
1. Verify that the sizes of I/O submission queue entries are equal to \( 2 \) to the power of the value of the CC.IOSQES register field.

Possible Problems: None.
Test 4.12 – Offset 14h: CC – Shutdown Notification (SHN) (M, OF)

**Purpose:** To validate the Shutdown Notification (SHN) field of the Controller Configuration (CC) register of an NVMe Controller.

**References:**


**Resource Requirements:**

Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** March 2, 2016

**Discussion:** This field is used to initiate shutdown processing when a shutdown is occurring, (i.e., a power down condition is expected). For a normal shutdown notification, it is expected that the controller is given time to process the shutdown notification. For an abrupt shutdown notification, the host may not wait for shutdown processing to complete before power is lost. The shutdown notification values are defined in Table 10.

<table>
<thead>
<tr>
<th>Value</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>No notification; no effect.</td>
</tr>
<tr>
<td>01b</td>
<td>Normal shutdown notification.</td>
</tr>
<tr>
<td>10b</td>
<td>Abrupt shutdown notification.</td>
</tr>
<tr>
<td>11b</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

This field should be written by host software prior to any power down condition and prior to any change of the PCI power management state. It is recommended that this field also be written prior to a warm reboot. To determine when shutdown processing is complete, refer to CSTS.SHST.

It is recommended that the host wait a minimum of the RTD3 Entry Latency reported in the Identify Controller data structure for the shutdown operations to complete; if the value reported in RTD3 Entry Latency is 0h, then the host should wait for a minimum of one second. It is not recommended to disable the controller via the CC.EN field. This causes a Controller Reset which may impact the time required to complete shutdown processes.

It is safe to power off the controller when CSTS.SHST indicates shutdown processing is complete. It remains safe to power off the controller until CC.EN transitions from '0' to '1'. To start executing commands on the controller after a shutdown operation, a Controller Reset is required. This initialization sequence should then be executed.

**Test Setup:** See Appendix A.

**Test Procedure:**

1. Configure the NVMe Host to read the CC.SHN register field (bits 15:14) of the NVMe Controller.
2. Configure the NVMe Host to write a value of 01b to the CC.SHN register field in order to initiate shutdown processing with a normal shutdown notification.
3. After the CSTS.SHST register field value transitions back to a value of 10b (shutdown processing complete), configure the NVMe Host to perform a full Controller Reset.
4. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h.
5. Configure the NVMe Host to write a value of 10b to the CC.SHN register field in order to initiate shutdown processing with an abrupt shutdown notification.
6. After the CSTS.SHST register field value transitions back to a value of 10b (shutdown processing complete), configure the NVMe Host to perform a full Controller Reset.
7. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h.

**Observable Results:**
1. Verify that the value of the CC.SHN register field is set to its default value of 00b (no notification) after a Controller Level Reset.
2. After the NVMe Host sets the value of the CC.SHN register field, verify that the controller sets the CSTS.SHST register field to its appropriate value as indicated in Table 13.
3. Verify that, after the NVMe Host performs a Controller Reset while CSTS.SHST indicates normal operation, the NVMe Host is able to issue commands to the NVMe Controller.

Possible Problems: None
Test 4.13 – Offset 14h: CC – Arbitration Mechanism Selected (AMS) (M, OF)

**Purpose:** To validate the Arbitration Mechanism Selected (AMS) field of the Controller Configuration (CC) register of an NVMe Controller.

**References:**

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** February 1, 2018

**Discussion:** This field selects the arbitration mechanism to be used. This value shall only be changed when EN is cleared to ‘0’. Host software shall only set this field to supported arbitration mechanisms indicated in CAP.AMS. If this field is set to an unsupported value, the behavior is undefined. The arbitration mechanism values are defined in Table 11.

Table 11 – CC.AMS Field Values

<table>
<thead>
<tr>
<th>Value</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>000b</td>
<td>Round Robin</td>
</tr>
<tr>
<td>001b</td>
<td>Weighted Round Robin with Urgent</td>
</tr>
<tr>
<td>010b – 110b</td>
<td>Reserved</td>
</tr>
<tr>
<td>111b</td>
<td>Vendor Specific.</td>
</tr>
</tbody>
</table>

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to set CC.EN to 0.
2. Configure the NVMe Host to read the CC.AMS register field of the NVMe Controller.
3. Configure the NVMe Host to read the CAP.AMS register field of the NVMe Controller.
4. For each optional arbitration mechanism reported to be supported by the CAP.AMS register field:
   a. Configure the NVMe Host to set the CC.AMS register field to the appropriate value for that mechanism.
   b. Configure the NVMe Host to read the CC.AMS register field of the NVMe Controller.

**Observable Results:**
1. Verify that the value of the CC.AMS register field is set to its default value of 000b when CC.EN is set to 0.
2. Verify that the NVMe Controller properly allows the NVMe Host to set supported values in the CC.AMS register field.

**Possible Problems:** The weighted Round Robin with Urgent and Vendor Specific arbitration mechanisms are optional to support. Therefore, it is valid for both bits of the CAP.AMS field to be cleared to ‘0’.
Test 4.14 – Offset 14h: CC – I/O Command Set Selected (CSS) (M, OF)

**Purpose:** To validate the I/O Command set Selected (CSS) field of the Controller Configuration (CC) register of an NVMe Controller.

**References:**

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** March 2, 2016

**Discussion:** This field specifies the I/O Command Set that is selected for use for the I/O Submission Queues. Host software shall only select a supported I/O Command Set, as indicated in CAP.CSS. This field shall only be changed when the controller is disabled (CC.EN is cleared to ‘0’). The I/O Command Set selected shall be used for all I/O Submission Queues. The command set values are defined in Table 12.

<table>
<thead>
<tr>
<th>Table 12 – CC.CSS Field Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
</tr>
<tr>
<td>000b</td>
</tr>
<tr>
<td>001b – 111b</td>
</tr>
</tbody>
</table>

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to read the CC.CSS register field (bits 06:04) of the NVMe Controller.
2. For each I/O Command Set supported by the NVMe Controller as indicated by the CAP.CSS register field:
   a. Configure the NVMe Host to set the CC.CSS register field to the appropriate value for that I/O Command Set.
   b. Configure the NVMe Host to read the CC.CSS register field of the NVMe Controller.

**Observable Results:**
1. Verify that the value of the CC.CSS register field is set to its default value of 000b after the NVMe Host clears the CC.EN register field to ‘0’ in order to initiate a Controller Reset (the host must set the CC.CSS field to a valid value prior to re-enabling the controller).
2. Verify that the NVMe Controller properly allows the NVMe Host to set supported values in the CC.CSS field.

**Possible Problems:** None
Test 4.15 – Offset 14h: CC – Enable (EN) (M, OF)

**Purpose:** To validate the Enable (EN) field of the Controller Configuration (CC) register of an NVMe Controller.

**References:**


**Resource Requirements:**

Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 21, 2012

**Discussion:** When set to ‘1’, the controller shall process commands based on Submission Queue Tail doorbell writes. When cleared to ‘0’, the controller shall not process commands nor post completion queue entries to Completion Queues. When this field transitions from ‘1’ to ‘0’, the controller is reset (referred to as a Controller Reset). The reset deletes all I/O Submission Queues and I/O Completion Queues, resets the Admin Submission Queue and Completion Queue, and brings the hardware to an idle state. The reset does not affect PCI Express registers nor the Admin Queue registers (AQA, ASQ, or ACQ). All other controller registers defined in section 3 of the NVMe specification and internal controller state (e.g., Feature values defined in section 5 of the NVMe specification that are not persistent across power states) are reset to their default values. The controller shall ensure that there is no data loss for commands that have had corresponding completion queue entries posted to an I/O Completion Queue prior to the reset operation. Refer to section 7.3 for reset details.

When this field is cleared to ‘0’, the CSTS.RDY bit is cleared to ‘0’ by the controller once the controller is ready to be re-enabled. When this field is set to ‘1’, the controller sets CSTS.RDY to ‘1’ when it is ready to process commands. CSTS.RDY may be set to ‘1’ before namespace(s) are ready to be accessed.

Setting this field from a ‘0’ to a ‘1’ when CSTS.RDY is a ‘1’, or setting this field from a ‘1’ to a ‘0’ when CSTS.RDY is a ‘0’ has undefined results. The Admin Queue registers (AQA, ASQ, and ACQ) shall only be modified when this field is cleared to ‘0’.

**Test Setup:** See Appendix A.

**Test Procedure:**

1. Configure the NVMe Host to read the CC.EN register field (bit 00) of the NVMe Controller.

**Observable Results:**

1. Verify that when Bit 0 of the CC.EN register field is set to ‘1’, the controller processes commands based on Submission Queue Tail doorbell writes.
2. Verify that when Bit 0 of the CC.EN register field is cleared to ‘0’, the controller does not process commands nor post completion queue entries to Completion Queues.

**Possible Problems:** None
Test 4.16 – Offset 1Ch: CSTS – Shutdown Status (SHST) (M, OF)

**Purpose:** To validate the Shutdown Status (SHST) field of the Controller Status (CSTS) register of an NVMe Controller.

**References:**


**Resource Requirements:**

Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** March 2, 2016

**Discussion:** This field indicates the status of shutdown processing that is initiated by the host setting the CC.SHN register field. The shutdown status values are defined in Table 13.

### Table 13 – CSTS.SHST Field Values

<table>
<thead>
<tr>
<th>Value</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>Normal operation (no shutdown has been requested)</td>
</tr>
<tr>
<td>01b</td>
<td>Shutdown processing occurring</td>
</tr>
<tr>
<td>10b</td>
<td>Shutdown processing complete</td>
</tr>
<tr>
<td>11b</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

To start executing commands on the controller after a shutdown operation (CSTS.SHST set to 10b), a reset (CC.EN cleared to ‘0’) is required. If host software submits commands to the controller without issuing a reset, the behavior is undefined.

**Test Setup:** See Appendix A.

**Test Procedure:**

1. Configure the NVMe Host to read the CSTS.SHST register field (bits 03:02) of the NVMe Controller.
2. Configure the NVMe Host to write a value of 01b to the CC.SHN register field in order to initiate shutdown processing with a normal shutdown notification.
3. Configure the NVMe Host to read the CSTS.SHST register field of the NVMe Controller.
4. After the CSTS.SHST register field value transitions back to a value of 10b (shutdown processing complete), configure the NVMe Host to perform a full Controller Reset.
5. Configure the NVMe Host to read the CSTS.SHST register field of the NVMe Controller.
6. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h.
7. Configure the NVMe Host to write a value of 10b to the CC.SHN register field in order to initiate shutdown processing with an abrupt shutdown notification.
8. Configure the NVMe Host to read the CSTS.SHST register field of the NVMe Controller.
9. After the CSTS.SHST register field value transitions back to a value of 10b (shutdown processing complete), configure the NVMe Host to perform a Controller Reset.
10. Configure the NVMe Host to read the CSTS.SHST register field of the NVMe Controller.
11. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h.

**Observable Results:**

1. Verify that the value of the CSTS.SHST register field is set to its default value of 00b (normal operation) after a Controller Level Reset.
2. After the NVMe Host sets the value of the CC.SHN register field to either 01b or 10b, verify that the NVMe Controller sets the CSTS.SHST register field to 01b to indicate that shutdown processing is occurring.
3. Record the time it takes for the NVMe Controller to transition the value of the CSTS.SHST register field from 01b to 10b (i.e. the shutdown processing time) for both normal and abrupt shutdown notifications.
4. Verify that, after the NVMe Host performs a Controller Reset while the CSTS.SHST register field indicates normal operation, the NVMe Host is able to issue commands to the NVMe Controller.

Possible Problems: None
Test 4.17 – Offset 1Ch: CSTS – Controller Fatal Status (CFS) (M, OF)

Purpose: To validate the Controller Fatal Status (CFS) field of the Controller Status (CSTS) register of an NVMe Controller.

References:

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 2, 2016

Discussion: This field is set to ‘1’ when a fatal controller error occurred that could not be communicated in the appropriate Completion Queue. This field is cleared to ‘0’ when a fatal controller error has not occurred. Refer to section 9.5.

The reset value of this field is ‘1’ when a fatal controller error is detected during controller initialization.

Since there is no means for a host to trigger a controller fatal status, there is no means to validate the value stored in this register field, and so this test is designed purely to determine the value the NVMe Controller returns when the register is read, and is therefore considered an informative test.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the CSTS.CFS field (bit 01) of the NVMe Controller.
2. Report the value of the CSTS.CFS field.

Observable Results: None.

Possible Problems: There are no explicit conditions for which the NVMe Host can generate a controller fatal status. Therefore this test is run as informative with no pass/fail criteria.
Test 4.18 – Offset -08h: CAP – Version (VS) (M, OF)

**Purpose:** To validate the Version (VS) field of the Capabilities (CAP) register of an NVMe Controller.

**References:**

[1] NVMe Specification 3.1.2

**Resource Requirements:**

Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** November 14, 2017

**Discussion:** This register indicates the major and minor version of the NVM Express specification that the controller implementation supports. Valid versions of the specification are: 1.0, 1.1, and 1.2.

**Test Setup:** See Appendix A.

**Test Procedure:**

1. Configure the NVMe Host to read the VS.CAP field of the NVMe Controller.
2. Report the value of the VS.CAP field.
3. Configure the NVMe Host to issue an Identify command to the NVMe Controller specifying CNS value 01h in order to retrieve the Identify Controller data structure.

Report the value of the VER field in the Identify Controller data structure returned by the DUT.

**Observable Results:**

1. Verify that the DUT reports a valid value for VS. Valid values are 1.0, 1.1, 1.2, 1.3
2. Verify that the version reported in the Identify Controller data structure matches the value reported in the VS.CAP field.
Group 5: System Memory Structure

**Overview:**

This section describes a method for performing conformance verification for NVMe products implementing the NVMe System Memory Structure.

**Notes:** The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 5.1 – Page Base Address and Offset (PBAO) (M, OF)

Purpose: To validate the Page Base Address and Offset field of PRP entries issued to an NVMe Controller.

References:
NVMe Specification 4.3

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: February 1, 2018

Discussion: A physical region page (PRP) entry is a point to a physical memory page. PRPs are used as a scatter/gather mechanism for data transfers between the controller and memory. To enable efficient out of order data transfers between the controller and the host, PRP entries are a fixed size.

The size of the physical memory page is configured by host software in CC.MPS. Figure 6 shows the layout of a PRP entry that consists of a Page Base Address and an Offset. The size of the Offset field is determined by the physical memory page size configured in CC.MPS.

The Page Base Address and Offset (PBAO) field indicates the 64–bit physical memory page address. The lower bits (n:2) of this field indicate the offset within the memory page. If the memory page size is 4KB, then bits 11:02 form the Offset; if the memory page size is 8KB, then bits 12:02 form the Offset, etc (i.e. n = CC.MPS + 11). If this entry is not the first PRP entry in the command or a PRP List pointer in a command, then the Offset portion of this field shall be cleared to 0h.

Figure 6 – PRP Entry Layout

<table>
<thead>
<tr>
<th>63</th>
<th>n+1</th>
<th>n</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Page Base Address</td>
<td>Offset</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to issue an Identify command with properly formatted PRP entries to the NVMe Controller.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

Possible Problems: None.
Test 5.2 – Completion Queue Entry (M)

Purpose: To verify that an NVMe Controller can properly post a completion queue entry to the proper Completion Queue.

References: NVMe Specification 4.6

Resource Requirements: Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 16, 2016

Discussion: An entry in the Completion Queue is 16 bytes in size. Figure 7 describes the layout of the Completion Queue Entry data structure. The contents of Dword 0 are command specific. If a command uses Dword 0, then the definition of this Dword is contained within the associated command definition. If a command does not use Dword 0, then the field is reserved. Dword 1 is reserved. Dword 2 is defined in Figure 26 and Dword 3 is defined in Figure 27 of the NVMe specification. Any additional I/O Command Set defined in the future may use an alternate Completion Queue entry size or format.

Figure 7 – Completion Queue Entry Layout – Admin and NVM Command Set

<table>
<thead>
<tr>
<th>DW0</th>
<th>DW1</th>
<th>DW2</th>
<th>DW3</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>23</td>
<td>15</td>
<td>7</td>
</tr>
</tbody>
</table>

The Status Field (SF) of Dword 3 is tested in Test 5.3 – Status Field Definition.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to setup and create two I/O Submission Queues paired with a single I/O Completion Queue.
2. Configure the NVMe Host to issue a Write command to the NVMe Controller through the first IOSQ.
3. Configure the NVMe Host to issue a Write command to the NVMe Controller through the second IOSQ.
4. Configure the NVMe Host to issue Write commands to the NVMe Controller through the first IOSQ until the IOSQ size number of commands have been issued.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the I/O Completion Queue indicating the status for the command.
2. Verify that the Submission Queue Identifier (SQID) field (bits 31:16) of Dword 2 of each completion queue entry is the SQID of the Submission Queue used to issue the command.
3. Verify that the Phase Tag (P) field (bit 16) of Dword 3 is set to 1 for the first round of completion queue entries arriving at the IOCQ and cleared to 0 for the second round of completion queue entries after the controller had wrapped around the top of the Completion Queue.
4. Verify that the Command Identifier (CID) field (bits 15:00) of Dword 3 for each completion queue entry matches the command ID assigned to the command by the NVMe Host when it was issued to the Submission Queue.
Possible Problems: None.
Test 5.3 – Status Field Definition (M, OF-FYI)

**Purpose:** To verify that an NVMe Controller can properly return the status in the completion queue entry for a command.

**References:**
- NVMe Specification 4.6.1

**Resource Requirements:**
- Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** The Status Field (SF) defines the status for the command indicated in the completion queue entry. If the SCT and SC fields are cleared to 0h, then this indicates a successful command completion, with no fatal or non-fatal error conditions.

The Status Field is bits 31:17 of Dword 3 of all completion queue entries.

The SCT and SC fields are further tested in subsequent tests.

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Configure the NVMe Host to issue an Identify command to the NVMe Controller.
2. After the NVMe Controller has processed the command, configure the NVMe Host to reap the completion queue entry for the Identify command from the Admin Completion Queue.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that the Status Code Type (SCT) field of the Status Field is 0h to indicate a Generic Command Status. Verify that the Status Code (SC) field of the Status Field is 0h to indicate successful completion of the command.

**Possible Problems:** None.
Test 5.4 – Generic Command Status Definition (M)

**Purpose:** To verify that an NVMe Controller can properly return Status Code values for the Generic Command Status type.

**References:**
NVMe Specification 4.6.1.2.1

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** Completion queue entries with a Status Code type of Generic Command Status (0h) indicate a status value associated with the command that is generic across all command types. The Status Code values for the Generic Command Status type are defined in Table 14 and Table 15.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>80h</td>
<td>LBA Out of Range: The command references an LBA that exceeds the size of the namespace.</td>
</tr>
<tr>
<td>81h</td>
<td>Capacity Exceeded: Execution of the command has caused the capacity of the namespace to be exceeded. This error occurs when the Namespace Utilization exceeds the Namespace Capacity.</td>
</tr>
<tr>
<td>82h</td>
<td>Namespace Not Ready: The namespace is not ready to be accessed. The Do Not Retry bit indicates whether re-issuing the command at a later time may succeed.</td>
</tr>
<tr>
<td>83h</td>
<td>Reservation Conflict: The command was aborted due to a conflict with a reservation held on the accessed namespace.</td>
</tr>
<tr>
<td>84h</td>
<td>Format In Progress. The namespace is currently being formatted. The Do Not Retry bit shall be cleared to '0' to indicate that the command may succeed if it is resubmitted.</td>
</tr>
<tr>
<td>85h – BFh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Test Setup:** See Appendix A.

**Test Procedure:**
1. For each of the Status Code values defined in Table 14 and Table 15, configure the NVMe Host to issue a command to the NVMe Controller which will cause the controller to return the Status Code in the completion queue entry for the command.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is cleared to 0h. Verify that the SC field of the Status field matches the expected Status Code.

**Possible Problems:** The NVMe specification does not explicitly state the exact conditions for when an NVMe Controller should use some of the defined Status Codes. Such status codes cannot be tested.
### Table 15 – Generic Command Status Values

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Successful Completion: The command completed successfully.</td>
</tr>
<tr>
<td>01h</td>
<td>Invalid Command Opcode: The associated command opcode field is not valid.</td>
</tr>
<tr>
<td>02h</td>
<td>Invalid Field in Command: An invalid field in the command parameters.</td>
</tr>
<tr>
<td>03h</td>
<td>Command ID Conflict: The command identifier is already in use. Note: It is implementation specific how many commands are searched for a conflict.</td>
</tr>
<tr>
<td>04h</td>
<td>Data Transfer Error: Transferring the data or metadata associated with a command had an error.</td>
</tr>
<tr>
<td>05h</td>
<td>Commands Aborted due to Power Loss Notification: Indicates that the command was aborted due to a power loss notification.</td>
</tr>
<tr>
<td>06h</td>
<td>Internal Error: The command was not completed successfully due to an internal error. Details on the internal device error are returned as an asynchronous event. Refer to section 5.2.</td>
</tr>
<tr>
<td>07h</td>
<td>Command Abort Requested: The command was aborted due to a Command Abort command being received that specified the Submission Queue Identifier and Command Identifier of this command.</td>
</tr>
<tr>
<td>08h</td>
<td>Command Aborted due to SQ Deletion: The command was aborted due to a Delete I/O Submission Queue request received for the Submission Queue to which the command was submitted.</td>
</tr>
<tr>
<td>09h</td>
<td>Command Aborted due to Failed Fused Command: The command was aborted due to the other command in a fused operation failing.</td>
</tr>
<tr>
<td>0Ah</td>
<td>Command Aborted due to Missing Fused Command: The command was aborted due to the companion fused command not being found as the subsequent Submission Queue entry.</td>
</tr>
<tr>
<td>0Bh</td>
<td>Invalid Namespace or Format: The namespace or the format of that namespace is invalid.</td>
</tr>
<tr>
<td>0Ch</td>
<td>Command Sequence Error: The command was aborted due to a protocol violation in a multi-command sequence (e.g., a violation of the Security Send and Security Receive sequencing rules in the TCG Storage Synchronous Interface Communications protocol).</td>
</tr>
<tr>
<td>0Dh</td>
<td>Invalid SGL Last Segment Descriptor: The command includes an invalid SGL Last Segment. This may occur when the SGL segment pointed to by an SGL Last Segment descriptor contains an SGL Segment descriptor or an SGL Last Segment descriptor. This may occur when an SGL Last Segment descriptor contains an invalid length (i.e., a length of zero or one that is not a multiple of 16).</td>
</tr>
<tr>
<td>0Eh</td>
<td>Invalid Number of SGL Descriptors: The number of SGL descriptors or SGL Last Segment descriptors in a SGL segment is greater than one.</td>
</tr>
<tr>
<td>0Fh</td>
<td>Data SGL Length Invalid: The length of a Data SGL is too short or too long.</td>
</tr>
<tr>
<td>10h</td>
<td>Metadata SGL Length Invalid: The length of a Metadata SGL is too short or too long.</td>
</tr>
<tr>
<td>11h</td>
<td>SGL Descriptor Type Invalid: The type of an SGL Descriptor is a type that is not supported by the controller.</td>
</tr>
<tr>
<td>12h</td>
<td>Invalid Use of Controller Memory Buffer: The attempted use of the Controller Memory Buffer is not supported by the controller.</td>
</tr>
<tr>
<td>13h</td>
<td>PRP Offset Invalid: The Offset field for a PRP entry is invalid. This may occur when there is a PRP entry with a non-zero offset after the first entry.</td>
</tr>
<tr>
<td>14h</td>
<td>Atomic Write Unit Exceeded: The length specified exceeds the atomic write unit size.</td>
</tr>
<tr>
<td>15h–7Fh</td>
<td>Reserved</td>
</tr>
<tr>
<td>80h–BFh</td>
<td>I/O Command Set Specific</td>
</tr>
<tr>
<td>C0h–FFh</td>
<td>Vendor Specific</td>
</tr>
</tbody>
</table>
Test 5.5 – Command Specific Errors Definition (M)

**Purpose:** To verify that an NVMe Controller can properly return the Status Code values for the Command Specific Status type.

**References:** 4.6.1.2.2 Figure 33, 5.21.1.9 (Case 7)

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** July 17, 2017

**Discussion:** Completion queue entries with a Status Code Type of Command Specific Errors (01h) indicate an error that is specific to a particular command opcode. These status values may indicate additional processing is required. The Status Code values for the Command Specific Status Type are defined in Error! Reference source not found. and Table 16.

For each of the Status Code values defined in Table 16 and 17 configure the NVMe Host to issue a command to the NVMe Controller which will cause the controller to return the Status Code in the completion queue entry for the command.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Commands Affected</th>
<th>Test Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>80h</td>
<td>Conflicting Attributes</td>
<td>Dataset Management, Read, Write</td>
<td></td>
</tr>
<tr>
<td>81h</td>
<td>Invalid Protection Information</td>
<td>Compare, Read, Write, Write</td>
<td></td>
</tr>
<tr>
<td>82h</td>
<td>Attempted Write to Read Only Range</td>
<td>Dataset Management, Write, Write Uncorrectable, Write</td>
<td></td>
</tr>
<tr>
<td>83h – BFh</td>
<td>Reserved</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Commands Affected</th>
<th>Test Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Completion Queue Invalid</td>
<td>Create I/O Submission Queue</td>
<td>Test 1.4 Case 7</td>
</tr>
<tr>
<td>01h</td>
<td>Invalid Queue Identifier</td>
<td>Create I/O Submission Queue, Create I/O Completion Queue, Delete I/O Submission Queue, Delete I/O Completion Queue</td>
<td>Test 1.4 Case 2 and 7</td>
</tr>
<tr>
<td>02h</td>
<td>Invalid Queue Size</td>
<td>Create I/O Submission Queue, Create I/O Completion Queue</td>
<td>Test 1.4 Case 4 and 5</td>
</tr>
<tr>
<td>03h</td>
<td>Abort Command Limit Exceeded</td>
<td>Abort</td>
<td>Test 5.5 Case 1</td>
</tr>
<tr>
<td>04h</td>
<td>Reserved</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>05h</td>
<td>Asynchronous Event Request Limit Exceeded</td>
<td>Asynchronous Event Request</td>
<td>Test 5.5 Case 2</td>
</tr>
<tr>
<td>06h</td>
<td>Invalid Firmware Slot</td>
<td>Firmware Commit</td>
<td>Test 5.5 Case 3</td>
</tr>
<tr>
<td>07h</td>
<td>Invalid Firmware Image</td>
<td>Firmware Commit</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>08h</td>
<td>Invalid Interrupt Vector</td>
<td>Create I/O Completion Queue</td>
<td>Test 1.4 Case 8</td>
</tr>
<tr>
<td>09h</td>
<td>Invalid Log Page</td>
<td>Get Log Page</td>
<td>Test 1.3 Case 2 and 3</td>
</tr>
<tr>
<td>0Ah</td>
<td>Invalid Format</td>
<td>Format NVM</td>
<td>Test 1.6 Case 5</td>
</tr>
<tr>
<td>0Bh</td>
<td>Firmware Activation Requires Conventional Reset</td>
<td>Firmware Commit</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>Code</td>
<td>Description</td>
<td>Test Procedure</td>
<td>Observable Results</td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------</td>
<td>---------------------------------------------</td>
<td>---------------------------------------------------------</td>
</tr>
<tr>
<td>0Ch</td>
<td>Invalid Queue Deletion</td>
<td>Delete I/O Completion Queue</td>
<td>Test 1.4 Case 3</td>
</tr>
<tr>
<td>0Dh</td>
<td>Feature Identifier Not Saveable</td>
<td>Set Features</td>
<td>Test 5.5 Case 4</td>
</tr>
<tr>
<td>0Eh</td>
<td>Feature Not Changeable</td>
<td>Set Features</td>
<td>Test 5.5 Case 5</td>
</tr>
<tr>
<td>0Fh</td>
<td>Feature Not Namespace Specific</td>
<td>Set Features</td>
<td>Test 5.5 Case 6 and 7</td>
</tr>
<tr>
<td>10h</td>
<td>Firmware Activation Required NVM Subsystem Reset</td>
<td>Firmware Commit</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>11h</td>
<td>Firmware Activation Requires Reset</td>
<td>Firmware Commit</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>12h</td>
<td>Firmware Activation Requires Maximum Time Violation</td>
<td>Firmware Commit</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>13h</td>
<td>Firmware Activation Prohibited</td>
<td>Firmware Commit</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>14h</td>
<td>Overlapping Range</td>
<td>Firmware Commit, Firmware Image Download, Set Features</td>
<td>Test 5.5 Case 8</td>
</tr>
<tr>
<td>15h</td>
<td>Namespace Insufficient Capacity</td>
<td>Namespace Management</td>
<td>Test 9.2 Case 3</td>
</tr>
<tr>
<td>16h</td>
<td>Namespace Identifier Unavailable</td>
<td>Namespace Management</td>
<td>Test 9.2 Case 1</td>
</tr>
<tr>
<td>17h</td>
<td>Reserved</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>18h</td>
<td>Namespace Already Attached</td>
<td>Namespace Attachment</td>
<td>Test 9.3 Case 1</td>
</tr>
<tr>
<td>19h</td>
<td>Namespace Is Private</td>
<td>Namespace Attachment</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>1Ah</td>
<td>Namespace Not Attached</td>
<td>Namespace Attachment</td>
<td>Test 9.3 Case 2</td>
</tr>
<tr>
<td>1Bh</td>
<td>Thin Provisioning Not Supported</td>
<td>Namespace Management</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>1Ch</td>
<td>Controller List Invalid</td>
<td>Namespace Attachment</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>1Dh</td>
<td>Device Self-test In Progress</td>
<td>Device Self-test</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>1Eh</td>
<td>Boot Partition Write Prohibited</td>
<td>Firmware Commit</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>1Fh</td>
<td>Invalid Controller Identifier</td>
<td>Virtualization Management</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>20h</td>
<td>Invalid Secondary Controller State</td>
<td>Virtualization Management</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>21h</td>
<td>Invalid Number of Controller Resources</td>
<td>Virtualization Management</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>22h</td>
<td>Invalid Resource Identifier</td>
<td>Virtualization Management</td>
<td>Not Implemented</td>
</tr>
<tr>
<td>23h–6Fh</td>
<td>Reserved</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>70h–7Fh</td>
<td>Directive Specific</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>80h–BFh</td>
<td>I/O Command Set Specific</td>
<td>Not Implemented</td>
<td>N/A</td>
</tr>
<tr>
<td>COh–FFh</td>
<td>Vendor Specific</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Test Setup:** See Appendix A.

**Case 1: Abort Command Limit Exceeded (M)**

**Test Procedure:**
1. Determine the Abort Command Limit Exceeded value, \( n \), by examining the Identify Controller Data Structure of the DUT.
2. Configure the NVMe Host to issue \( n+1 \) Abort commands to the NVMe Controller.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is set to Abort Command Limit Exceeded, \( 03h \) for one command only.

**Case 2: Asynchronous Event Request Limit Exceeded (M)**
Test Procedure:
1. Determine the Asynchronous Event Request Limit value, n, by examining the Identify Controller Data Structure of the DUT.
2. Configure the NVMe Host to issue \( n+1 \) Asynchronous Event Request commands to the NVMe Controller.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is set to Asynchronous Event Request Limit Exceeded, 05h for one command only.

Case 3: Invalid Firmware Slot (M)

Test Procedure:
1. Determine the number of firmware slots the DUT supports by examining the Firmware Update field in the Identify Controller Data Structure.
2. Configure the NVMe Host to issue a Firmware Commit with a Slot ID of one greater than the number of slots supported by the DUT.
   a. If the DUT supports the maximum number of slots, determine if Slot 1 is Read-only. If Slot 1 is read-only, issue a Firmware Commit to Slot 1. If Slot 1 is not read-only, then this test is not applicable.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is set to Invalid Firmware Slot, 06h.

Case 4: Feature Identifier Not Saveable (M)

Test Procedure:
1. Configure the NVMe Host to issue a Get Feature command to the NVMe Controller for each supported Feature ID.
2. For each Feature indicated as Not Saveable, issue a Set Feature Command to save that feature.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is set to Feature Identifier Not Saveable, 0Dh.

Case 5: Feature Not Changeable (M)

Test Procedure:
1. Configure the NVMe Host to issue a Get Feature command to the NVMe Controller for each supported Feature ID.
2. For each Feature indicated as Not Changeable, issue a Set Feature Command to change that feature.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify if the DUT indicates that certain supported features are unchangeable, that the SCT field of the Status Field is set to Feature Not Changeable, 0Eh when the DUT responds to Set Features commands sent for that Feature. If no features are indicated as Not Changeable, then this test case is Not Applicable.
Case 6: Feature Not Namespace Specific IV=1 (M)

**Test Procedure:**
1. Configure the NVMe Host to issue a Set Feature – Interrupt Vector Configuration command to the NVMe Controller with IV=1 and CD=0.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is set to Feature Not Namespace Specific, 0Fh.

Case 7: Overlapping Range (M)

**Test Procedure:**
1. Configure the NVMe Host to issue a Set Feature command to the NVMe Controller with an overlapping LBA range.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is set to Overlapping Range, 14h.

**Possible Problems:** The NVMe specification does not explicitly state the exact conditions for when an NVMe Controller should use some of the defined Status Codes. Such status codes cannot be tested. Additionally, some of the Status Codes can only be used for optional commands which the NVMe controller may or may not support.
Test 5.6 – Media and Data Integrity Errors Definition (M)

**Purpose:** To verify that an NVMe Controller can properly return the status for the command in the completion queue entry.

**References:**
NVMe Specification 4.5.1.2.3

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** June 24, 2015

**Discussion:** Completion queue entries with a Status Code Type of Media and Data Integrity Errors (02h) indicate a media specific error that occurred in the NVM or data integrity type errors. The Status Code values for the Media and Data Integrity Errors Status Type are defined in Table 18 and Table 19.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h – 7Fh</td>
<td>Reserved</td>
</tr>
<tr>
<td>80h – BFh</td>
<td>I/O Command Set Specific</td>
</tr>
<tr>
<td>C0h – FFh</td>
<td>Vendor Specific</td>
</tr>
</tbody>
</table>

Table 18 – Media and Data Integrity Error Values

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>80h</td>
<td><strong>Write Fault:</strong> The write data could not be committed to the media.</td>
</tr>
<tr>
<td>81h</td>
<td><strong>Unrecovered Read Error:</strong> The read data could not be recovered from the media.</td>
</tr>
<tr>
<td>82h</td>
<td><strong>End-to-end Guard Check Error:</strong> The command was aborted due to an end-to-end guard check failure.</td>
</tr>
<tr>
<td>83h</td>
<td><strong>End-to-end Application Tag Check Error:</strong> The command was aborted due to an end-to-end application tag check failure.</td>
</tr>
<tr>
<td>84h</td>
<td><strong>End-to-end Reference Tag Check Error:</strong> The command was aborted due to an end-to-end reference tag check failure.</td>
</tr>
<tr>
<td>85h</td>
<td><strong>Compare Failure:</strong> The command failed due to a miscompare during a Compare command.</td>
</tr>
<tr>
<td>86h</td>
<td><strong>Access Denied:</strong> Access to the namespace and/or LBA range is denied due to lack of access rights. Refer to TCG SIIS.</td>
</tr>
<tr>
<td>87h</td>
<td><strong>Deallocated or Unwritten Logical Block:</strong> The command failed due to an attempt to read from an LBA range containing a deallocated or unwritten logical block.</td>
</tr>
<tr>
<td>88h – BFh</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Table 19 – Media and Data Integrity Error Values, NVM Command Set

**Test Setup:** See Appendix A.

**Test Procedure:**
1. For each of the Status Code values defined in Table 18 and Table 19, configure the NVMe Host to issue a command to the NVMe Controller which will cause the controller to return the Status Code in the completion queue entry for the command.

**Observable Results:**
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the SCT field of the Status Field is set to 2h. Verify that the SC field of the Status field matches the expected Status Code.
Possible Problems: The NVMe specification does not explicitly state the exact conditions for when an NVMe Controller should use some of the defined Status Codes. Such status codes cannot be tested. Additionally, some of the Status Codes can only be used for optional commands which the NVMe controller may or may not support.
Group 6: Controller Architecture

Overview:

This section describes a method for performing conformance verification for NVMe products implementing the NVMe Controller Architecture.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 6.1 – Controller Level Reset – Conventional Reset (IP)

Purpose: To verify that an NVMe Controller performs the proper actions when a Conventional Reset occurs.

References:
- NVMe Specification 7.3.2

Resource Requirements:
- Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 24, 2015

Discussion: When a Controller Level Reset occurs, the Host and Controller are required to take specific action.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Device to perform a Conventional Controller Level Reset. Repeat this for each of the following cases:
   a. PCI Express Warm reset (if there is a means provided by the vendor)
   b. PCI Express Cold reset
2. When the reset is complete, configure the NVMe Host to issue a Write and then a Read command to the NVMe Controller.

Observable Results:
1. Verify that the NVMe Controller is able to properly execute NVMe Write and Read commands after the reset is complete.
2. Verify that the NVMe Controller performs the following actions when each reset case defined above is initiated:
   a. The controller stops processing any outstanding Admin or I/O commands.
   b. All I/O Submission Queues are deleted.
   c. All I/O Completion Queues are deleted.
   d. The controller is brought to an Idle state. When this is complete, CSTS.RDY is cleared to ‘0’.
   e. All controller registers defined in section 3 of the NVMe Specification and internal controller state are reset.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 6.2 – Controller Level Reset – Function Level Reset (M)

Purpose: To verify that an NVMe Controller performs the proper actions when a Function Level Reset occurs.

References:
NVMe Specification 7.3.2

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 16, 2016

Discussion: When a Controller Level Reset occurs, the Host and Controller are required to take specific action. Support for the Function Level Reset mechanism is indicated in the Function Level Reset Capability (FLRC) field (bit 28) of the PCI Express Device Capabilities (PXDCAP) (offset PXCAP + 4h) PCI Express Register. All NVMe Controllers must support Function Level Reset and so this register value should be set to ‘1’ for all NVMe Controllers.

A Function Level Reset is initiated by the NVMe Host by writing a value of ‘1’ to the Initiate Function Level Reset field (bit 15) of the PCI Express Device Control (PXDC) (offset PXCAP + 8h) PCI Express Register. The value read by software from this field shall always be ‘0’.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the PXDCAP.FLRC PCI Express register field.
2. Configure the NVMe Host to read the Initiate Function Level Reset field of the PXDC PCI Express register.
3. Configure the NVMe Host to write a value of ‘1’ to the Initiate Function Level Reset field of the PXDC PCI Express register in order to initiate a Function Level Reset.
4. When the reset is complete, configure the NVMe Host to issue a Write command to the NVMe Controller.

Observable Results:
1. Verify that the value read from the PXDCAP.FLRC PCI Express register field is ‘1’ to indicate support for the Function Level Reset mechanism.
2. Verify that the value read from the Initiate Function Level Reset field of the PXDC PCI Express register is ‘0’.
3. Verify that the NVMe Controller is able to properly execute the Write command after the reset is complete:
   a. The controller stops processing any outstanding Admin or I/O commands.
   b. All I/O Submission Queues are deleted.
   c. All I/O Completion Queues are deleted.
   d. The controller is brought to an Idle state. When this is complete, CSTS.RDY is cleared to ‘0’.
   e. All controller registers defined in section 3 of the NVMe Specification and internal controller state are reset.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 6.3 – Controller Level Reset – Controller Reset (M, OF-IP)

Purpose: To verify that an NVMe Controller performs the proper actions when a Controller Reset occurs.

References:
NVMe Specification 7.3.2

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 24, 2015

Discussion: When a Controller Level Reset occurs, the Host and Controller are required to take specific action.

A Controller Reset is initiated when the CC.EN controller register field transitions from ‘1’ to ‘0’. This is performed by the NVMe Host by writing a value of ‘0’ to the CC.EN while the CC.EN field is set to ‘1’.

Test Setup: See Appendix A.

Test Procedure
1. Configure the NVMe Host to write a value of ‘0’ to the CC.EN controller register field.
2. When the reset is complete, configure the NVMe Host to issue a Write and then a Read command to the NVMe Controller.

Observable Results:
1. Verify that the NVMe Controller is able to properly execute NVMe Write and Read commands after the reset is complete.
2. Verify that the NVMe Controller performs the following actions when the Controller Reset is initiated:
   a. The controller stops processing any outstanding Admin or I/O commands.
   b. All I/O Submission Queues are deleted.
   c. All I/O Completion Queues are deleted.
   d. The controller is brought to an Idle state. When this is complete, CSTS.RDY is cleared to ‘0’.
   e. The Admin Queue registers (AQA, ASQ, or ACQ) are not reset as part of a controller reset. All other controller registers defined in section 3 of the NVMe Specification and internal controller state are reset.

Possible Problems: None.
Test 6.4 – Controller Level Reset – NVM Subsystem Reset (M)

Purpose: To verify that an NVMe Controller performs the proper actions when an NVM Subsystem Reset occurs.

References:
NVMe Specification 7.3.1 and 7.3.2

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 27, 2016

Discussion: When a Controller Level Reset occurs, the Host and Controller are required to take specific action.

An NVM Subsystem Reset is initiated when:
1. Power is applied to the NVM System,
2. A value of 4E564D65h (“NVMe”) is written to the NSSR.NSSRC controller register field, or
3. A vendor specific event occurs.

When an NVM Subsystem Reset occurs, the entire NVM subsystem is reset. This includes the initiation of a Controller Level Reset on all controllers that make up the NVM subsystem and a transition to the Detect LTSSM state by all PCI Express ports of the NVM subsystem.

The occurrence of an NVM Subsystem Reset while power is applied to the NVM subsystem is reported by the initial value of the CSTS.NSSRO field following the NVM Subsystem Reset. This field may be used by host software to determine if the sudden loss of communication with a controller was due to an NVM Subsystem Reset or some other condition.

This test is only applicable if the CAP.NSSRS field is set ‘1’ to indicate support for writing to the NSSR.NSSRC field.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the NVMe Host to read the CAP.NSSRS field to determine if the DUT supports writing to the NSSR.NSSRC field. If the NSSRS field is cleared to ‘0’, the test is not applicable. If the CAP.NSSRS field is set to ‘1’, continue to step 3.
2. Configure the NVMe host to read the CSTS.NSSRO register value, and record the value. If the value is not zero, perform a power cycle of the DUT and restart the test.
3. Configure the NVMe host to write a value of 4E564D65h (“NVMe”) to the NSSR.NSSRC field.
4. When the reset is complete, the PCIe link is reestablished, the NVMe controller is enabled and an Identify is performed.

Observable Results:
1. Verify that the NVMe Controller is able to properly execute NVMe Identify command after the reset is complete.
2. Read the CSTS.NSSRO register value and ensure that it is set to 1.
3. Verify that the NVMe Controller performs the following actions when the NVM Subsystem Reset is initiated:
   a. The controller stops processing any outstanding Admin or I/O commands.
   b. All I/O Submission Queues are deleted.
   c. All I/O Completion Queues are deleted.
   d. The controller is brought to an Idle state. When this is complete, CSTS.RDY is cleared to ‘0’.
   e. All controller registers defined in section 3 of the NVMe Specification and internal controller state are reset.

Possible Problems: The DUT may or may not support NVM Subsystem Reset as it is an optional NVMe feature.
Overview:

This section describes a method for performing conformance verification for NVMe products implementing NVMe Reservations. These tests are not applicable to devices that do not claim to support reservations.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 7.1 – Reservation Report Command (M)

Purpose: To determine if an NVMe Controller properly reports the status of a reservation when processing a Reservation Report command.

References:
NVMe Specification 8.8, 5.14.1.15, 6.13

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 15, 2018

Discussion: A host may determine the current reservation status associated with a namespace by executing a Reservation Report command. The Reservation Report command returns a Reservation Status data structure to memory that describes the registration and reservation status of a namespace.

The size of the Reservation Status data structure is a function of the number of controllers in the NVM Subsystem that are associated with hosts that are registrants of the namespace (i.e., there is a Registered Controller data structure for each such controller).

The command uses Command Dword 10. If the command uses PRPs for the data transfer, then PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Test Setup: See Appendix A.

Case 1: No Registrants (M)

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      ii. Configure the NVMe Host to issue a Get Features command with the Reservation Persistence feature to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Type (RTYPE) field of the Reservation Status data structure is set to 0 to indicate that no reservation is held on the namespace.
3. Verify that the Number of Registered Controllers (REGCTL) field of the Reservation Status data structure is set to 0 to indicate that no hosts are registrants of the namespace.
4. Verify that the Persist Through Power Loss State (PTPLS) field of the Reservation Status data structure is set to the same value of the Persist Through Power Loss (PTPL) field of Command Dword 0 of the completion queue entry for the Get Features command with Reservation Persistence feature.
Case 2: Host is a Registrant (FYI)

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace, and perform a Reservation Acquire to that namespace.
      ii. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      iii. Configure the NVMe Host to issue an Identify command specifying CNS value 01h to the NVMe Controller in order to receive back the Identify Controller data structure for that controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Generation (GEN) field of the Reservation Status data structure is incremented for each Reservation Register command which the host issues to an NVMe Controller.
3. Verify that the Reservation Type (RTYPE) field of the Reservation Status data structure is set to not 0 to indicate that a reservation is held on the namespace.
4. Verify that the Number of Registered Controllers (REGCTL) field of the Reservation Status data structure is set to the number of controllers for which the host has set its Host Identifier for to indicate the number of controllers associated with the host and that the host is a registrant of the namespace.
5. Verify that the number of Registered Controller data structures returned as part of the Reservation Status data structure is exactly equal to the value stored in the REGCTL field.
6. Verify that the Controller ID (CNTLID) field of the Registered Controller data structures matches the CNTLID field in the Identify Controller data structure for that controller.
7. Verify that the Reservation Status (RCSTS) field of the Registered Controller data structures have bit 0 cleared to not '0' to indicate that the host associated with the controller holds a reservation on the namespace.
8. Verify that the Host Identifier (HOSTID) field of the Registered Controller data structures is set to the same value which the host set for its Host Identifier in the Set Features command.
9. Verify that the Reservation Key (RKEY) field of the Registered Controller data structures is set to the same value which the host set for its reservation key in the Reservation Register command.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 7.2 – Reservation Registration (IP)

Purpose: To determine if an NVMe Controller properly supports registering hosts via the Reservation Register command.

References:
NVMe Specification 8.8, 5.14.1.15, 6.11

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 15, 2018

Discussion: Prior to establishing a reservation on a namespace, a host shall become a registrant of that namespace by registering a reservation key. Registering a reservation key with a namespace creates an association between a host and a namespace. A host need only register on a single controller in order to become a registrant of the namespace on all controllers in the NVM Subsystem that have access to the namespace and are associated with the host.

A host registers a reservation key by executing a Reservation Register command on the namespace with Reservation Register Action (RREGA) field set to 000b (i.e., Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field.

The Reservation Register command uses Command Dword 10 and a Reservation Register data structure in memory. If the command uses PRPs for the data transfer, then the PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Test Setup: See Appendix A.

Case 1: Basic Operation (IP)

Test Procedure:
1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e., Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host was successfully registered to the namespace.

Case 2: Re-registration (IP)

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.

2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e., Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue an additional Reservation Register command with Register Reservation Key action and the same reservation key to the NVMe Controller.
      iii. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      iv. Configure the NVMe Host to issue an additional Reservation Register command with Register Reservation Key action and a different reservation key to the NVMe Controller.
      v. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated completion queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host was successfully registered to the namespace.
3. Verify that the completion queue entry for the final Reservation Register command (with the different reservation key) indicates status Reservation Conflict.
4. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the final Reservation Report command indicates that the reservation key for the host was not changed.

Case 3: Replace Registration Key (IP)
A host that is a registrant of a namespace may replace its existing reservation key by executing a Reservation Register command on the namespace with the RREGA field set to 010b (i.e., Replace Reservation Key), supplying the current reservation key in the Current Reservation Key (CRKEY) field, and the new reservation key in the NRKEY field. If the contents of the CRKEY field do not match the key currently associated with the host, then the Reservation Register command shall be aborted with status of Reservation Conflict. A host may replace its reservation key without regard to its registration status or current reservation key value by setting the Ignore Existing Key (IEKEY) bit to ‘1’ in the Reservation Register command. Setting the IEKEY bit to ‘1’ causes the Reservation Register command to succeed regardless of the value of the CRKEY field (i.e., the current reservation key is not checked).

Replacing a reservation key has no effect on any reservation that may be held on the namespace.

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e., Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Register command with the RREGA field set to 010b (i.e., Replace Reservation Key), supplying the current reservation key in the
Current Reservation Key (CRKEY) field, and a new reservation key in the NRKEY field to the NVMe Controller for the namespace in order to associate a new reservation key with the registrant of the namespace.

iii. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

iv. Configure the NVMe Host to issue a Reservation Register command with the Replace Reservation Key action, supplying any key value that is not the current reservation key in the CRKEY field, and a new reservation key in the NRKEY field to the NVMe Controller. Also, set the RType to 2 using the Reservation Acquire Command.

v. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

vi. Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field to the NVMe Controller in order for the host to acquire a reservation on the namespace.

vii. Configure the NVMe Host to issue a Reservation Register command with the Register Reservation Key action, supplying a new reservation key in the New Reservation Key (NRKEY) field, and setting the IEKEY bit to ‘1’ to the NVMe Controller for the namespace in order to make the host a registrant of that namespace with a different reservation key.

viii. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command after the second Reservation Registration command indicates that the host successfully changed its reservation key.
3. Verify that the completion queue entry for the third Reservation Register command (with the invalid current reservation key) indicates status Reservation Conflict.
4. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command after the third Reservation Register command indicates that the reservation key associated with the host did not change.
5. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command after the fourth Reservation Register command (with the IEKEY set) indicates that the host successfully changed its reservation key and that it still holds the reservation it previously acquired.

Case 4: Multiple Hosts (IP) Dual Port Devices Only
There are no restrictions on the reservation key value used by hosts with different Host Identifiers. For example, multiple hosts may all register the same reservation key value.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:
1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying the same reservation key that NVMe Host 1 used in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
6. Configure NVMe Host 1 to issue a Reservation Report command to NVMe Controller 1.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that both hosts were successfully registered to the namespace.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 7.3 – Unregistering (M)

**Purpose:** To determine if an NVMe Controller properly supports reservations.

**References:**
NVMe Specification 8.8, 5.14.1.15, 6.11

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** August 29, 2017

**Discussion:** A host that is a registrant of a namespace may unregister with the namespace by executing a Reservation Register command on the namespace with the Reservation Register Action (RREGA) field set to 0001b (i.e., Unregister Reservation Key) and supplying its current reservation key in the CRKEY field. If the contents of the CRKEY field do not match the key currently associated with the host or if the host is not a registrant, then the command shall be aborted with a status of Reservation Conflict. A host may unregister without regard to its current reservation key value by setting the IEKEY bit to 1 in the Reservation Register command.

Successful completion of an unregister operation causes the host to no longer be a registrant of that namespace.

Unregistering due to preemption or a registration clear is verified in subsequent tests.

**Test Setup:** See Appendix A.

**Case 1: Unregistering with Reservation Register Command (M)**

**Test Procedure:**
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Register command with the Unregister Reservation Key action and supplying its current reservation key in the CRKEY field to the NVMe Controller for the namespace in order to unregister the host as a registrant of that namespace.
      iii. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated completion queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host was successfully unregistered from the namespace.
Case 2: Unregistering due to Preemption (M)Dual Port Devices Only

If a preemption occurs and there is no reservation held on the namespace, then execution of the Reservation Acquire command with Preempt action causes registrants whose reservation key match the value of the PRKEY field to be unregistered.

See the Preempting a Reservation test for more information on reservation preemption.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:

1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
6. Configure NVMe Host 2 to issue a Reservation Acquire command, setting the RACQA field to 001b (Preempt), and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the Preempt Reservation Key (PRKEY) field to the current reservation key associated with NVMe Host 1 to NVMe Controller 2 in order to preempt the NVMe Host 1’s reservation.
7. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.

Observable Results:

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that NVMe Host 2 was not unregistered from the namespace and NVMe Host 1 was successfully unregistered from the namespace.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 7.4 – Acquiring a Reservation (M)

Purpose: To determine if an NVMe Controller properly allows acquisition of reservations via the Reservation Register command.

References:
NVMe Specification 8.8, 5.14.1.15, 6.10

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: April 1, 2016

Discussion: In order for a host to obtain a reservation on a namespace, it shall be a registrant of that namespace. A registrant obtains a reservation by executing a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), and supplying the current reservation key associated with the host to the Current Reservation Key (CRKEY) field.

The Reservation Acquire command uses Command Dword 10 and a Reservation Acquire data structure in memory. If the command uses PRPs for the data transfer, then the PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are used.

Test Setup: See Appendix A.

Case 1: Basic Operation (M)

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue an Identify command specifying CNS value 00h to the NVMe Controller in order to receive back the Identify Namespace data structure for the namespace.
      iii. For each reservation type supported by the namespace based on the RESCAP field of the Identify Namespace data structure for the namespace:
          1. Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to the reservation type to the NVMe Controller in order for the host to acquire a reservation on the namespace with the reservation type.
          2. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
          3. Configure the NVMe Host to issue a Reservation Release command, setting the Reservation Release Action (RRELA) field to 000b (i.e. Release), setting the Reservation Type (RTYPE) field to the type of the reservation being released, and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field.
Reservation Key (CRKEY) field to the NVMe Controller in order to release the reservation held by the host.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host successfully acquired the reservation with the associated reservation type.

Case 2: Error Conditions (M)
If the CRKEY value does not match that used by the registrant to register with the namespace or the host is not a registrant, the command shall be aborted with status Registration Conflict. A Host may acquire a reservation without regard to its current reservation key value by setting the Ignore Existing Key (IEKEY) bit to ‘1’ in the command.

If a reservation holder attempts to obtain a reservation of a different type on a namespace for which it is already the reservation holder, then the command shall be aborted with status Reservation Conflict. It is not an error for a reservation holder to attempt to obtain a reservation of the same type on a namespace for which it is already the reservation holder.

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. RES_ACQ1: Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying a random reservation key in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to the NVMe Controller.
      ii. RES_REP1: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      iii. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      iv. RES_ACQ2: Configure the NVMe Host to issue a Reservation Acquire command, setting the Acquire action, supplying any reservation key other than the reservation key currently associated with the host in the CRKEY field, and setting the RTYPE field to a reservation type supported by the namespace to the NVMe Controller.
      v. RES_REP2: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      vi. RES_ACQ3: Configure the NVMe Host to issue a Reservation Acquire command, setting the Acquire action, supplying any reservation key other than the reservation key currently associated with the host in the CRKEY field, setting the IEKEY bit to ‘1’, and setting the RTYPE field to a reservation type supported by the namespace to the NVMe Controller in order for the host to acquire a reservation on the namespace.
      vii. RES_REP3: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      viii. RES_ACQ4: Configure the NVMe Host to issue a Reservation Acquire command, setting the Acquire action, supplying the reservation key currently associated with the host in the CRKEY field, and setting the RTYPE field to a different reservation type supported by the namespace to the NVMe Controller.
namespace than the one used for the current reservation held by the host to the NVMe Controller.
ix. RES_REP4: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
x. RES_ACQ5: Configure the NVMe Host to issue a Reservation Acquire command, setting the Acquire action, supplying the reservation key currently associated with the host in the CRKEY field, and setting the RTYPE field to the same reservation type used for the current reservation held by the host to the NVMe Controller.
xi. RES_REP5: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the completion queue entry for RES_ACQ1 indicates status Reservation Conflict.
3. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP1 indicates that the host does not hold any reservations.
4. Verify that the completion queue entry for RES_ACQ2 indicates status Reservation Conflict.
5. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP2 indicates that the host does not hold any reservations.
6. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP3 indicates that the host successfully acquired a reservation with the namespace.
7. Verify that the completion queue entry for RES_ACQ4 indicates status Reservation Conflict.
8. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP4 indicates that the host still holds its reservation with the namespace with the same reservation type.
9. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP5 indicates that the host still holds its reservation with the namespace with the same reservation type.

Case 3: Multiple Hosts (M) Dual Port Devices Only

Only one reservation is allowed at a time on a namespace. If a registrant attempts to obtain a reservation on a namespace that already has a reservation holder, then the command is aborted with status Reservation Conflict.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:
1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
6. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to NVMe Controller 1.
Configure NVMe Host 2 to issue a Reservation Acquire command with the Acquire action, supplying the reservation key currently associated with NVMe Host 2 in the CRKEY field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to NVMe Controller 2.

Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the completion queue entry for the Reservation Acquire command sent by NVMe Host 2 indicates status Reservation Conflict.
3. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that NVMe Host 1 holds a reservation on the namespace and that NVMe Host 2 does not.

**Possible Problems:** A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 7.5 – Releasing a Reservation (M)

Purpose: To determine if an NVMe Controller properly releases reservations.

References:
NVMe Specification 8.8, 5.14.1.15, 6.12

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: April 1, 2016

Discussion: A host releases a reservation by executing a Reservation Release command, setting the Reservation Release Action (RRELA) field to 000b (i.e. Release), setting the Reservation Type (RTYPE) field to the type of the reservation being released, and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field.

The Reservation Release command uses Command Dword 10 and a Reservation Release data structure in memory. If the command uses PRPs for the data transfer, then the PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Reservation release due to preemption or a registration clear is verified in subsequent tests.

Test Setup: See Appendix A.

Case 1: Release with Reservation Release Command (FYI)

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to the NVMe Controller in order for the host to acquire a reservation on the namespace with the reservation type.
      iii. Configure the NVMe Host to issue a Reservation Release command, setting the Reservation Release Action (RRELA) field to 000b (i.e. Release), setting the Reservation Type (RTYPE) field to the type of the reservation being released, and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field to the NVMe Controller in order to release the reservation held by the host.
   iv. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.

2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host successfully released the reservation.

**Case 2: Reservation Release Command Error Conditions (FYI)**

If the CRKEY value does not match that used by the registrant to register with the namespace, the command shall be aborted with status Registration Conflict. A host may release a reservation without regard to its current reservation key value by setting the Ignore Existing Key (IEKEY) bit to ‘1’ in the command. If the RTYPE field does not match the type of the current reservation, then the command shall be completed with status Invalid Field in Command.

**Test Procedure:**

1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable.

2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to the NVMe Controller in order for the host to acquire a reservation on the namespace with the reservation type.
      iii. RES_REL1: Configure the NVMe Host to issue a Reservation Release command, setting the Reservation Release Action (RRELA) field to 000b (i.e. Release), setting the Reservation Type (RTYPE) field to the type of the reservation being released, and supplying any reservation key other than the current reservation key associated with the host in the Current Reservation Key (CRKEY) field to the NVMe Controller.
      iv. RES_REP1: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      v. RES_REL2: Configure the NVMe Host to issue a Reservation Release command with the Release action, setting the RTYPE field to any reservation type other than the type of the reservation being released, supplying any reservation key other than the current reservation key associated with the host in the CRKEY field to the NVMe Controller.
      vi. RES_REP2: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      vii. RES_REL3: Configure the NVMe Host to issue a Reservation Release command with the Release action, setting the Reservation Type (RTYPE) field to the type of the reservation being released, supplying any reservation key other than the current reservation key associated with the host in the CRKEY field, and setting the IEKEY bit to ‘1’ to the NVMe Controller in order to release the reservation held by the host.
      viii. RES_REP3: Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.

2. Verify that the completion queue entry for RES_REL1 indicates status Reservation Conflict.

3. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP1 indicates that the host still holds a reservation with the namespace.
4. Verify that the completion queue entry for RES_REL2 indicates status Invalid Field in Command.
5. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP2 indicates that the host still holds a reservation with the namespace.
6. Verify that the Reservation Status data structure returned by the NVMe Controller after completing RES_REP3 indicates that the host successfully released the reservation.

Case 3: Multiple Hosts (M) Dual Port Devices Only
An attempt by a registrant to release a reservation using the Reservation Release command in the absence of a reservation held on the namespace or when the host is not the reservation holder shall cause the command to complete successfully, but shall have no effect on the controller or namespace.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
6. Configure NVMe Host 1 to issue a Reservation Release command, setting the Reservation Release Action (RRELA) field to 000b (i.e. Release), setting the Reservation Type (RTYPE) field to any reservation type, and supplying the current reservation key associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field to NVMe Controller 1.
7. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to NVMe Controller 1.
8. Configure NVMe Host 2 to issue a Reservation Release command with the Release action, setting the RTYPE field to the type of the reservation which NVMe Host 1 holds, and supplying the current reservation key associated with NVMe Host 1 in the CRKEY field to NVMe Controller 2.
9. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the completion queue entry for the Reservation Release command sent by NVMe Host 1 indicates status Success.
3. Verify that the completion queue entry for the Reservation Release command sent by NVMe Host 2 indicates status Success.
4. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that NVMe Host 1 holds a reservation on the namespace and that NVMe Host 2 does not.
Case 4: Release Due to Unregister (FYI)
If a host is the last remaining reservation holder (i.e. the Reservation Type is Write Exclusive - All Registrants or Exclusive Access - All Registrants) or is the only reservation holder, then the reservation is released when the host unregisters.

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations, then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to 01h (Write Exclusive Access) to the NVMe Controller in order for the host to acquire a reservation on the namespace.
      iii. Configure the NVMe Host to issue a Reservation Register command with the Unregister Reservation Key action and supplying its current reservation key in the CRKEY field to the NVMe Controller for the namespace in order to unregister the host as a registrant of that namespace.
      iv. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host was successfully unregistered from the namespace and that the reservation held by the host on the namespace was released.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 7.6 – Preempting a Reservation (M)

Purpose: To determine if an NVMe Controller properly preempts reservations.

References:
NVMe Specification 8.8, 5.14.1.15, 6.10

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: April 1, 2016

Discussion: A host that is a registrant may preempt a reservation and/or registration by executing a Reservation Acquire command, setting the Reservation Acquire (RACQA) field to 001b (Preempt), and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field. The preempt actions that occur are dependent on the type of reservation held on the namespace, if any, and the value of the Preempt Reservation Key (PKEY) field in the command.

The case of preemption when no reservation is held is covered in the Unregistering test.

Test Setup: See Appendix A.

Case 1: Write Exclusive - All Registrants or Exclusive Access - All Registrants (M) Dual Port Devices Only
If the existing reservation type is Write Exclusive - All Registrants or Exclusive Access - All Registrants, then the actions performed by the command depend on the value of the PRKEY field as follows:

1. If the PRKEY field value is zero, then the following occurs as an atomic operation:
   a. All registrants other than the host that issued the command are unregistered,
   b. The reservation is released, and
   c. A new reservation is created for the host of the type specified by the Reservation Type (RTYPE) field in the command.

2. If the PRKEY value is non-zero, then each registrant whose reservation key matches the value of the PRKEY field are unregistered.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:
1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
6. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to Write Exclusive - All Registrants or Exclusive Access - All Registrants to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation on the namespace.
7. Configure NVMe Host 2 to issue a Reservation Acquire command, setting the RACQA field to 001b (Preempt), and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the Preempt Reservation Key (PRKEY) field to 0 to NVMe Controller 2 in order to preempt NVMe Host 1's reservation.
8. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.
9. Configure NVMe Host 2 to issue a Reservation Release command, setting the Reservation Release Action (RRELA) field to 000b (i.e. Release), setting the Reservation Type (RTYPE) field to the type of the reservation being released, and supplying the current reservation key associated with NVMe Host 2 in the Current Reservation Key (CRKEY) field to NVMe Controller 2 in order to release the reservation held by NVMe Host 2.
10. Configure NVMe Host 1 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
11. Configure NVMe Host 1 to issue a Reservation Acquire command with the Acquire action, supplying the reservation key currently associated with NVMe Host 1 in the CRKEY field, and setting the RTYPE field to Write Exclusive - All Registrants or Exclusive Access - All Registrants to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation on the namespace.
12. Configure NVMe Host 2 to issue a Reservation Acquire command with the Preempt action, and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the PRKEY field to the current reservation key associated with NVMe Host 1 to NVMe Controller 2 in order to preempt NVMe Host 1's reservation.
13. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the first Reservation Report command indicates that NVMe Host 2 was not unregistered from the namespace, NVMe Host 1 no longer holds a reservation and was successfully unregistered from the namespace, and that NVMe Host 2 holds a reservation of the type specified in the Reservation Acquire command with Preempt action.
3. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the second Reservation Report command indicates that NVMe Host 2 was not unregistered from the namespace and NVMe Host 1 was successfully unregistered from the namespace.

Case 2: Other Registration Types (M) Dual Port Devices Only

If the existing reservation type is not Write Exclusive - All Registrants and not Exclusive Access - All Registrants (i.e. Write Exclusive, Exclusive Access, Write Exclusive - Registrants Only, or Exclusive Access - Registrants Only), then the actions performed by the command depend on the value of the PRKEY as follows:
1. If the PRKEY field value matches the reservation key of the current reservation key of the current reservation holder, then the following occur as an atomic operation:
   a. The reservation holder is unregistered,
   b. The reservation is released, and
   c. A new reservation is created of the type specified by the Reservation Type (RTYPE) field in the command for the host as the reservation key holder.
2. If the PRKEY value does not match that of the current reservation holder and is not equal to zero, then each registrant whose reservation key matches the value of the value of the PRKEY field are unregistered.
3. If the PRKEY value does not match that of the current reservation holder and is equal to zero, then the command shall be aborted with status Invalid Field in Command.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:
1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
6. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to Write Exclusive, Exclusive Access, Write Exclusive - Registrants Only, or Exclusive Access - Registrants Only to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation on the namespace.
7. Configure NVMe Host 2 to issue a Reservation Register command, setting the RACQA field to 001b (Preempt), and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the Preempt Reservation Key (PRKEY) field to the reservation key associated with NVMe Host 1 to NVMe Controller 2 in order to preempt NVMe Host 1’s reservation.
8. Configure NVMe Host 2 to issue a Reservation Acquire command with the Acquire action, supplying the reservation key currently associated with NVMe Host 1 in the CRKEY field, and setting the RTYPE field to Write Exclusive, Exclusive Access, Write Exclusive - Registrants Only, or Exclusive Access - Registrants Only to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation on the namespace.
9. Configure NVMe Host 2 to issue a Reservation Acquire command with the Acquire action, supplying the reservation key currently associated with NVMe Host 1 in the CRKEY field, and setting the RTYPE field to Write Exclusive, Exclusive Access, Write Exclusive - Registrants Only, or Exclusive Access - Registrants Only to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation on the namespace.
10. Configure NVMe Host 1 to issue a Reservation Acquire command with the Preempt action, and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the PRKEY field to a reservation key other than NVMe Host 1’s reservation keys to NVMe Controller 2.
11. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.
12. Configure NVMe Host 2 to issue a Reservation Acquire command with the Preempt action, and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the PRKEY field to a reservation key other than NVMe Host 2’s reservation keys to NVMe Controller 2.
13. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.
14. Configure NVMe Host 1 to issue a Reservation Acquire command with the Acquire action, supplying the reservation key currently associated with NVMe Host 1 in the CRKEY field, and setting the RTYPE field to Write Exclusive, Exclusive Access, Write Exclusive - Registrants Only, or Exclusive Access - Registrants Only to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation on the namespace.
15. Configure NVMe Host 2 to issue a Reservation Acquire command with the Preempt action, and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the PRKEY field to 0 to NVMe Controller 2 in order to preempt NVMe Host 1’s reservation.
16. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the first Reservation Report command indicates that NVMe Host 2 was not unregistered from the namespace, NVMe Host 1 no longer holds a reservation and was successfully unregistered from the namespace, and that NVMe Host 2 holds a reservation of the type specified in the Reservation Acquire command with Preempt action.
3. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the second Reservation Report command indicates that both hosts are still registered and NVMe Host 1 still holds a reservation on the namespace.

4. Verify that the completion queue entry for the third Reservation Acquire command with Preempt action indicates status Invalid Field in Command.

5. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the third Reservation Report command indicates that both hosts are still registered and NVMe Host 1 still holds a reservation on the namespace.

Case 3: Self-preemption (M) Dual Port Devices Only
A reservation holder may preempt itself using the above mechanism. When a host preempts itself, the following occurs as an atomic operation:
1. Registration of the host is maintained,
2. The reservation is released, and
3. A new reservation is created for the host of the type specified by the RTYPE field.

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to the NVMe Controller in order for the host to acquire a reservation on the namespace with the reservation type.
      iii. Configure the NVMe Host to issue a Reservation Acquire command, setting the RACQA field to 001b (Preempt), and supplying the current reservation key associated with the host in the CRKEY field and setting the Preempt Reservation Key (PRKEY) field to 0 to the NVMe Controller in order to preempt the host's reservation.
      iv. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host was not unregistered from the namespace and that the host holds a reservation of the type specified in the Reservation Acquire command with Preempt action.

Case 4: Preempt and Abort (M) Dual Port Devices Only
A host may abort commands as a side effect of preempting a reservation by executing a Reservation Acquire command and setting the RACQA field to 010b (Preempt an Abort). The behavior of such a command is exactly the same as that described above with the RACQA field set to 001b (Preempt), except that commands that target the namespace are aborted by controllers associated with hosts whose reservation or registration is preempted. As with the Abort Admin command, abort as a side effect of preempting a reservation is best effort; the commands to abort may have already completed, currently be in execution, or may be deeply queued.
This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
6. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation on the namespace.
7. Configure NVMe Host 1 to issue 10 NVMe Read commands to NVMe Controller 1.
8. Configure NVMe Host 2 to issue a Reservation Acquire command, setting the RACQA field to 010b (Preempt and Abort), and supplying the current reservation key associated with the NVMe Host 2 in the CRKEY field and setting the Preempt Reservation Key (PRKEY) field to the reservation key associated with NVMe Host 1 to NVMe Controller 2 in order to preempt NVMe Host 1’s reservation.
9. Configure NVMe Host 2 to issue a Reservation Report command to NVMe Controller 2.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Determine the status of each of the NVMe commands issued by NVMe Host 1.
3. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the proper actions were taken according to the reservation type acquired by NVMe Host 1.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 7.7 – Clearing a Reservation (M)

Purpose: To determine if an NVMe Controller properly supports clearing reservations.

References:
NVMe Specification 8.8, 5.14.1.15, 6.12

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: April 1, 2016

Discussion: A host that is a registrant may clear a reservation (i.e. force the release of a reservation held on the namespace and unregister all registrants) by executing a Reservation Release command, setting the Reservation Release Action (RRELA) field to 001b (i.e. Clear), and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field.

When a reservation is cleared, the following occur as an atomic operation:
1. the reservation is released, and
2. All registrants are unregistered from the namespace.

Test Setup: See Appendix A.

Case 1: Basic Operation with Reservation Release Command (M)

Test Procedure:
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      ii. Configure the NVMe Host to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to a reservation type supported by the namespace to the NVMe Controller in order for the host to acquire a reservation on the namespace with the reservation type.
      iii. Configure the NVMe Host to issue a Reservation Release command, setting the Reservation Release Action (RRELA) field to 001b (i.e. Clear) and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field to the NVMe Controller in order to clear the reservation.
     iii. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the Reservation Report command indicates that the host no longer holds a reservation on the namespace and was successfully unregistered from the namespace.
Case 2: Error Conditions (M)

If the CRKEY value does not match that used by the host to register with the namespace, then the command shall be aborted with status Reservation Conflict. A host may clear a reservation without regard to its current reservation key value by setting the Ignore Existing Key (IEKEY) bit to '1' in the command.

If the host is not a registrant, then the command shall be aborted with a status of Reservation Conflict.

Test Procedure:

1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable.
2. For each NVMe Controller in the NVM Subsystem:
   a. Configure the NVMe Host to issue a Set Features command with the Host Identifier feature to the NVMe Controller in order to set its Host Identifier for that controller.
   b. For each active namespace attached to the NVMe Controller:
      i. Configure the NVMe Host to issue a Reservation Release command, setting the Reservation Release Action (RRELA) field to 001b (i.e. Clear) and setting the Current Reservation Key (CRKEY) field to a random reservation key value to the NVMe Controller.
      ii. Configure the NVMe Host to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to the NVMe Controller for the namespace in order to make the host a registrant of that namespace.
      iii. Configure the NVMe Host to issue a Reservation Release command with the Clear action and supplying any reservation key other than the current reservation key associated with the host in the CRKEY field to the NVMe Controller.
      iv. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.
      v. Configure the NVMe Host to issue a Reservation Release command with the Clear action, supplying any reservation key other than the current reservation key associated with the host in the CRKEY field, and setting the IEKEY bit to '1' to the NVMe Controller in order to clear the reservation.
      vi. Configure the NVMe Host to issue a Reservation Report command to the NVMe Controller.

Observable Results:

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the completion queue entry for the first Reservation Release command with Clear action indicates status Reservation Conflict.
3. Verify that the completion queue entry for the second Reservation Release command with Clear action indicates status Reservation Conflict.
4. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the first Reservation Report command indicates that the host is still a registrant of the namespace.
5. Verify that the Reservation Status data structure returned by the NVMe Controller after completing the second Reservation Report command indicates that the host was successfully unregistered from the namespace.

Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 7.8 – Command Behavior with Different Reservation Types (M)

**Purpose:** To determine if an NVMe Controller exhibits proper command behavior in the presence of different reservation types.

**References:**
- NVMe Specification 8.8, 5.14.1.15

**Resource Requirements:**
- Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** April 1, 2016

**Discussion:** NVMe supports six types of reservations:
- Write Exclusive
- Exclusive Access
- Write Exclusive - Registrants Only
- Exclusive Access - Registrants Only
- Write Exclusive - All Registrants
- Exclusive Access - All Registrants

The differences between these reservation types are: the type of access that is excluded (i.e., writes or all accesses), whether registrants have the same access rights as the reservation holder, and whether registrants are also considered to be reservation holders.

For the purposes of reservation types, the following commands are considered to be in the NVM Read Command Group:
- Read
- Compare
- Security Receive

And the following commands are considered to be in the NVM Write Command Group:
- Write
- Write Uncorrectable
- Dataset Management
- Flush
- Format NVM
- Namespace Attachment
- Namespace Management
- Security Send

Additionally, certain reservation commands have specific behavior and all other commands shall be allowed regardless of reservation status or type. The behavior of vendor specific commands is vendor specific.

**Test Setup:** See Appendix A.

**Case 1: Write Exclusive (M) Dual Port Devices Only**
A Write Exclusive reservation disallows commands from the NVM Write Command Group by any host other than the registration holder. Any commands from the NVM Read Command Group are still allowed by any host.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

**Test Procedure:**
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to Write Exclusive to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation of type Write Exclusive.
6. Configure each host to issue each of the commands in the NVM Read Command Group above to their respective controllers.
7. Configure each host to issue each of the commands in the NVM Write Command Group above to their respective controllers.
8. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.
9. Configure NVMe Host 2 to issue each of the commands in the NVM Read Command Group above to NVMe Controller 2.
10. Configure NVMe Host 2 to issue each of the commands in the NVM Write Command Group above to NVMe Controller 2.

**Observable Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the completion queue entries for all commands sent by NVMe Host 1 indicate status Successful Completion.
3. Verify that the completion queue entries for all commands from the NVM Read Command Group sent by NVMe Host 2 indicate status Successful Completion.
4. Verify that the completion queue entries for all commands from the NVM Write Command Group sent by NVMe Host 2 indicate status Reservation Conflict.

**Case 2: Exclusive Access (M) Dual Port Devices Only**
An Exclusive Access reservation disallows commands from both the NVM Write Command Group and the NVM Read Command Group by any host other than the registration holder.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

**Test Procedure:**
1. Check the ONCS field to determine if the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.
2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.
3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.
4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.
5. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in
the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to Exclusive Access to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation of type Exclusive Access.

6. Configure each host to issue each of the commands in the NVM Read Command Group above to their respective controllers.

7. Configure each host to issue each of the commands in the NVM Write Command Group above to their respective controllers.

8. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.

9. Configure NVMe Host 2 to issue each of the commands in the NVM Read Command Group above to NVMe Controller 2.

10. Configure NVMe Host 2 to issue each of the commands in the NVM Write Command Group above to NVMe Controller 2.

Observable Results:

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.

2. Verify that the completion queue entries for all commands sent by NVMe Host 1 indicate status Successful Completion.

3. Verify that the completion queue entries for all commands sent by NVMe Host 2 indicate status Reservation Conflict.

Case 3: Write Exclusive - Registrants Only or Write Exclusive - All Registrants (M) Dual Port Devices Only

A Write Exclusive - Registrants Only or a Write Exclusive - All Registrants reservation disallows commands from the NVM Write Command Group by any non-registrant of the namespace. Any commands from the NVM Read Command Group are still allowed by any host and registrants of the namespace are still allowed to issue commands from the NVM Write Command Group.

The difference between the Write Exclusive - Registrants Only and Write Exclusive - All Registrants reservation types is that all registrants are also considered reservation holders with the Write Exclusive - All Registrants type.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

Test Procedure:

1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.

2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.

3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.

4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.

5. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to Write Exclusive - Registrants Only or Write Exclusive - All Registrants to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation of the specified type.

6. Configure each host to issue each of the commands in the NVM Read Command Group above to their respective controllers.

7. Configure each host to issue each of the commands in the NVM Write Command Group above to their respective controllers.
8. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.

9. Configure NVMe Host 2 to issue each of the commands in the NVM Read Command Group above to NVMe Controller 2.

10. Configure NVMe Host 2 to issue each of the commands in the NVM Write Command Group above to NVMe Controller 2.

**Observable Results:**

1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.

2. Verify that the completion queue entries for all commands sent by NVMe Host 1 indicate status Successful Completion.

3. Verify that the completion queue entries for all commands from the NVM Read Command Group sent by NVMe Host 2 indicate status Successful Completion.

4. Verify that the completion queue entries for all commands from the NVM Write Command Group sent by NVMe Host 2 while not a registrant of the namespace indicate status Reservation Conflict.

5. Verify that the completion queue entries for all commands from the NVM Read Command Group sent by NVMe Host 2 while a registrant of the namespace indicate status Successful Completion.

**Case 4: Exclusive Access - Registrants Only or Exclusive Access - All Registrants (M) Dual Port Devices Only**

An Exclusive Access - Registrants Only or an Exclusive Access - All Registrants reservation disallows commands from both the NVM Write Command Group and NVM Read Command Group by any non-registrant of the namespace. Registrants of the namespace are still allowed to issue commands from either command group.

The difference between the Exclusive Access - Registrants Only and Exclusive Access - All Registrants reservation types is that all registrants are also considered reservation holders with the Write Exclusive - All Registrants type.

This test requires there to be at least two controllers with a shared namespace in the NVM Subsystem.

**Test Procedure:**

1. Check the ONCS field to determine of the controller supports reservations. If the controller does not support reservations then this test is not applicable. If the DUT is a single port device then this test is not applicable.

2. Configure NVMe Host 1 to issue a Set Features command with the Host Identifier feature to NVMe Controller 1 in order to set its Host Identifier for that controller.

3. Configure NVMe Host 2 to issue a Set Features command with the Host Identifier feature to NVMe Controller 2 with a different Host Identifier than NVMe Host 1.

4. Configure NVMe Host 1 to issue a Reservation Register command with the Reservation Register Action (RREGA) field set to 000b (i.e. Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field to NVMe Controller 1 for the shared namespace in order to make the host a registrant of that namespace.

5. Configure NVMe Host 1 to issue a Reservation Acquire command, setting the Reservation Acquire Action (RACQA) field to 000b (Acquire), supplying the reservation key currently associated with NVMe Host 1 in the Current Reservation Key (CRKEY) field, and setting the Reservation Type (RTYPE) field to Exclusive Access - Registrants Only or Exclusive Access - All Registrants to NVMe Controller 1 in order for NVMe Host 1 to acquire a reservation of the specified type.

6. Configure each host to issue each of the commands in the NVM Read Command Group above to their respective controllers.

7. Configure each host to issue each of the commands in the NVM Write Command Group above to their respective controllers.

8. Configure NVMe Host 2 to issue a Reservation Register command with the Register Reservation Key action and supplying a reservation key in the NRKEY field to NVMe Controller 2 for the shared namespace in order to make the host a registrant of that namespace.

9. Configure NVMe Host 2 to issue each of the commands in the NVM Read Command Group above to NVMe Controller 2.
10. Configure NVMe Host 2 to issue each of the commands in the NVM Write Command Group above to NVMe Controller 2.

**Observables Results:**
1. Verify that after the completion of each command, the controller posts a completion queue entry to the associated Completion Queue indicating the status for the command.
2. Verify that the completion queue entries for all commands sent by NVMe Host 1 indicate status Successful Completion.
3. Verify that the completion queue entries for all commands sent by NVMe Host 2 while not a registrant of the namespace indicate status Reservation Conflict.
4. Verify that the completion queue entries for all commands sent by NVMe Host 2 while a registrant of the namespace indicate status Successful Completion.

**Possible Problems:** A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Group 8: Power State Transitions

Overview:

This section describes a method for performing conformance verification for NVMe products implementing NVMe Power State Transitions.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 8.1 – Autonomous Power State Transitions Enabled (M)

**Purpose:** To determine if an NVMe Controller properly supports Autonomous Power State Transitions.

**References:**
NVMe Specification 5.14.1.12, Fig 90, Fig 108, Fig 124

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** April 13, 2015

**Discussion:** An NVMe device may change power states autonomously without host intervention if Autonomous Power State Transitions are supported by the device and enabled by the Host. There are 32 allowable power states defined sequentially in the 256 byte data structure entry.

Each entry is 64 bits long and describes the Idle Time Prior to Transition (ITPTT) and Idle Transition Power State (ITPS). The Idle Transition Power State specifies the next power state the device will transition to after there is a continuous period of idle time in the current power state that exceeds the time specified in the Idle Time Prior to Transition field.

This test is not applicable to devices that do not claim to support Autonomous Power State Transitions.

**Test Setup:** See Appendix A.

**Test Procedure:**
1. Check that the DUT supports Autonomous Power State Transitions by setting Bit 0 of Byte 265 of the Identify Controller Data Structure, to 1. If this bit is set to 0, the test is not performed.
2. Using the Set Features Command, enable Feature Identifier 0Ch for Autonomous Power State Transition.
3. Perform the Get Feature Command to see that the Autonomous Power State Transitions feature was enabled (APSTE), and receive the Autonomous Power State Transition data structure.

**Observable Results:**
1. Verify that the controller returns a properly formatted Autonomous Power State Transition data structure.

**Possible Problems:** A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 8.2 – Return from Non–Operational State (FYI)

Purpose: To determine if an NVMe Controller properly supports Autonomous Power State Transitions.

References:
- NVMe Specification 8.4.1

Resource Requirements:
- Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: January 23, 2018

Discussion: When in a non-operational power state, regardless of whether autonomous power state transitions are enabled, the controller shall autonomously transition back to the last operational power state when an I/O Submission Queue Tail Doorbell is written.

When in a non-operational power state, regardless of whether autonomous power state transitions are enabled, the controller shall not transition back if an Admin Command has been sent.

Test Setup: See Appendix A.

Case 1: Basic Operation (FYI)

Test Procedure:
1. Check that the DUT supports Autonomous Power State Transitions by setting Bit 0 of Byte 265 of the Identify Controller Data Structure, to 1. If this bit is set to 0, the test is not performed.
2. Using the Set Features Command, enable Feature Identifier 0Ch for Autonomous Power State Transition.
3. Perform the Get Feature Command to see that the Autonomous Power State Transitions feature was enabled (APSTE), and receive the Autonomous Power State Transition data structure.
4. If the Autonomous Power State Transition Data Structure indicates that the device supports entering a non-operational state via APST, allow the DUT to remain idle for ITPT for each power state successively until the DUT enters a non-operational state.
5. Perform Identify Power State Descriptor Data Structure, check the NOPS field.
6. Perform an NVMe I/O Command, such as NVMe Write to the DUT.
7. Perform Identify Power State Descriptor Data Structure, check the NOPS field.

Observable Results:
1. Verify that the controller returns a properly formatted Autonomous Power State Transition data structure.
2. Verify that after the writing of the I/O Submission Queue Tail Doorbell, through the write command, the DUT returns to the last operational power state.

Case 2: Non-Operation State Admin Commands (FYI)

Test Procedure:
1. Check that the DUT supports Autonomous Power State Transitions by setting Bit 0 of Byte 265 of the Identify Controller Data Structure, to 1. If this bit is set to 0, the test is not performed.
2. Using the Set Features Command, enable Feature Identifier 0Ch for Autonomous Power State Transition.
3. Perform the Get Feature Command to see that the Autonomous Power State Transitions feature was enabled (APSTE), and receive the Autonomous Power State Transition data structure.
4. If the Autonomous Power State Transition Data Structure indicates that the device supports entering a non-operational state via APST, allow the DUT to remain idle for ITPT for each power state successively until the DUT enters a non-operational state.
5. For each supported Admin Command opcode, perform an Admin Command of that opcode, then perform Identify Power State Descriptor Data Structure, check the NOPS field.

**Observable Results:**
1. Verify that the controller returns a properly formatted Autonomous Power State Transition data structure.
2. Verify that after each Admin Command, the DUT stays in the Non-Operational Power State.

**Possible Problems:** None.
Test 8.3 – Autonomous Power State Transition (M)

Purpose: To verify that an NVMe system can properly handle autonomous power state transitions.

References:
- NVMe Specification 8.4.2, 5.14.1.12

Resource Requirements:
- Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: April 1, 2016

Discussion: The controller may support autonomous power state transitions, as indicated in the Identify Controller data structure at byte 265. Autonomous power state transitions provide a mechanism for the host to configure the controller to automatically transition between power states on certain conditions without software intervention.

The entry condition to transition to the Idle Transition Power State is that the controller has been idle for a continuous period of time exceeding the Idle Time Prior to Transition time specified. The controller is idle when there are no commands outstanding to any I/O Submission Queue. The power state to transition to shall be a non-operational power state (a non-operational power state may autonomously transition to another non-operational power state). If an operational power state is specified then the controller should abort the command with a status of Invalid Field in Command.

Test Setup: See Appendix A.

Test Procedure:

Case 1: Proper Structure
Each entry in the Autonomous Power State Transition data structure is defined in Figure 124 of the NVMe Specification. Each entry is 64 bits in size. There is an entry for each of the allowable 32 power states. For power states that are not supported, the unused Autonomous Power State Transition data structure entries shall be cleared to all zeroes. The entries begin with power state 0 and then increase sequentially (i.e., power state 0 is described in bytes 7:0, power state 1 is described in bytes 15:8, etc.). The data structure is 256 bytes in size and shall be physically contiguous.

Test Procedure:
1. Configure the NVMe Host to issue a Set Features command with an unsupported power state.
2. Configure the NVMe Host to issue a Get Features command with the feature ID set to Autonomous Power State Transition (0Ch) to the NVMe Controller.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that the Autonomous Power State Transition data structure and each of its entries are of proper size.
3. Verify that Autonomous Power State Transition data structure entries for power states not supported by the controller are cleared to all zeroes.

Case 2: Controller and Power State Basis
The Autonomous Power State Transition Feature uses Command Dword 11 and specifies the attribute information in the data structure indicated in Figure 123 and the Autonomous Power State Transition data structure consisting of 32 of the entries defined in Figure 124.
If a Get Features command is issued for this Feature, the attributes specified in Figure 123 are returned in Dword 0 of the completion queue entry and the Autonomous Power State Transition data structure, whose entry structure is defined in Figure 124 is returned in the data buffer for that command.

Test Procedure:
1. Configure the NVMe Host to issue a Set Features command for the Autonomous Power State Transition Feature with the Autonomous Power State Transition Enable (APSTE) bit cleared to ‘0’.
2. Configure the NVMe Host to issue a Get Features command for the Autonomous Power State Transition Feature to the NVMe Controller.
3. Configure the NVMe Host to issue a Set Features command for the Autonomous Power State Transition with the Autonomous Power State Transition Feature with APSTE bit set to ‘1’.
4. Configure the NVMe Host to issue a Get Features command for the Autonomous Power State Transition Feature to the NVMe Controller.
5. For each power state supported by the NVMe Controller:
   a. Configure the NVMe Host to issue a Set Features command for the Autonomous Power State Transition Feature with APSTE bit set to ‘1’ and, in the Autonomous Power State Transition data structure entry for that power state, specify a non-operational power state in the Idle Transition Power State (ITPS) field and a value of 100ms in the Idle Time Prior to Transition (ITPT) field.
   b. Ensure that the NVMe Controller is idle long enough for the controller to autonomously transition to the power state and then configure the NVMe Host to issue a Get Features command for the Power Management Feature to the NVMe Controller to get the current power state of the NVMe Controller.
   c. Configure the NVMe Host to issue a Set Features command for the Autonomous Power State Transition Feature with APSTE bit set to ‘1’ and, in the Autonomous Power State Transition data structure entry for that power state, specify a non-operational power state in the ITPS field and a value of 0ms in the ITPT field.
   d. After 10 seconds, configure the NVMe Host to issue a Get Features command for the Power Management Feature to the NVMe Controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. While Autonomous Power State Transition is disabled for a power state, verify that the controller does not autonomously transition from that power state.
3. While Autonomous Power State Transition is enabled for a power state, verify that the controller autonomously transitions to the configured power states after the configured idle time prior to transition period.

Case 3: Configurations

Test Procedure:
1. For each valid, non-operational power state, configure the NVMe Host to issue a Set Features command for the Autonomous Power State Transition Feature to the NVMe Controller specifying the non-operational power state in the Idle Transition Power State (ITPS) field for each entry in the Autonomous Power State Transition data structure and a value of 100ms in each Idle Time Prior to Transition (ITPT) field. Ensure that the Autonomous Power State Transition Enable (APSTE) field of the Set Features command is set to ‘1’.
2. Configure the NVMe Host to issue a Get Features command for the Autonomous Power State Transition Feature to the NVMe Controller specifying an operational power state to transition in the ITPS field.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.
2. Verify that the NVMe Controller successfully transitions to each non-operational power state.
3. Verify that the completion queue entry for the Set Features command with ITPS field set to an operational power state indicates status Invalid Field in Command.
Possible Problems: A reliable means of performing this test has not been determined. Therefore, this test should not be included in any industry approved determination of conformance.
Test 8.4 – Power State Entrance Latency (FYI)

Purpose: To verify that an NVMe system properly documents its entrance latency for each Power State.

Reference:
NVMe Specification 8.4

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: January 23, 2018

Discussion
The controller may support a Power States Entrance Latency field, as indicated in the Power State Descriptor table described in Figure 113 of the NVMe specification. This field indicates how long it should take, in microseconds, for a controller's power state to transition to another.

Test Setup: See Appendix A

Test Procedure:
1. For each Power State in the Power State Descriptor table with an ENLAT field that is not 0h:
2. Record the ENLAT field of the selected Power State and the EXLAT field of the current Power State
3. Have the NVMe host send a Set Feature Command with Feature Identifier 02h, Power Management, indicating a the new Power State
4. Wait the EXLAT of the previous Power State and the ENLAT of the power state being selected.
5. Send a Get Features command with Feature Identifier 02, Power Management.

Observable Results:
1. Verify that the Get Features command returns the Power State selected in the Set Features command.

Possible Problems: None.
Test 8.5 – Power State Exit Latency (FYI)

Purpose: To verify that an NVMe system properly documents its exit latency for each Power State.

Reference: NVMe Specification 8.4

Resource Requirements: Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: January 23, 2018

Discussion
The controller may support a Power States Exit Latency field, as indicated in the Power State Descriptor table described in Figure 113 of the NVMe specification. This field indicates how long it should take, in microseconds, for a controller’s power state to transition to another.

Test Setup: See Appendix A

Test Procedure:
1. For each Power State in the Power State Descriptor table with an EXLAT field that is not 0b:
2. Record the ENLAT field of the selected Power State and the EXLAT field of the current Power State
3. Have the NVMe host send a Set Feature Command with Feature Identifier 02h, Power Management, indicating a new Power State
4. Wait the EXLAT of the previous Power State and the ENLAT of the power state being selected.
5. Send a Get Features command with Feature Identifier 02, Power Management.

Observable Results:
1. Verify that the Get Features command returns the Power State selected in the Set Features command.

Possible Problems: None.
Test 8.6 – Relative Read Throughput (FYI)

**Purpose:** To determine if an NVMe Controller properly supports the Relative Read Throughput rates supported by different power states correctly.

**Reference:**
- NVMe Specification 8.4

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** January 23, 2018

**Discussion**
Different Power States have different Relative Read Throughput values that determine the speed at which they can read from the NVMe.

**Test Setup:** See Appendix A

**Test Procedure:**
1. Record the Relative Read Throughput for each supported power state.
2. For each power state, record the time it takes to do 100 read operations.

**Observable Results:**
1. Verify that the times for the 100 reads for a power state is lower than the time for any power state with a higher RRT.

**Possible Problems:** None.
Test 8.7 – Relative Write Throughput (FYI)

**Purpose:** To determine if an NVMe Controller properly supports the Relative Write Throughput rates supported by different power states correctly.

**Reference:**
NVMe Specification 8.4

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** January 23, 2018

**Discussion**
Different Power States have different Relative Write Throughput values that determine the speed at which they can write to the NVMe.

**Test Setup:** See Appendix A

**Test Procedure:**
1. Record the Relative Write Throughput for each supported power state.
2. For each power state, record the time it takes to do 100 writes.

**Observable Results:**
1. Verify that the times for the 100 writes for a power state is lower than the time for any power state with a higher RWT.

**Possible Problems:** None.
Test 8.8 – Host Controlled Thermal Management (FYI)

**Purpose:** To determine if an NVMe Controller properly supports the Host Controlled Thermal Management feature correctly.

**Reference:**
NVMe Specification 8.4

**Resource Requirements:**
Tools capable of monitoring and decoding traffic on the NVMe interface.

**Last Modification:** January 23, 2018

**Discussion**
The Host Controlled Thermal Management command can be set within certain boundaries specified by the Minimum Host Thermal Management Temperature field and the Maximum Host Thermal Management field in the Identify Controller Structure, this test ensures that the behavior of a Set Features command with an FID specifying Host Controlled Thermal Management reacts correctly to improper Thermal Management 1 & 2 values.

**Test Setup:** See Appendix A

**Case 1: Basic Operation (FYI)**

**Test Procedure:**
1. Record the current temperature of the DUT.
2. Set the drive to the highest active power state
3. If possible, send a Set Features with FID 10h (Host Controlled Thermal Management), with a Thermal Management Temperature 1 that is below the current device temperature, and a Thermal Management Temperature 2 that is above the current temperature.
4. Record the current power state.
5. Set the drive to the highest active power state
6. If possible, send a Set Features with FID 10h (Host Controlled Thermal Management), with a Thermal Management Temperature 1 that is below the current device temperature, and a Thermal Management Temperature 2 that is above the Thermal Management Temperature 1, but below the current temperature.
7. Record the current power state.

**Observable Results:**
1. Verify that after each Set Features command completes correctly.
2. For informational purposes display the Power State after each Set Features command.

**Case 2: Invalid Field (FYI)**

**Test Procedure:**
1. Record the current power state.
2. Perform a Set Features with FID 10h (Host Controlled Thermal Management), with a Thermal Management Temperature 1 that is 1 degree above the allowed , and a Thermal Management Temperature 2 that is 0xFFFF.
3. Record the current power state.
4. Perform a Set Features with FID 10h (Host Controlled Thermal Management), with a Thermal Management Temperature 1 that is 0xFFFF , and a Thermal Management Temperature 2 that is 1 degree above the Minimum Thermal Management Temperature.
5. Record the current power state.
6. Perform a Set Features with FID 10h (Host Controlled Thermal Management), with a Thermal Management Temperature 1 that is 1 degree above the allowed , and a Thermal Management Temperature 2 that is 0x1.
7. Record the current power state.
8. Perform a Set Features with FID 10h (Host Controlled Thermal Management), with a Thermal Management Temperature 1 that is 0x1, and a Thermal Management Temperature 2 that is 1 degree above the Minimum Thermal Management Temperature.
9. Record the current power state.

**Observable Results:**
1. Verify that after each Set Features command, an error code of Invalid Field is indicated and the power state has not changed.

**Possible Problems:** None.
Group 9: Namespace Management

Overview:

This section describes a method for performing conformance verification for NVMe products implementing NVMe Namespace Management features.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 9.1 – Namespace Management Identify Command (M, OF-FYI)

Purpose: To determine if an NVMe Controller properly implements the features of the Identify command relating to namespace management.

References:
- NVMe Specification 8.12

Resource Requirements:
- Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 2, 2016

Discussion: Additional CNS values were added to the Identify command relating to namespace management. Refer to Table 1.

Test Setup: See Appendix A.

Case 1: CNS 10h & 11h – Namespace Lists (M, OF-FYI)

Test Procedure:
1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue an Identify command specifying CNS value 10h and CDW1.NSID 00h to the NVMe Controller Under Test in order to receive back a Namespace List containing all allocated namespaces.
3. For each namespace returned in the Namespace List from the previous step, configure the NVMe Host to issue an Identify command specifying CNS value 11h and setting CDW1.NSID to the namespace identifier of the namespace to the NVMe Controller Under Test in order to receive back an Identify Namespace data structure for the specified namespace.

Observable Results:
1. Verify that the requested data structures are posted to the memory buffer indicated in PRP Entry 1, PRP Entry 2, and Command Dword 10, and that a command completion queue entry is posted to the Admin Completion Queue for each command issued to the NVMe Controller Under Test.
2. Verify that all Identify Namespace data structures returned by the controller are not zero filled.
3. Verify that unused entries in the Namespace List are zero filled.

Case 2: CNS 12h – Controller List – Controllers Attached to a Namespace (M)

Test Procedure:
1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue an Identify command specifying CNS value 02h and CDW1.NSID 00h to the NVMe Controller Under Test in order to receive back a Namespace List containing active namespaces.
3. For each namespace returned in the Namespace List from the previous step, configure the NVMe Host to issue an Identify command specifying CNS value 12h, CDW10.CNTID value 00h, and setting CDW1.NSID to the namespace identifier of the namespace to the NVMe Controller Under Test in order to receive back a Controller List containing the controller identifiers of all controllers attached to the namespace.

Observable Results:
1. Verify that the requested data structures are posted to the memory buffer indicated in PRP Entry 1, PRP Entry 2, and Command Dword 10, and that a command completion queue entry is posted to the Admin Completion Queue for each command issued to the NVMe Controller Under Test.
2. Verify that the controller identifier of the NVMe Controller Under Test is contained within each Controller List returned by the controller.
3. Verify that each Controller List contains valid values and that unused entries in the Controller List are zero filled.

Case 3: CNS 13h – Controller List – All Controllers (M)

Test Procedure:
1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue an Identify command specifying CNS value 13h and CDW10.CNTID value 00h to the controller in order to receive back a Controller List containing the controller identifiers of all controllers in the NVM subsystem. 0h is a valid controller identifier.

Observable Results:
1. Verify that the requested data structure is posted to the memory buffer indicated in PRP Entry 1, PRP Entry 2, and Command Dword 10, and that a command completion queue entry is posted to the Admin Completion Queue.
2. Verify that the controller identifier of the NVMe Controller Under Test is contained within the Controller List returned by the controller.
3. Verify that the Controller List contains valid values and that unused entries in the Controller List are zero filled.

Case 4: Common Namespace Data Structure (M, OF-FYI)

Test Procedure:
1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue an Identify command specifying CNS value 00h and CDW1.NSID value FFFFFFFFh to the controller in order to receive back an Identify Namespace data structure that specifies capabilities that are common across namespaces.

Observable Results:
1. Verify that the requested data structure is posted to the memory buffer indicated in PRP Entry 1, PRP Entry 2, and Command Dword 10, and that a command completion queue entry is posted to the Admin Completion Queue.

Possible Problems: None.
Test 9.2 – Namespace Management Command (M)

Purpose: To determine if an NVMe Controller properly implements the Namespace Management command.

References:
NVMe Specification 6.1, 8.12

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: July 20, 2016

Discussion: The Namespace Management command is used for managing namespaces. It can be used for creating and deleting namespaces. The Select (SEL) field of Command Dword 10 is used to specify the type of operation for the Namespace Management command.

The Namespace Management command uses the PRP Entry 1, PRP Entry 2, and Dword 10 fields. All other command specific fields are reserved.

Test Setup: See Appendix A.

Case 1: Namespace Creation – Exceed Number Supported (M)

The create operation creates a new namespace. The new namespace will not be attached to any controller. The Namespace Attachment command must be used to attach a new namespace to a controller if desired.

The data structure used for the created operation is defined in Figure 102 of the NVMe Specification and has the same format as the Identify Namespace data structure. However, the host is only allowed to set the following fields in the data structure:
- Namespace Size (NSZE)
- Namespace Capacity (NCAP)
- Formatted LBA Size (FLBAS)
- End-to-end Data Protection Type Settings (DPS)
- Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)

All other fields are reserved and shall be cleared to 0.

For the creation operation, the CDW1.NSID field is reserved and shall be cleared to 0. The controller selects the next available namespace identifier to use for the new namespace. The namespace identifier of the new namespace is returned in Dword 0 of the completion queue entry for the command.

If creation of a new namespace would cause the number of namespace to exceed the number of supported namespaces, then the controller shall return status Namespace Identifier Unavailable.

If the size of the new namespace exceeds the amount of available space on the device, then the controller shall return status Namespace Insufficient Capacity and the Command Specific Information field of the Error Information Log specifies the total amount of NVM capacity required to create the namespace in bytes.

Test Procedure:
1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue a Namespace Management command specifying Select field value 0h (Create) and valid values for the attached data structure to the NVMe Controller Under Test in order to create a new namespace.
3. Configure the NVMe Host to issue an Identify command specifying CNS field value 11h and CDW1.NSID value set to the namespace identifier of the newly created namespace to the NVMe Controller Under Test in order to receive back the Identify Namespace data structure for that namespace.

4. Configure the NVMe Host to issue Namespace Management commands specifying Select field value 0h (Create) and valid values for the attached data structure to the controller until the number of namespaces exceeds the number of namespaces supported by the NVM subsystem.

**Observable Results:**

1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.

2. Verify that a new inactive namespace is created and that the capabilities returned in the Identify Namespace data structure match the appropriate values set using the Namespace Management command.

3. Verify that the Namespace Identifier Unavailable status is returned when the number of namespaces exceeds the number of supported namespaces.

**Case 2: Namespace Deletion (M)**

The delete operation deletes an existing namespace. As a side effect of the delete operation, the namespace is detached from any controller as it is no longer present in the system. Namespaces detached due to a delete operation will become an inactive namespace.

There is no data structure transferred for the delete operation.

The CDW1.NSID field specifies the namespace to delete.

**Test Procedure:**

1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.

2. Configure the NVMe Host to issue a Namespace Management command specifying Select field value 1h (Delete) and CDW1.NSID field set to an active namespace in order to delete the specified namespace.

3. Configure the NVMe Host to issue an Identify command specifying CNS field value 02h and CDW1.NSID value 00h to the controller in order to receive back a Namespace List containing active namespace IDs attached to the controller.

**Observable Results:**

1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.

2. Verify that the deleted namespace is not contained within the Namespace List.

**Case 3: Namespace Creation – Insufficient Capacity (IP)**

The create operation creates a new namespace. The new namespace will not be attached to any controller. The Namespace Attachment command must be used to attach a new namespace to a controller if desired.

The data structure used for the create operation is defined in Figure 102 of the NVMe Specification and has the same format as the Identify Namespace data structure. However, the host is only allowed to set the following fields in the data structure:

- Namespace Size (NSZE)
- Namespace Capacity (NCAP)
- Formatted LBA Size (FLBAS)
- End-to-end Data Protection Type Settings (DPS)
- Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)

All other fields are reserved and shall be cleared to 0.
For the creation operation, the CDW1.NSID field is reserved and shall be cleared to 0. The controller selects the next available namespace identifier to use for the new namespace. The namespace identifier of the new namespace is returned in Dword 0 of the completion queue entry for the command.

If creation of a new namespace would cause the number of namespace to exceed the number of supported namespaces, then the controller shall return status Namespace Identifier Unavailable.

If the size of the new namespace exceeds the amount of available space on the device, then the controller shall return status Namespace Insufficient Capacity and the Command Specific Information field of the Error Information Log specifies the total amount of NVM capacity required to create the namespace in bytes.

**Test Procedure:**

1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue a Namespace Management command specifying Select field value 0h (Create) and valid values for the attached data structure to the NVMe Controller Under Test in order to create a new namespace.
3. Configure the NVMe Host to issue an Identify command specifying CNS field value 11h and CDW1.NSID value set to the namespace identifier of the newly created namespace to the NVMe Controller Under Test in order to receive back the Identify Namespace data structure for that namespace.
4. Configure the NVMe Host to issue Namespace Management commands specifying Select field value 0h (Create) and valid values for the attached data structure to the controller until the amount of available space on the device is exceeded.

**Observable Results:**

1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that a new inactive namespace is created and that the capabilities returned in the Identify Namespace data structure match the appropriate values set using the Namespace Management command.
3. Verify that the Namespace Insufficient Capacity status is returned if the size of a new namespace would exceed the available space on the device.

**Possible Problems:**

For Case 1, there may not be enough capacity remaining in the NVM subsystem or the number of namespace limit may already be reached which would prevent creation of a new namespace. In this case, the NVMe Host may delete an existing namespace to allow for creation of a new namespace.

For Case 2, there may be no active namespaces available for deletion. In this case, the NVMe Host may create and set up an active namespace in order to perform procedure steps which require such a namespace.

The NVMe Host should return the state of the device to its state from prior to running these test cases in order to prevent issues with other tests.
Test 9.3 – Namespace Attachment Command (M)

Purpose: To determine if an NVMe Controller properly implements the Namespace Attachment command.

References:
NVMe Specification 6.1, 8.12

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: March 2, 2016

Discussion: The Namespace Attachment command is used to attach and detach controllers from a namespace.

The Select field of command Dword 10 of the Namespace Attachment command is used to specify the operation of the command (attach or detach). The data structure used in the command is a 4096 byte Controller List which specifies the controllers that are to be attached or detached as part of the command. If the Controller List data structure transferred with the Namespace Attachment command is not properly formatted or is otherwise invalid then the command shall return status Controller List Invalid.

The Namespace Attachment command uses the Command Dword 10 field. All other command specific fields are reserved.

Test Setup: See Appendix A.

Case 1: Namespace Attachment (M)

If a Namespace Attachment command is issued with the Controller Attach action selected and the namespace is already attached to a controller specified in the Controller List data structure transferred with the command, then the command shall return status Namespace Already Attached.

If a Namespace Attachment command is issued with the Controller Attach action selected and the namespace is private and already attached to another controller, then the namespace shall not be attached to any of the controllers specified in the Controller List data structure transferred with the command and the command shall return status Namespace Is Private.

Test Procedure:
1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue a Namespace Attachment command, specifying Select field value 0 (Attach), CDW0.NSID field value of an inactive namespace, and the controller identifier of the NVMe Controller Under Test in the attached data structure, to the controller in order to attach the specified namespace to the controller.
3. Configure the NVMe Host to issue an Identify command specifying CNS field value 02h and CDW1.NSID value 00h to the NVMe Controller Under Test in order to receive back a Namespace List containing active namespace IDs attached to the controller.
4. Configure the NVMe Host to issue a Namespace Attachment command, specifying Select field value 0 (Attach), CDW0.NSID field value of the same namespace used in the previous step, and the controller identifier of the NVMe Controller in the attached data structure, to the controller.

Observable Results:
1. Verify that after the completion of the command, the controller posts a completion queue entry to the appropriate Completion Queue indicating the status for the command.
2. Verify that the namespace attached to the controller via the Namespace Attachment command is contained within the returned Namespace List to signify that the namespace was successfully attached.
3. Verify that the status of the second Namespace Attachment command is Namespace Already Attached.

Case 2: Namespace Detachment (M)

When a namespace is detached from a controller it becomes an inactive namespace on that controller. Previously submitted but uncompleted or subsequently submitted commands to the affected namespace are handled by the controller as if they were issued to an inactive namespace.

If a Namespace Attachment command is issued with the Controller Detach action selected and the namespace is not attached to a controller specified in the Controller List data structure transferred with the command, then the command shall return status Namespace Not Attached.

Test Procedure:
1. Check the OACS field to determine if the DUT supports Namespace Management. If the DUT does not support Namespace Management then this test is not applicable.
2. Configure the NVMe Host to issue a Namespace Attachment command, specifying Select field value 1h (Detach), CDW0.NSID field value of an inactive namespace, and the controller identifier the NVMe Controller Under Test in the attached data structure, to the controller in order to attempt to detach the specified namespace from the controller.
3. Configure the NVMe Host to issue a Namespace Attachment command, specifying Select field value 1h (Detach), CDW0.NSID field value of a namespace attached to the controller, and the controller identifier of the NVMe Controller Under Test in the attached data structure, to the controller in order to detach the specified namespace from the controller.
4. Configure the NVMe Host to issue an Identify command specifying CNS field value 02h and CDW1.NSID value 00h to the NVMe Controller Under Test in order to receive back a Namespace List containing active namespace IDs attached to the controller.

Observable Results:
1. Verify that after the completion of each command, the controller posts a completion queue entry indicating the status for the command.
2. Verify that the status of the first Namespace Attachment command isNamespace Not Attached.
3. Verify that the namespace identifier of the namespace which was detached from the controller via the Namespace Attachment command is not contained within the returned Namespace List to signify that the namespace was successfully detached from the NVMe Controller Under Test.

Possible Problems:

There may not be an inactive namespace in the NVM subsystem. In this case, the NVMe Host may create an inactive namespace in order to perform procedure steps which require such a namespace.
Group 10: System Bus Registers

Overview:

This section describes a method for performing conformance verification for NVMe products implementing the System Bus Register.

Notes:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).
Test 10.1 – PCI Express Capability Registers (M)

Purpose: To determine if an NVMe Controller properly implements the PCI Express Capability Registers.

References:
NVMe Specification 2.5

Resource Requirements:
Tools capable of monitoring and decoding traffic on the NVMe interface.

Last Modification: June 13, 2016

Discussion: NVMe controller using the PCI Express system bus must report their PCI Express capabilities via the PCI Express Capability Registers.

Test Setup: See Appendix A.

Test Procedure:
1. Configure the Host and Controller to bring up the PCIe link, and bring the NVMe Controller to the enabled state.
2. Examine the PCIe bringup sequence for the PXCAP register contents, and record. The PCIe capability structure ID is 0x10.

Observable Results:
1. Verify that the PCIe Capabilities register (PXCAP) follows the format defined in section 2.5 of the NVMe Specification.
2. Verify that all reserved bits are set to 0.

Possible Problems: None.
Appendix A: DEFAULT TEST SETUP

Except where otherwise specified, all tests will require the DUT to have one of the following default physical configuration at the beginning of each test case:

Test Setup for NVMe Device:
Appendix B: NOTES ON TEST PROCEDURES

There are scenarios where in test procedures it is desirable to leave certain aspects of the testing procedure as general as possible. In these cases, the steps in the described test procedure may use placeholder values, or may intentionally use non-specific terminology, and the final determination of interpretation or choice of values is left to the discretion of the test technician. The following is an attempt to capture and describe all such instances used throughout the procedures.

Ports on Testing Station and Device Under Test

In general, any PCIe Port on the Testing Station or Device Under Test may be used as an interface with a test station or interoperability partner. There is assumed to be no difference in behavior, with respect to the protocols involved in this test suite, between any two PCIe ports on the Testing Station or Device Under Test. Hence, actual ports used may be chosen for convenience. However, it is recommended that the PCIe port used in the test configuration is recorded by the test technician.

Use of “various”

To maintain generality, some steps will specify that “various other values” (or the like) should be used in place of a given parameter. Ideally, all possible values would be tested in this case. However, limits on available time may constrain the ability of the test technician to attempt this. Given this, a subset of the set of applicable values must generally be used.

When deciding how many values should be used, it should be noted that the more values that are tested, the greater the confidence of the results obtained (although there is a diminishing return on this).

When deciding which specific values to use, it is generally recommended to choose them at pseudo-randomly yet deterministically. However, if there exist subsets of the applicable values with special significance, values from each subset should be attempted.
Appendix C: TEST TOOLS

The Tests described in this document can be performed using available IOL INTERACT NVMe Test Software available from UNH–IOL.

If using the PC Edition of the IOL INTERACT NVMe Test Software, UNH-IOL recommends using v9 or higher of the IOL INTERACT NVMe Test Software. This software is available via https://www.iol.unh.edu/solutions/test-tools/interact.

If using the Teledyne-LeCroy edition of the IOL INTERACT NVMe Test Software, UNH-IOL recommends using v9 or higher of the IOL INTERACT NVMe Test Software. This software is available at https://www.iol.unh.edu/solutions/test-tools/interact. This should be used in conjunction with v8.7 or higher of the Teledyne-LeCroy PC Edition software available at: http://teledynelecroy.com/support/softwaredownload/documents.aspx?standardid=18
Appendix D: NVMe INTEGRATORS LIST REQUIREMENTS

Purpose: To provide guidance on what tests are required for NVMe Integrators List Qualification

References:
[1] NVMe Integrators List Policy Document

Resource Requirements:
NVMe Host Platform and Device.

Last Modification: November 28, 2017

Discussion: Each Test defined in this document is defined as being Mandatory (M), FYI, or In Progress (IP). This primary designation is shown in the title of the test case and is understood to apply to PCIe based products. An additional designation is provided if a test is applicable to NVMeoF products (OF). Tests that are designated as being applicable to NVMeoF Products are understood to inherit the primary designation of the test (i.e. M, FYI, IP), unless an additional designation is specified. The following examples are provided:

Test 1.1 Example Name (M)– Test is mandatory for all PCIe based products, and does not apply to NVMeoF products.
Test 2.1 Example Name (M, OF)– Test is mandatory for all products, including NVMeoF products.
Test 3.1 Example Name (M, OF-IP)– Test is mandatory for all PCIe based products, and test is currently On Progress for NVMeoF products.

If a Test is designated as Mandatory, a product must pass this test in order to qualify for the NVMe Integrators List. For tests that deal with features defined as optional in the NVMe specification, a check is performed at the beginning of the test to determine if the optional feature is supported or not. If the optional feature is not supported the test is marked as ‘Not Applicable’ and does not impact qualification for the Integrators List.

If a Test is designated as FYI, a device does not need to pass this test in order to qualify for the NVMe Integrators List. Tests designated as FYI may become Mandatory tests in the future.

If a Test is designated as In Progress, a device does not need to pass this test in order to qualify for the NVMe Integrators List. These test cases are still under development. Tests designated as In Progress may become Mandatory tests in the future.

Any Test may have a Case within it with a different designation as the Test itself (i.e. a Mandatory test may include FYI cases). In this case, only the Mandatory Cases are required for NVMe Integrators List qualification.