University of New Hampshire InterOperability Laboratory Ethernet Consortium



As of November 4th, 1999 the Ethernet Consortium Clause # 28 Auto Negotiation State Machine Base Page Exchange Conformance Test Suite version 3.10 has been superseded by the release of the Auto Negotiation State Machine Base Page Exchange Conformance Test Suite version 4.0.2. This document along with earlier versions, are available on the Ethernet Consortium test suite archive page.

Please refer to the following site for both current and superseded test suites:

http://www.iol.unh.edu/testsuites/ethernet/archive.html

Test Group 1: FLP Burst Transmission

Test #28.1.1: Separation of FLP Bursts

Purpose: To verify proper separation of consecutive FLP bursts.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.1.4.1, 28.2.1.1, 28.2.1.1.2

Resource Requirements:

• Line Monitor

Last Modification: May 5, 1999

Discussion: A station capable of auto-negotiation must transmit fast link pulse (FLP) bursts. Not only is the content and composition of these bursts important, but also the timing of the bursts. This test is designed to verify that the timing of the device under test's consecutive FLP bursts fall within the specified range.

Test Setup: Set up the devices as shown. Using Category 5 UTP cable, connect the DUT to a 100 Ω line termination. Connect the Line Monitor's first channel to the DUT's receive pair and second channel to the DUT's transmit pair with differential high impedance taps.

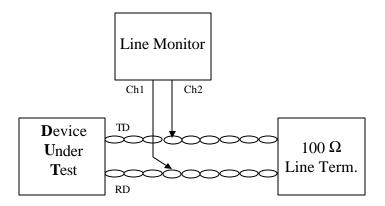


Figure 28.1.1-1: Test Configuration

Procedure:

- 1. The DUT is configured to send FLP bursts
- 2. Monitor the transmitted bursts
- 3. The separation of each burst is measured

Observable Results:

• The separation of FLP bursts should be 14 ± 8.3 ms

Test #28.1.2: Internal Separation of FLP Bursts

Purpose: To verify that the device under test transmits FLPs with valid pulse separation.

References:

• ANSI/IEEE Std 802.1998 Edition: Sections 28.1.4.1, 28.2.1.1, 28.2.1.1.2

Resource Requirements:

• Line Monitor

Last Modification: May 5, 1999

Discussion: To ensure that the content of an FLP burst is interpreted accurately, the individual pulses that make up the burst must be analyzed. This test is designed to verify that the device under test sends FLP bursts whose clock and data pulses are spaced properly.

Test Setup: See Figure 28.1.1-1

Procedure:

- 1. The DUT is configured to send FLP bursts
- 2. Monitor the transmitted bursts
- 3. The spacing between clock pulses (starting with the first pulse and then every odd pulse after that) is measured
- 4. The spacing between clock and data pulses is measured

- The spacing between clock pulses should be 125±14 μs
- The spacing between clock and data pulses should be $62.5\pm7 \mu s$

Test #28.1.3: Transmitted Link Code Word (Base Page) Encoding

Purpose: To verify that the device under test transmits valid FLP data. This includes an acceptable selector field combination, advertises the correct abilities in the technology ability field, and transmits proper initial values for the remote fault, acknowledge, and next page bits.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.1.1, 28.2.1.2, 28.2.1.2.1, 28.2.1.2.2, 28.2.1.2.3, 28.2.1.2.4, 28.2.1.2.5, Annex 28A, 28B, 28B.1, 28B.2

Resource Requirements:

• Line Monitor

Last Modification: May 5, 1999

Discussion: This test is designed to verify that the device under test transmits Link Code words with acceptable content. There are defined selector field combinations that a station is permitted to transmit in its link code word. The technology ability field of the link code word advertises a station's abilities. The final three bits in the link code word (Remote Fault bit, Acknowledge bit, Next Page bit) should all have a proper initial setting. The default value for the RF bit on a non-faulting link is zero. The Ack bit should be initially zero. The NP bit should be one if it supports Next Page exchange and zero if it doesn't or does not wish to implement a NP exchange. In this test, it is confirmed that the device under test transmits a link code word with the selector field combination corresponding to IEEE 802.3, advertises the data service abilities that it supports in its technology ability field, and has the RF, Ack, and NP bits set correctly.

Test Setup: See Figure 28.1.1-1

Procedure:

- 1. The DUT is configured to send FLP bursts
- 2. Monitor the transmitted bursts
- 3. The number of pulses and data present in the several burst is observed
- 4. The contents of the selector field (first five data bits), technology ability field (D[5:12]), and of the Remote Fault bit, Acknowledge bit, and Next Page bit are acquired

- The number of pulses in a burst should be 17-33 (inclusive)
- The data in the default base code word should not change
- The selector field combination should correspond to S[4:0]=00001 as defined in table 28-9
- The technology ability field should advertise the proper abilities as indicated in table 28-10
- The DUT should not advertise any abilities that it does not possess
- The value of the Remote Fault bit should be zero
- The value of the Acknowledge bit should be zero
- The value of the Next Page bit should be one if it supports Next Page exchange and zero if it doesn't or does not wish to implement a NP exchange

Test #28.1.4: NLP Compliance

Purpose: To verify the device under test's link pulse waveforms meet specification.

References:

ANSI/IEEE Std 802.3 1998 Edition: Sections 28.1.4.1, 28.2.1.1, 28.4

• ANSI/IEEE Std 802.3, 1993 Edition: Section 14.3.1.2.1, Figure 14-12

Resource Requirements:

- Oscilloscope
- Differential Voltage Probes
- TP Test Card

Last Modification: May 5, 1999

Discussion: All link pulses need to conform to the transmitter waveform specifications for Link Test Pulses defined in IEEE 802.3 Figure 14-12, including those contained in an FLP burst. This test is designed to verify that the device under test produces link pulses within specification.

Test Setup: Set up the devices as shown. Using Category 5 UTP cable, connect the DUT to the TP Test Card. Connect the Oscilloscope to the TP Test Card using Differential Voltage Probes.

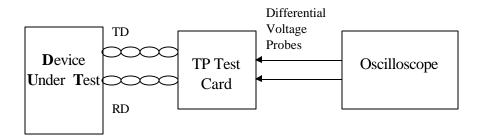


Figure 28.1.4-1: Test Configuration

Procedure:

- 1. The DUT is configured to send FLP bursts
- 2. Monitor the transmitted bursts
- 3. Observe the link pulse waveforms across each test load defined in fig. 14-11
- 4. Repeat procedure with loads connected through the TPM

- Under each test setup, the FLP's link pulses should fit within the NLP template defined in Figure 14-12.
- After the differential output voltage drops below -50 mV, it shall remain below +50 mV.

Test Group 2: FLP Burst Reception

Test #28.2.1: Acknowledge Bit

Purpose: To verify that the device under test enters the Acknowledge Detect state upon reception of complete, consecutive and consistent FLP bursts, ignoring the value of the Acknowledge bit.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.1.4.2, 28.2.1.2.4

Resource Requirements:

• Line Monitor

• Traffic Generator

Last Modification: May 5, 1999

Discussion: Once an auto-negotiating device identifies its link partner as auto-negotiation able, it will enter the Acknowledge Detect state only after it receives at least 3 complete, consecutive and consistent link code words from its link partner, ignoring the Acknowledge bit. Once the Acknowledge Detect state is entered, the station should send out FLP bursts containing its link code word with the Acknowledge bit (the fifteenth data pulse) set to logic one. This test is designed to verify that the device under test will set the Acknowledge bit after the reception of 3 or more complete, consecutive and consistent link code words.

Test Setup: Set up the devices as shown. Using Category 5 UTP cable, connect the DUT's transmit pair to a 100Ω line termination, and the receive pair to a traffic generator. Connect the Line Monitor's first channel to the DUT's receive pair and second channel to the DUT's transmit pair with differential high impedance taps.

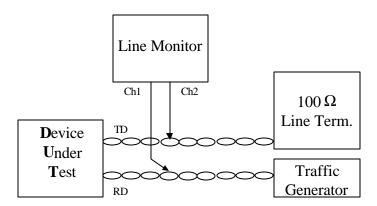


Figure 28.2.1-1: Test Configuration

Procedure:

Part A:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send a series of 3 FLPs
- 3. Monitor the FLPs sent back by the DUT and determine whether the Acknowledge bit is set
- 4. If it was not set, repeat the procedure with an increasing number of FLPs until the bit is set
- 5. Repeat steps 1-3 sending the number of FLPs that was determined to put the DUT into the Acknowledge Detect state, all with the Acknowledge bit set to a logic one
- 6. Repeat using FLPs that have Acknowledge bits that alternate between 1 and 0 *Part B:*

7. Establish a connection (not a link) to the DUT

- 8. Use the Traffic Generator to send enough FLPs, alternating between valid FLPs containing different advertised abilities, such that the number of FLPs would be enough to put the station into the Acknowledge Detect state
- 9. Monitor the FLPs sent back by the DUT and determine whether the Acknowledge bit is set *Part C*:
- 10. Establish a connection (not a link) to the DUT
- 11. Send a series of FLPs designed to put the DUT in Acknowledge State
- 12. Monitor the FLPs sent from the DUT after returning to the Ability Detect State and determine whether the Acknowledge bit is set

Observable Results:

Part A:

- The Acknowledge bit should be set after the reception of at least 4 complete and matching FLPs, regardless of the value of the Acknowledge bit
- Record the number of FLPs required to put the DUT into the Acknowledge Detect state for use in later tests

Part B:

• The DUT should not enter the Acknowledge Detect state

Part C:

• The DUT should reset to its default base page and not be sending FLPs with the Acknowledge Bit set

Test #28.2.2: Transmit Disable State

Purpose: To verify that the device under test enters the Ability Detect state upon completion of break_link_timer from the Transmit Disable State

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.1.4.2, 28.2.1.2.4

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once an auto-negotiating device enters the Transmit Disable State, it should stop transmission for break_link_timer before it re-enters the Ability Detect State. However, there is no specification as to whether the DUT's receiver has to be turned off in the Transmit Disable State. If a sequence of FLPs designed to cause an auto-negotiating station to enter the Acknowledge Detect State is sent to the DUT during Transmit Disable, acknowledge detect can be set to true. However, once break_link_timer is finished, the DUT will enter the Ability Detect State where acknowledge detect is reset to false.

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send a series of 4 FLPs designed to cause the DUT to enter the Acknowledge Detect State (determined in test #28.2.1)
- 3. Once the DUT halts its FLP transmission, send the same sequence of FLPs at periodic intervals less than break link timer
- 4. Monitor the DUTs FLP transmission during this process

Observable Results:

• The DUT should resume FLP transmission after break_link_timer is finished, regardless of the received FLPs during the time where the DUT was in the Transmit Disable State

Test #28.2.3: Behavior with Incomplete FLPs

Purpose: To observe the device under test's behavior upon receipt of incomplete FLP bursts.

References:

 ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.3.1 & Figures 28-7, 28-15 Receive State Diagram

Resource Requirements:

- Traffic Generator
- Line Monitor

Last Modification: May 5, 1999

Discussion: This test identifies how a given implementation chooses to handle FLPs with less than 16 data positions. While Figure 28-15 'Receive State Diagram', will accept incomplete FLPs without error, a difficulty in interpretation lies with the definition of 'ability_match' in 28.3.1. Here it is stated that the Acknowledge bit will be set upon reception of three matching consecutive Link Code Words. While section 28.2.1.2 and Figure 28-7 'Base page encoding' suggest a Link Code Word is 16 bits, this is not stated explicitly. Thus, if one interprets a Link Code Word to be 16 bits (or greater, refer to #28.2.4, then any FLP containing less than 16 data positions would be ignored as such a short FLP would not be used in the ability_match function. Alternatively, if a Link Code Word is interpreted to mean any length bit-vector, then any short/incomplete FLP must be used in an ability_match. This would allow for the possibility of ability_match being set to true upon receipt of three matching consecutive, but short, FLPs. While such a scenario would undoubtedly present problems, the likelihood seems small. A benefit gained through such an approach may be increased robustness as incomplete FLPs resulting from error conditions and/or line noise will not be ignored by the auto-negotiating device, as is the case in the first case.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A: (informative)

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT enough incomplete FLPs consisting of only 15 pulses to put the DUT into the Acknowledge Detect state (see test #28.2.1)
- 3. Observe whether the DUT entered the Acknowledge Detect state

Part B:

- 4. Establish a connection (not a link) to the DUT
- 5. Use a Traffic Generator to send the DUT enough incomplete FLPs, consisting of only 9 clock pulses and spaced so that the time to send all four FLPs is larger than nlp_test_max_timer, to put the DUT into the Acknowledge Detect state (see test #28.2.1)
- 6. Observe whether the DUT entered the Acknowledge Detect state

Part C:

- 7. Establish a connection (not a link) to the DUT
- 8. Use a Traffic Generator to send the DUT a series of the following 2 FLPs alternating at 16 ms apart:
- 9. a 17 pulse FLP containing the following data: 1 1 0 0 0 1 1 1 1 1 with no clock pulse after the final 1
- 10. an 8 pulse FLP containing the following data: 0 0 0 0 1 0 with a final clock pulse
- 11. Observe whether the DUT entered the Acknowledge Detect state

Observable Results:

Part A:

• As mentioned in the discussion above, a DUT may or may not enter the Acknowledge detect state

Part B:

• The DUT should not enter the Acknowledge Detect state

Part C:

• The DUT should not enter the Acknowledge Detect state

Test #28.2.4: Acceptance of Long FLPs

Purpose: To verify that the device under test properly accepts FLPs that have more than 16 data positions by ignoring all but the first 16 data bits.

References:

ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.2, 28.2.2.1, 28.3.3 (Rx_bit_cnt), Figure 28-15 Receive State Diagram

Resource Requirements:

- Traffic Generator
- Line Monitor

Last Modification: May 5, 1999

Discussion: An FLP burst normally consists of 17 to 33 pulses, with normally 16 data bits. However, if a device receives an FLP with more than 16 data positions, it should still accept the burst. The first 16 data bits should be kept and any additional should be ignored. This test is designed to determine whether the Device Under Test properly accepts FLPs with more than 16 data bits.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A:

- 1. Establish a connection (not a link) to the DUT.
- 2. Use a Traffic Generator to send enough valid FLPs with 1 extra data position corresponding to a '1' (1 extra clock pulse and 1 data pulses) attached to the end to put the DUT into the Acknowledge Detect state (see #28.2.1).
- 3. Observe whether the DUT enters the Acknowledge Detect state.
- 4 Part R
- 5. Repeat steps 1 through 3 above, sending 5 additional data bits corresponding to 10001.

Observable Results:

• The DUT should enter the Acknowledge Detect state in both cases

Test #28.2.5: Next Page and Remote Fault Bits

Purpose: To verify that the device under test can handle the reception of an FLP from a next page capable device as well as the reception of a flagged remote fault bit.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.2.1.2.3, 28.2.1.2.5, 28.2.3.4, 28.2.3.5

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: When a station is connected to a next page able device, it will receive FLP bursts with set next page bits (the final bit of the link code words set to logic one). Regardless of whether the receiving station is next page able or not, it should still accept the link code word as valid. When connected to any station, it is possible for a device to receive a logic one in the Remote Fault (RF) bit position (bit D13) of the link code word. The only defined behavior for a device to take in this event is that it should set the remote fault bit in the MII status register. Other than that, there is no specification as to what action a device should take upon reception of a remote fault. This test is designed to verify that the device under test is capable of receiving a flagged next page and/or remote fault bit.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send enough FLPs with the next page bit set to a logic one to put it into the Acknowledge Detect state (see test #28.2.1)
- 3. Verify that the DUT enters the Acknowledge Detect state

Part B:

4. Repeat with FLPs with the remote fault bit set to a logic one

Observable Results:

Part A:

• The DUT should enter the Acknowledge Detect state

Part B:

• The DUT should set the remote fault bit in its MII status register, and any other behavior is unpredictable

Test #28.2.6: Selector Field Reserved Combinations

Purpose: To verify that the device under test accepts FLPs with the selector field set to a reserved combination or to the defined Isochronous Ethernet combination.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.2.1.2.1, Annex 28A, 28B, 28B.1

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: There are combinations for the selector field that are reserved by the IEEE. A station is never supposed to transmit these combinations, but there are no specifications as to the combinations that can be received. Therefore, as long as complete and consistent link code words are received, a station should accept them as valid regardless of the selector field combination. This test is designed to verify that the device under test will accept a link code word with the selector field set to a reserved combination. A second Selector Field combination has been defined as Isochronous Ethernet (0,1,0,0,0).

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send enough FLPs with the selector field combination of 0,0,1,1,1 (ordered bit S0 to S4) to put it into the Acknowledge Detect state (see test #28.2.1)
- 3. Verify that the DUT enters the Acknowledge Detect state
- 4. Repeat steps 2 and 3 changing the selector field combination to 0,1,0,0,0

Observable Results:

• In both cases, the DUT should enter the Acknowledge Detect state

Test #28.2.7: Technology Ability Field Reserved Bits

Purpose: To verify that the device under test accepts FLPs with the reserved bits of the technology ability field set to logic one.

References:

ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.2.1.2.2, 28.2.3.3, Annex 28B.2

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: The last three bits of the technology ability field of a link code word are reserved by the IEEE. A station is supposed to transmit these bits as logic zero, but is supposed to be able to receive these bits set to a one without a problem. This test is designed to verify that the device under test will accept a link code word with the last three bits (the reserved bits) of the technology ability field set to logic one.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send enough FLPs with the fifth, sixth, and seventh bits of the technology ability field set to logic one to put it into the Acknowledge Detect state (see test #28.2.1)
- 3. Verify that the DUT enters the Acknowledge Detect state

Observable Results:

• The DUT should enter the Acknowledge Detect state

Test #28.2.8: Range of NLP Timer

Purpose: To verify that the device under test accepts FLP bursts with proper spacing, and refuses those with spacing outside of the acceptable range.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.2.1, 28.3.2

Resource Requirements

- Traffic Generator
- Line Monitor

Last Modification: May 5, 1999

Discussion: As well as characteristic requirements, FLP bursts have requirements for the delay between consecutive bursts. In order to be accepted as valid, received FLP bursts must have a delay between them between "nlp_test_min_timer" and "nlp_test_max_timer." The value for "nlp_test_min_timer" must be between 5 and 7ms. The value for "nlp_test_max_timer" must be between 50 and 150ms. This test is to verify that the device under test accepts FLP bursts with spacing within these ranges, and refuses FLP bursts with spacing outside of these ranges. Note, "nlp_test_min_timer" is measured from the beginning of an FLP to the beginning of the next FLP, whereas "nlp_test_max_timer" is measured from the end of an FLP to the beginning of the next FLP.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A: nlp_test_min_timer

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT enough FLP bursts spaced at 5 ms apart to put it into the Acknowledge Detect state (see test #28.2.1)
- 3. Observe whether the DUT entered the Acknowledge Detect state
- 4. Repeat steps 1 through 3 varying the spacing of the FLPs until the DUT enters the Acknowledge Detect state

Part B: nlp_test_max_timer

5. Repeat steps 1 through 3 varying the spacing of the FLPs starting at 150ms, until the DUT enters the Acknowledge Detect state

- In Part A, the nlp_test_min_timer should lay between 5ms and 7ms
- In Part B, the nlp_test_max_timer should lay between 50ms and 150ms

Test #28.2.9: Identification of Link Partner as Auto-Negotiation Able

Purpose: To verify that the device under test is able to recognize its link partner as capable of autonegotiation within specification.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.2.2.1

Resource Requirements:

• Traffic Generator

Last Modification: May 5, 1999

Discussion: When establishing a link, a station is required to recognize its link partner as autonegotiation able within a certain range of pulses in an FLP burst. This test is designed to verify that the device under test adheres to this range. As determined from State Diagram 28-15, flp_cnt is determined to be 1 less than the number of pulses required to recognize its link partner as auto-negotiation able.

Test Setup: See Figure 28.2.1-1.

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT 6 pulses spaced at 50µs, wait 16ms, then send enough valid FLP bursts to put the DUT into the Acknowledge Detect state. The proper number of FLP bursts should be one less than the value determined in #28.1.3 as that value includes the FLP required to identify a device as auto-negotiation able.
- 3. Determine whether the DUT has entered the Acknowledge Detect state
- 4. If the DUT did not enter the Acknowledge Detect state, repeat steps 1 through 3 increasing the number of initial pulses until the DUT enters the Acknowledge Detect state

Observable Results:

• The DUT should recognize the Link Partner as auto-negotiation able within 7 to 18 (inclusive) pulses. Flp_cnt is one less than this determined number

Test #28.2.10: Range of FLP Pulse Timer

Purpose: To verify that the device under test determines that its link partner is auto-negotiation able upon receiving pulses spaced within flp_test_min_timer and flp_test_max_timer, and does not recognize a device as auto-negotiation able upon receiving pulses spaced outside the acceptable range.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.2.1, 28.3.2, Figure 28-15 Receive State Diagram

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: As well as characteristic requirements, FLP bursts have requirements for the delay between consecutive pulses within the burst. In order to be accepted as valid, received pulses must have a delay between them between "flp_test_min_timer" and "flp_test_max_timer." The value for "flp_test_min_timer" must be between 5 and 25 μ s. The value for "flp_test_max_timer" must be between 165 and 185 μ s. This test is to verify that the device under test accepts FLP bursts with pulses spaced within these ranges, and refuses FLPs with pulses spaced outside of these ranges.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A: flp test min timer

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT enough pulses spaced at 5µs to identify the link partner as auto-negotiation able (refer to #28.2.9), wait 16ms, then send enough valid FLP bursts to put the DUT into the Acknowledge Detect state. The proper number of FLP bursts should be one less than the value determined in #28.2.1 as that value includes the FLP required to identify a device as auto-negotiation able.
- 3. Observe whether the DUT entered the Acknowledge Detect state
- 4. Repeat steps 1 through 3 varying the pulse spacing until the DUT enters the Acknowledge Detect state

Part B: flp test max timer

5. Repeat steps 1 through 3 varying the pulse spacing, starting at 185µs until the DUT enters the Acknowledge Detect state

- In Part A, the flp_test_min_timer should lay between 5µs and 25µs
- In Part B, the flp test max timer should lay between 165 \mu s and 185 \mu s

Test #28.2.11: Range of Data Detect Timer

Purpose: To verify that the device under test accepts data pulses with proper spacing and refuses data pulses with spacing outside the acceptable range.

References:

 ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.2.1, 28.3.2, Figure 28-15 Receive state diagram

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: As well as characteristic requirements, FLP bursts have requirements for the delay between clock and data pulses within the burst. In order to be accepted as valid, received data pulses must have a delay between them and the previous clock pulse between "data_detect_min_timer" and "data_detect_max_timer." The value for "data_detect_min_timer" must be between 15 and 47 μs. The value for "data_detect_max_timer" must be between 78 and 100 μs. This test is designed to verify that the device under test accepts FLP bursts with data pulses spaced within these ranges, and ignores NLPs with data pulses spaced outside of these ranges. As defined in Figure 28-15, if an FLP containing the data pattern 1,0 is sent with the data 1 transmitted a time exceeding 100 μs following the clock pulse, then the data_detect_max_timer should be violated. In a conformant device, this should result in the interpretation of the data pattern as 0,1. Thus, by alternating the transmission of this test FLP with FLPs containing typical spacing, a conformant device should not enter the Acknowledge Detect state. This technique is used to test the validity of data_detect_max_timer.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A: data_detect_min_timer

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send the DUT enough FLPs, alternating between FLPs with the first data pulse spaced 15µs from the clock pulse and FLPs with perfect spacing, to put it into the Acknowledge Detect state (see test #28.2.1)
- 3. Observe whether the DUT entered the Acknowledge Detect state
- 4. Repeat steps 1 through 3, varying the gap from the clock pulse to the data pulse until the DUT enters the Acknowledge Detect state

Part B: data_detect_max_timer

5. Repeat steps 1 through 3, varying the gap from the clock pulse to the data pulse, starting at 100μs, until the DUT enters the Acknowledge Detect state

Part C: ignoring pulses below data detect min timer

6. Repeat steps 1 through 3, changing the FLP to contain two "data" pulses, one before the implemented data_detect_min_timer is finished, and another after the data_detect_min_timer is finished.

Observable Results:

Part A:

• The data_detect_min_timer should lay between 15µs and 47µs

Part B:

The data_detect_max_timer should lay between 78μs and 100μs

Part C:

• The DUT should ignore the first data pulse and decode the second data pulse as a logic one causing the DUT to enter the Acknowledge Detect State

Test #28.2.12: Consistency Match

Purpose: To verify that the device under test performs a consistency match test on received FLPs.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.3.1

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Upon entering the Acknowledge Detect state of the auto-negotiation process, a device must receive 3 consecutive and consistent FLPs from its link partner before it can proceed. However, these FLPs must not only be consistent amongst themselves, but also with the FLPs that the device received to put it into the Acknowledge Detect state. To ensure this, a station must perform a consistency match test. If a consistency mismatch occurs, the device should enter the Transmit Disable state and cease sending FLPs. This test is designed to verify that the device under test checks to be sure that the FLPs received in the Acknowledge Detect state are consistent (ignoring the Acknowledge bit) with the FLPs that it received to get it there.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send a series of FLPs- first some with the Acknowledge bit not set (enough to put the DUT into the Acknowledge Detect state- refer to results of test #28.2.1) followed by 3 with the Acknowledge bit set to logic one and different advertised abilities than the initial FLPs
- 3. Monitor the transmit line coming from the DUT

Observable Results:

• The DUT should cease transmitting FLPs once the inconsistent FLPs are received

Test #28.2.13: Range of Break Link Timer

Purpose: To verify that the device under test recognizes a broken link and restarts the auto-negotiation process within the acceptable range.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.2.3.2, 28.3

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once a device has entered the Transmit Disable state, it must wait a specified amount of time before it restarts the auto-negotiation process. This time is defined by the device's "break_link_timer," and is required to be between 1200 and 1500 ms. This test is designed to verify that the device under test restarts the auto-negotiation process after entering the Transmit Disable state within this range.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send the same series of FLP bursts as in test #28.2.12 to put the DUT into the Transmit Disable state
- 3. Verify that the DUT starts a renegotiation
- 4. Measure the amount of time between when the station entered the Transmit Disable and when the first FLP of the renegotiation process was transmitted, and this will be the value of break link timer

Observable Results:

• The DUT's break_link_timer should be in the range 1200 to 1500 ms

Test #28.2.14: Range of Link Fail Inhibit Timer

Purpose: To verify that the device under test will wait a specified amount of time between when it parallel detects a link partner and when it establishes that link.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.2.3.2, 28.3

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once a device has entered the FLP LINK GOOD CHECK state, it must receive a link_status=OK message from its link partner within a specified amount of time. If this message is not received, it will enter the Transmit Disable state and wait for the duration of its break_link_timer before starting a renegotiation. This time is defined by the device's "link_fail_inhibit_timer," and is required to be between 750 and 1000 ms. This test is designed to verify that the device under test enters the Transmit Disable state from the FLP LINK GOOD CHECK state when a link_status=OK message is not received from its link partner in the acceptable range of time.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to put the device into the COMPLETE ACKNOWLEDGE state (see test #19.28)
- 3. Verify that the DUT starts a renegotiation
- 4. Measure the amount of time between when the station transmitted it's final FLP after entering the COMPLETE ACKNOWLEDGE state (see results of test #28.2.15) and when the first FLP of the renogotiation process was transmitted, and this will be the value of break_link_timer + link_fail_inhibit_timer
- 5. Subtract the value of break_link_timer (see results of test #28.2.13) from this value to acquire the value of link fail inhibit timer

Part B:

- 6. Repeat steps 1-3 above, changing the advertised abilities to include only 10Base-T abilities.
- 7. Measure the amount of time NLPs are sent from the DUT and verify it is also link fail inhibit timer.

Observable Results:

• In both parts, the DUT's link_fail_inhibit_timer should be the same and in the range 750 to 1000 ms

Test #28.2.15: Complete Acknowledge

Purpose: To verify that the device under test enters the Complete Acknowledge state only after receiving 3 consecutive and consistent FLPs with the Acknowledge bit set, and then sends out a valid number of link code words after the Complete Acknowledge state has been entered.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.2.1.2.4

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Well into the auto-negotiation process is the Complete Acknowledge state. A station reaches this state after first entering the Acknowledge Detect state (which is done when at least 3 complete, consecutive and consistent FLP bursts are received, ignoring the Acknowledge bit- see Test #28.2.1), and then receiving 3 complete, consecutive and consistent FLPs with the Acknowledge bit set. Once the Complete Acknowledge state has been entered, a station should send out 6 to 8 (inclusive) more FLPs containing its link code word and with the Acknowledge bit set to 1. This test is designed to verify that the device under test sends out 6 to 8 (inclusive) FLPs after entering the Complete Acknowledge state, and requires the reception of 3 consecutive and consistent FLPs with the Acknowledge bit set before doing so.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send a series of FLPs- first some with the Acknowledge bit not set (enough to put the DUT into the Acknowledge Detect state- refer to results of test #28.1.3) followed by 3 with the Acknowledge bit set to logic one, to put the DUT into the COMPLETE ACKNOWLEDGE state
- 3. Monitor the transmit line coming from the DUT and count the number of FLPs sent by the DUT after the COMPLETE ACKNOWLEDGE state has been entered

Part B:

- 4. Repeat steps 1-2 above, but send FLPs whose Acknowledge bits alternate between 0 and 1
- 5. Monitor the transmit line coming from the DUT and count the number of FLPs sent by the DUT with the Acknowledge bit set to 1

Part C:

- 6. Repeat Steps 1-2 above, but send FLPs only advertising 10Base-T abilities
- 7. Follow the previous sequence with 10 NLPs and determine if the DUT entered FLP Link Good State

Observable Results:

Part A:

• After COMPLETE ACKNOWLEDGE state has been entered, the DUT should send out 6 to 8 (inclusive) FLPs containing its Link Code Word. Following the FLPs should be a gap of link_fail_inhibit_timer + break_link_timer until FLP transmission resumes.

Part B:

• The DUT should never enter the COMPLETE ACKNOWLEDGE state, and should send out FLPs with the Acknowledge bit set until nlp_test_max_timer expires. Following the FLPs should be a gap of 'break_link_timer' until FLP transmission resumes.

Part C:

• The DUT should enter the FLP Link Good State and then halt for approximately break_link_timer before resuming FLP transmission from the Ability Detect State.

Test Group 3: Establishing a Link

Test #28.3.1: Range of Link Loss Timer

Purpose: To verify that the device under test implements link_loss_timer within 50ms and 150ms.

References:

- ANSI/IEEE Std 802.3 1998 Edition: Section 28.3, Figures 28-16 & 28-17
- · ANSI/IEEE Std 802.3 1993 Edition: Section 14.2.1.7

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once a 10Base-T link has been detected, the link should not fail unless frames or link test pulses are not received for a period of time governed by the link_loss_timer.

Test Setup: See Figure 28.2.1-1.

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT a sufficient number of link pulses to cause the device to enter the FLP Link Good Check state. Follow this by a gap and repeat the pattern continuously.
- 3. Observe the line and determine if the DUT ever dropped the link.

Observable Results:

• The DUT should keep link with the a gap within 50ms and 150ms

Test #28.3.2: Link Count Max

Purpose: To verify that the device under test implements lc_max within 2 to 10 link test pulses.

References:

- ANSI/IEEE Std 802.1998 Edition: Section 28.3, Figures 28-16 & 28-17
- ANSI/IEEE Std 802.3 1993 Edition: Section 14.2.3.1, Figure 14-12

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: When a device implementing a 10Base-T PMA begins to receive link test pulses conformant to Figure 14-12, it must indicate link_status [NLP]=READY after 'lc_max' number of pulses have been received. According to Figure 28-16, once link_status [NLP]=READY is indicated, the device should cease transmitting FLPs. To prevent a device from indicating link off a received FLP, the state machine depicted in Figure 28-17 resets if a pulse is received before the link_test_min_timer has expired. This test is designed to verify that the implemented value of lc_max is between 2 and 10 pulses (inclusive).

Test Setup: See Figure 28.2.1-1.

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT 6 pulses spaced at 16ms.
- 3. Determine whether the DUT has ceased transmitting FLPs
- 4. If the DUT did not cease FLP transmission, repeat steps 1 through 3 varying the number of pulses sent until the DUT ceases FLP transmission.

Observable Results:

• The DUT should cease FLP transmission for approximately link_loss_timer after receiving between 2 to 10 link test pulses

Test #28.3.3: Single Link Ready

Purpose: To verify that the device under test properly monitors the status of single_link_ready during parallel detection.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.3, Figures 28-16 & 28-17

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: When a device implementing a 10Base-T PMA begins to receive link test pulses it must indicate link_status[NLP]=READY after 'lc_max' number of pulses have been received. According to Figure 28-16, once link_status[NLP]=READY is indicated, the device should cease transmitting FLPs and start autoneg_wait_timer. Single_link_ready is then used to indicate if exactly one PMA is currently ready. If any more or fewer than a single link is simultaneously ready then single_link_ready=false, mr_parallel_detection_fault=true, and FLP transmission should resume "immediately". This test is designed to verify that the process described above functions appropriately.

Test Setup: See Figure 28.2.1-1.

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT 'lc max' pulses spaced at 16ms.
- 3. Determine the duration for which the DUT has ceased transmitting FLPs

Observable Results:

• The DUT should cease FLP transmission for approximately link loss timer

Test #28.3.4: Range of Link Test Timers

Purpose: To verify that the device under test accepts NLPs (link test pulses) with proper spacing, and refuses those with spacing outside of the acceptable range.

References:

- ANSI/IEEE Std 802.1998 Edition: Sections 28.3, Figure 28-17
- ANSI/IEEE Std 802.3 1993 Edition: Section 14.2.1.7

Resource Requirements

- Traffic Generator
- Line Monitor

Last Modification: May 5, 1999

Discussion: The acceptable gap between NLPs (10Base-T link test pulses) is defined to be between "link_test_min_timer" and "link_test_max_timer". The value for "link_test_min_timer" must be between 2 and 7 ms. The value for "link_test_max_timer" must be between 25 and 150 ms. This test is designed to verify that a device implementing a 10Base-T PMA will establish a 10Base-T link upon receipt of NLPs with valid spacing, and refuses link with spacing outside of these ranges.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A: link test min timer

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT lc_max link pulses spaced at 7ms apart to cause it to enter the Parallel Detect State
- 3. Determine whether the DUT entered the Parallel Detect State by monitoring the DUT for any delay in FLP transmission
- 4. Repeat steps 1 through 3 varying the spacing of the link pulses until the DUT fails to enter the Parallel Detect State

Part B: link test max timer

- 5. Repeat steps 1 through 3 varying the spacing of the link pulses from 25ms and higher *Part C*:
- 6. Repeat steps 1-3 sending link pulses continuously and spaced closer together than the determined link_test_min_timer

Observable Results:

Part A:

• The link_test_min_timer should lay between 2ms and 7ms

Part B:

• The link_test_max_timer should lay between 25ms and 150ms

Part C:

• The device should never enter the Link Status Check State

Test #28.3.5: Range of Auto-Negotiation Wait Timer

Purpose: To verify that the implemented value of autoneg_wait_timer is within the specified range of 500 to 1000ms.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.3.2, Figure 28-16 Arbitration state diagram

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: In order for an auto-negotiation able device to properly parallel detect a link partner, it must receive a valid single link ready=true signal from its link partner for a period of time before it negotiates to that link. This time is defined by the device's "autoneg_wait_timer," and is specified to be between 500 and 1000 ms. This test is designed to verify that the device under test does not parallel detect to a link before waiting a time within this range. This timer cannot be measured precisely from the RJ-45 interface, however, it's can be bounded. The upper bound can be established by causing a single link to be ready and observing the gap between cessation of FLPs and commencement of the link pulses/stream. This delay includes any inter-FLP gap that the device may be in the midst of when detection of a single link ready occurs. Additionally, any delay from the proper link being enabled to actual signaling appearing on the line will add to the value of the observed gap. The lower bound may be established for devices implementing a 10Base-T PMA by first determining the implemented values of lc_max and link_loss_timer. With these values known, the DUT can be sent a burst of a link test pulses corresponding to lc_max plus the duration of autoneg_wait_timer found for the upper bound. The number of pulses in the burst may then be decreased until the DUT is observed to source FLPs following reception of the pulses, instead of NLPs (10Base-T link). This transition identifies the range of the lower bound. This range should be autoneg wait timer minus the time required to detect single link ready=false.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the station valid NLPs continuously with valid spacing
- 3. Monitor the DUT's transmit line
- 4. Verify that the DUT establishes a 10Base-T link
- 5. Measure the time between when the DUT ceased transmission of FLPs and when the DUT began transmitting NLPs. The minimum of these observations is the upper bound of autoneg_wait_timer
- 6. Break link, and calculate the number of NLPs to send to satisfy: X*NLP_gap = 'upper bound of autoneg_wait_timer'.
- 7. Send $X + lc \max NLPs$ at a gap of 'NLP gap' to the DUT.
- 8. Repeat step 7, decreasing X until the DUT sources FLPs following cessation of the NLPs from the Traffic Generator. (the gap should be approximately link loss timer)

Observable Results:

• The DUT's autoneg_wait_timer should be in the range of 500 to 1000 ms

Possible Problems:

• If only the upper or lower bound lays outside the conformance window, then the autoneg_wait_timer cannot be found conformant nor non-conformant.

Test #28.3.6: Link Integrity and RD Active

Purpose: To verify that the device under test maintains 10Base-T link upon reception of valid 10Base-T frames.

References:

- ANSI/IEEE Std 802.3u October 26, 1995 Edition: Sections 28.3, Figure 28-17
- ANSI/IEEE Std 802.3 1993 Edition: Section 14.2.3.1, 14.3.1.3.2 Figures 14-16, 14-17

Resource Requirements

- Traffic Generator
- Line Monitor

Last Modification: May 5, 1999

Discussion: Auto-negotiating devices implementing a 10Base-T PMA must support Figure 28-17 "NLP Receive Link Integrity Test state diagram", unlike legacy 10Base-T implementation which follow Figure 14-6 "Link Integrity Test Function State Diagram". The significant difference between these figures is that link may not be established based on the reception of 10Base-T frames (indicated as RD=active). However, once a 10Base-T link is ready, reception of either link test pulses or 10Base-T frames may maintain the link. However, as indicated in section 14.3.1.3.2, reception of signaling not meeting the requirements of Figures, 14-16, or 14-17 should not be accepted as RD=active. This includes 100Base-TX signaling.

Test Setup: See Figure 5.28-1

Procedure:

Part A: Link maintenance via RD=active

- 1. Establish a connection (not a link) to the DUT
- 2. Use a Traffic Generator to send the DUT 'lc_max' link pulses spaced at 16ms followed by validly formed 10Base-T frames spaced at 16ms
- 3. Determine whether the DUT entered into a good link by determining if it is sending NLPs. Also, if the means exists, determine if the DUT received the frames after link control[NLP]=ENABLE occurs.

Part B: Refusal of link based on RD=active

- 4. Establish a connection (not a link) to the DUT
- 5. Use a Traffic Generator to send the DUT validly formed 10Base-T frames spaced at 16ms for a duration exceeding autoneg_wait_timer
- 6. Determine whether the DUT entered into a good link by determining if it is sending NLPs. Also, if the means exists, determine if the DUT received any of the frames

Part C: Refusal of link maintenance upon reception of 100Base-TX signaling

- 7. Establish a connection (not a link) to the DUT
- 8. Use a Traffic Generator to send the DUT 'lc_max' link pulses spaced at 16ms, then 100Base-TX signaling for several seconds, followed by validly formed 10Base-T frames spaced at 16ms
- 9. Determine whether the DUT remains in a 10Base-T link by monitoring if it is sending out NLPs throughout the process. Also, if the means exists, determine if the DUT received any of the frames

Observable Results:

Part A:

 Once the device enters the FLP LINK GOOD state, the DUT should be sending out NLPs and receiving the frames

Part B:

• The DUT should never establish a link, and thus, never send out NLPs and never receive the frames

Part C:

• The DUT should exit break its 10Base-T link and parallel detect to 100Base-TX upon reception of the 100Base-TX idle. Once it is switched back to the 10Base-T frames, the 100Base-TX link should be broken and no link should be formed by the detection of the frames. Also, none of the frames sent after the 100Base-TX idle should be received

Test #28.3.7: Parallel Detection of 10Base-T Devices

Purpose: To verify that the device under test can detect that its link partner is a fixed speed 10Base-T device.

References:

- ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.2.2, 28.2.3.1, 28.4
- ANSI/IEEE Std 802.3, 1993 Edition: Section 14.3.1.2.1

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: A station capable of auto-negotiation should also implement the parallel detection function. This provides for the detection of a 10Base-T fixed speed device before the detection of FLPs. In this case, a station should either enable its 10Base-T PMA if supported and establish a link, or otherwise not allow a link to be established. This test is designed to verify that the device under test properly handles the presence of a fixed speed 10Base-T device as a link partner.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to simulate the presence of a non-auto-negotiating 10Base-T device
- 3. If the DUT has a 10Base-T PMA, verify that it is enabled by determining whether a link is established
- 4. Send the DUT a packet and see if it is accepted
- 5. If the DUT has no 10Base-T PMA, verify that no link is established

Observable Results:

• If the DUT supports a 10Base-T PMA, a link should be established in each case. If not, a link should be refused.

Test #28.3.8: Parallel Detection of 100Base-TX Devices

Purpose: To verify that the device under test can properly parallel detect a fixed speed 100Base-TX link partner.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.2.3.1

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: A station capable of auto-negotiation should also implement the parallel detection function. This provides for the detection of a 100Base-TX fixed speed device before the detection of FLPs. In this case, a station should either enable its 100Base-TX PMA if supported and establish a link, or otherwise not allow a link to be established. This test is designed to verify that the device under test properly handles the presence of a fixed speed 100Base-TX device as a link partner.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to simulate the presence of a non-auto-negotiating 100Base-TX device
- 3. If the DUT has a 100Base-TX PMA, verify that it is enabled by determining whether a link is established
- 4. Send the DUT a packet and see if it is accepted
- 5. If the DUT has no 100Base-TX PMA, verify that no link is established

Observable Results:

• If the DUT supports a 100Base-TX PMA, a link should be established. If not, a link should be refused.

Test #28.3.9: Parallel Detection of 100Base-T4 Devices

Purpose: To verify that the device under test can properly parallel detect a fixed speed 100Base-T4 link partner.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.2.3.1

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: A station capable of auto-negotiation should also implement the parallel detection function. This provides for the detection of a 100Base-T4 fixed speed device before the detection of FLPs. In this case, a station should either enable its 100Base-T4 PMA if supported and establish a link, or otherwise not allow a link to be established. This test is designed to verify that the device under test properly handles the presence of a fixed speed 100Base-T4 device as a link partner.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to simulate the presence of a non-auto-negotiating 100Base-T4 device
- 3. If the DUT has a 100Base-T4 PMA, verify that it is enabled by determining whether a link is established
- 4. Send the DUT a packet and see if it is accepted
- 5. If the DUT has no 100Base-T4 PMA, verify that no link is established

Observable Results:

• If the DUT supports a 100Base-T4 PMA, a link should be established. If not, a link should be refused.

Test #28.3.10: Priority Resolution Function

Purpose: To verify that the device under test properly configures the highest common denominator (HCD) technology for the transmitted technologies in a link code word.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.3.3, Annex 28B.2, 28B.3

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once a station has received its link partner's link code word and completed the exchange of FLP bursts, the technology at which communication is to be established must be resolved. Through the priority resolution function, the highest common denominator (HCD) technology should be found. This test is designed to verify that the device under test resolves the proper HCD for all possible technology combinations.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send a series of FLP bursts that advertise a set of abilities
- 3. Verify that the DUT establishes a link when it can, and refuses a link otherwise
- 4. Verify that the DUT resolved the highest common technology by sending a packet to the DUT in that format and determining whether it was received
- 5. Verify that full duplex was resolved whenever possible
- 6. Repeat this procedure for all possible combinations of the first five bits of the technology ability field

Observable Results:

• In every case, the DUT should resolve the highest priority possible based on the priority resolution function for the technologies advertised

Test #28.3.11: Failed Link for HCD

Purpose: To verify that the device under test starts a renegotiation upon the reception of a link_status=FAIL from the resolved highest common denominator (HCD) technology.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.2.3.2

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once the highest common denominator (HCD) technology has been determined through the parallel detection function, if a station receives a link_status=FAIL message from that priority, it should cause a renegotiation. This test is designed to verify that the device under test does start a renegotiation upon the receipt of a link_status=FAIL message from the HCD technology.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send enough NLPs to put the DUT into the Flp Link Good state
- 3. Verify the DUT resolves the HCD priority and establishes a link
- 4. Send the DUT a link_status=FAIL for the HCD priority
- 5. Verify that the DUT starts a renegotiation

Observable Results:

• The DUT should start a renegotiation upon reception of the link status=FAIL message

Test Group 4: Next Page Functionality

Test #28.4.1: Transmitted Next Pages

Purpose: To verify that the device under test transmits next pages with valid characteristics after completion of link code word transmission.

References:

- ANSI/IEEE Std 802.3 1998 Edition: Sections 28.1.4.1, 28.2.1.1, 28.2.1.1.1, 28.2.1.1.2, 28.4
- ANSI/IEEE Std 802.3, 1993 Edition: Section 14.3.1.2.1, Figure 14-3

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: After completing the exchange of link code words, if two stations both advertise next page functionality, they are required to send out at least one next page. All next pages are required to meet the same timing and electrical specifications as all other FLPs. This test is designed to verify that a device advertising next page functionality sends out at least one next page and that its next pages have the same timing and electrical characteristics as its other FLPs.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send the DUT a series of FLPs with the next page bit set to a logic one to put it through the Complete Acknowledge state (see test #28.2.15)
- 3. Send the DUT a sequence of next pages containing the null message code, consisting of first the number required with the Ack bit set to zero to put the DUT into the Acknowledge Detect state (see test #28.2.1), followed by 9 with the Ack bit set to one to get the DUT through the Complete Acknowledge state and into the NEXT PAGE WAIT state
- 4. Verify that the DUT transmits a next page after completion of the Complete Acknowledge state (see test #28.2.15)
- 5. Capture a single next page and verify that it meets the requirements of tests #28.1.1, #28.1.2, #28.1.3 and #28.1.4

- The device should transmit at least one next page after completion of the Complete Acknowledge state
- The next pages should meet the requirements of tests #28.1.1, #28.1.2, #28.1.3 and #28.1.4

Test #28.4.2: Next Page Consistency Match

Purpose: To verify that the device under test performs a consistency match test on received next pages.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Section 28.3.1

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: This test is virtually identical to test #28.2.12, but is repeated here to verify that the consistency match test is carried through to the next page exchange process and is performed on next pages. See test #28.2.12 for full details.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send the DUT enough FLPs to get it through the Complete Acknowledge state (see test #28.2.15)
- 3. Send a series of message pages- first some with the Acknowledge bit not set (enough to put the DUT into the Acknowledge Detect state- refer to results of test #28.2.1) followed by 3 with the Acknowledge bit set to logic one and bit D10 holding the opposite value as the initial 4 message pages
- 4. Monitor the transmit line coming from the DUT

Observable Results:

• The DUT should cease transmitting next pages immediately once the inconsistent message pages are received

Test #28.4.3: Null Message Page

Purpose: To verify that the device under test transmits proper Null Message pages if it completes sending Message and Unformatted Pages before its link partner.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.3.4, 28.2.3.4.1, 28.2.3.4.7, 28.2.3.4.8, 28.2.3.4.11, Annex 28C, 28C.2

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once a device has finished sending Message and Unformatted next pages, it is required to send Null Message pages until its link partner is done as well. A null page is defined as a Message Page that contains the null message code 0 0 0 0 0 0 0 0 0 0 0 1 (bits M[10:0]). This test is designed to verify that once the device under test completes its transmission of Message and Unformatted Pages, it sends out valid Null Message pages until its link partner is done as well. Alternatively, a device may solely transmit next pages containing Null Message codes with the next page bit set. Once a Null Message page is received from the device's partner, a final Null Message page without the next page bit should be sent. This would allow a device with no next page data to transmit, to still receive next page information from it's link partner.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A: Auto-Negotiation Next Page session extension via Null Messages

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send the DUT enough FLPs to put it through the Complete Acknowledge state (see test #28.2.15)
- 3. Send the DUT two more next pages (not null pages) than Message or Unformatted codes that it has to transmit (for example, if a station has two next pages to transmit before beginning to transmit null pages, send it four next pages)
- 4. Monitor the next pages transmitted by the DUT
- 5. Verify that the last two next pages sent by the DUT contained the null message code

Part B: Auto-Negotiation Next Page exchange using Null Messages only

6. Repeat sending two more Null Message next page than Message or Unformatted pages that the DUT has to transmit. (the last page sent does not have the next page bit set)

- The DUT's last two next pages should contain the null message code
- The NP bit in the last null message should be set to 0

Test #28.4.4: Next Page Bit

Purpose: To verify that the device under test makes proper use of the next page bit throughout the next page exchange process.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.2.1.2.5, 28.2.3.4, 28.2.3.4.1, 28.2.3.4.2, 28.2.3.4.11

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: During the exchange of next pages, the NP bit plays a simple role. It is to have the value 1 if a station has further next pages to transmit, and 0 if it is transmitting its last page of information. Once both a device and its link partner have transmitted all of their next pages, the next page process should end and a link should be established. If a device's partner finishes transmitting message or unformatted pages before the device and is sending out null pages, then the device should go directly from its last message or unformatted page to a link. If both devices transmit their last message or unformatted page at the same time, they should both go straight to a link and no null pages should be sent. This test is designed to verify that the device under test properly sets the NP bit throughout the next page process, and does not transmit any null pages if its link partner either finishes transmitting its message and unformatted pages before it or at the same time that it does.

Test Setup: See Figure 28.2.1-1

Procedure:

Part A:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send the DUT enough FLPs to put it through the Complete Acknowledge state (see test #28.2.15)
- 3. Send the DUT two less next pages than message or unformatted pages that it has to transmit, followed by two null pages (for example, if a device has three next pages to transmit, send it one next page followed by two null pages)
- 4. Monitor the next pages transmitted by the DUT
- 5. Verify that the DUT concludes its next page exchange

Part B:

6. Repeat steps 1 through 5 with the following modification to step 3: send the DUT the same number of next pages that it has message and unformatted pages to transmit (for example, if a device has three next pages to transmit, send it three next pages) with the NP bit of the last page set to 0

- The DUT should set the NP bit to 0 for the last message or unformatted page that it sends
- For all next pages preceding the last page, the NP bit should be set to 1
- In both cases, the DUT should conclude the next page exchange

Test #28.4.5: Toggle Bit

Purpose: To verify that the device under test properly alternates values of 0 and 1 in the toggle bit position (bit D11) of its next pages, and checks to see if its received next pages follow this pattern.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.2.3.4, 28.2.3.4.1, 28.2.3.4.6

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: During next page exchange, the toggle bit (bit D11) of the transmitted next pages serves a simple purpose. The value of this bit alternates between 0 and 1 in consecutive pages, and therefore provides the receiving station with a quick and easy check to verify that it is receiving next pages in the proper order. Therefore, it is important that the DUT sets these bits properly, starting with its first next page, whose toggle bit value takes the opposite value of bit D11 in the device's link code word. If a device receives consecutive pages without the toggle bit toggled, it should sit in the NEXT PAGE WAIT state until it receives a next page with the proper toggle bit value. This test is designed to verify that the device under test sets the toggle bit properly throughout the exchange of next pages, and makes sure that its received next pages are toggled properly as well.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send enough FLPs to put the DUT through the Complete Acknowledge state (see test #28.2.15)
- 3. Send the DUT enough next pages to allow it to send all of its message and unformatted pages with the following modification: reverse the values of the toggle bit of the last 2 pages (by doing this, you end up with toggle values of either 0 0 1 or 1 1 0 for the last 3 pages)
- 4. Monitor the transmitted next pages
- 5. Verify that the DUT sets the toggle bit properly in all of its next pages

- The value of the toggle bit in the first next page should have the opposite value of bit D11 in the DUT's link code word
- The value of the toggle bit of the next page transmitted by the DUT's should always take the opposite value of the toggle bit of the previous next page (if the previous value was a 0, it should be a 1, and vice versa)
- The DUT should not leave the NEXT PAGE WAIT state on reception of the second to last page, but should accept the last page and conclude the next page exchange

Test #28.4.6: Message and Unformatted Pages

Purpose: To verify that the device under test transmits properly formatted message and unformatted pages.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.2.3.4, 28.2.3.4.1, 28.2.3.4.4, 28.2.3.4.7, 28.2.3.4.8, 28.2.3.4.9, 28.2.3.4.10, 28.2.3.4.11, Annex 28C (all parts)

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: There are two types of pages that a device may send as next pages: message or unformatted pages. Each type of page has its own formatting. Message pages contain an 11-bit message code field that can contain only a few defined encodings. Unformatted pages contain an 11-bit wide unformatted code field whose encoding is arbitrary. There is also an MP bit, which is required to be set to 1 if the page is a message page, and 0 if it is an unformatted page. If the selector fields in the device's and its link partner's link code words do not match, then every series of unformatted pages must be preceded by a message page that specifies how they should be interpreted. Otherwise, the device is permitted to transmit unformatted pages whenever it desires (this is not a behavior that is expected, but could conceivably occur). This test is designed to verify that the DUT's message pages contain an acceptable message code followed by the appropriate number of unformatted pages (see Annex 28 for the message codes and appropriate number of unformatted pages), and all pages have the MP bit set correctly.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send enough FLPs to put the DUT through the Complete Acknowledge state, followed by enough null pages to allow the DUT to transmit all of its next pages
- 3. Monitor the next pages transmitted by the DUT
- 4. Verify that the message code field in each message page is valid
- 5. Verify that the correct number of unformatted pages is sent after each message page
- 6. Verify that the MP bit is set correctly in all next pages

- The message pages (including null pages) should contain a message code (bits D[0-10]) with a defined value from Annex 28C
- All message pages should be followed by the number of unformatted pages required by its message code field (see Annex 28C)
- The MP bit should be set to 1 in all message pages and 0 in all unformatted pages

Test #28.4.7: Reception of Next Pages

Purpose: To verify that the device under test properly receives message and unformatted pages, for both existing message codes as well as reserved.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.1.2, 28.2.3.4, 28.2.3.4.1, 28.2.3.4.4, 28.2.3.4.7, 28.2.3.4.8, 28.2.3.4.9, 28.2.3.4.10, 28.2.3.4.11, Annex 28C

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: A device supporting next page exchange should be capable of receiving a wide variety of next pages from its link partner. It should properly accept all sequences of message pages and unformatted pages that are attainable from the defined message code fields in Annex 28C. However, it should also be capable of receiving message and unformatted page combinations not yet defined by simply ignoring them. If defined and undefined combinations are mixed, the device should be able to recognize all of the message codes that are defined and ignore those that are not. Presently, there is no way of confirming whether a device ignores or accepts a next page, unless it drops link or reports an error on the reception of an undefined page, so this test is difficult to perform.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send enough FLPs to put the DUT through the Complete Acknowledge state
- 3. Send the device the following sequence of next pages:
 - An unformatted page
 - The first 3 defined (not including the null message code) message and unformatted page sequences defined in Annex 28C
 - A message page containing an undefined encoding for the message code field followed by 3 unformatted pages
 - The other 3 defined sequences
 - If the link partner has not finished transmission of message and unformatted pages, transmit the appropriate number of null pages
- 4. Monitor the next pages transmitted by the DUT
- 5. Verify that the DUT concludes its next page exchange

- The DUT should accept all defined combinations
- The DUT should ignore the first unformatted page as well as the undefined combination
- The DUT should conclude its exchange of next pages

Test #28.4.8: Transmit Disable

Purpose: To verify that the device under test enters the TRANSMIT DISABLE state from the NEXT PAGE WAIT state if flp_receive_idle becomes true.

References:

 ANSI/IEEE Std 802.3 1998 Edition: Sections 28.3.1, Figure 28-16 Arbitration State Diagram

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once the next page exchange process has begun, if a device's link partner for some reason stops sending next pages, the device should cease transmission as well. When in the NEXT PAGE WAIT state, if a device detects flp_receive_idle=true, then it should immediately transition to the TRANSMIT DISABLE state. This test is designed to verify that the device under test exits the next page exchange process if flp_receive_idle becomes true.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send the DUT enough FLPs to put it through the Complete Acknowledge state (see test #28.2.15)
- 3. Send the DUT a message page with the NP bit set to 1 (going through the Complete Acknowledge state), then cease transmission of next pages
- 4. Verify that the DUT enters the TRANSMIT DISABLE state

Observable Results:

• After the expiration of nlp_max_timer, the device should enter the TRANSMIT DISABLE state and cease transmission of next pages

Test #28.4.9: Priority Resolution Following Next Page Exchange

Purpose: To verify that the device under test properly configures the highest common denominator (HCD) technology for the transmitted technologies in a link code word, following a next page exchange.

References:

• ANSI/IEEE Std 802.3 1998 Edition: Sections 28.2.3.3, 28.2.4.1.4, Annex 28B.2, 28B.3

Resource Requirements:

- Line Monitor
- Traffic Generator

Last Modification: May 5, 1999

Discussion: Once a station has received its link partner's link code word and completed the exchange of any next page FLP bursts, the technology at which communication is to be established must be resolved. Through the priority resolution function, the highest common denominator (HCD) technology should be found. Similar to test #28.3.10- Priority Resolution Function, this test is designed to verify that the device under test resolves the proper HCD for all possible technology combinations, even after a lengthy next page exchange. This test is targeted specifically to verify that a device implementing Next Page functionality does not "lose" information if the Auto-Negotiation link partner ability register is overwritten with the received next page data.

Test Setup: See Figure 28.2.1-1

Procedure:

- 1. Establish a connection (not a link) to the DUT
- 2. Use the Traffic Generator to send a series of FLPs (base and next page) that advertise a set of abilities
- 3. Verify that the DUT establishes a link when it can, and refuses a link otherwise
- 4. Verify that the DUT resolved the highest common technology by sending a packet to the DUT in that format and determining whether it was received
- 5. Repeat this procedure for all possible combinations of the advertised technology abilities

Observable Results:

• In every case, the DUT should resolve the highest priority possible based on the priority resolution function for the technologies advertised