

Ethernet

Clause 22, 28, and 40 Management Registers Test Suite V3.0

Technical Document



Last Updated: Thursday, July 20, 2006 4:13 PM

*University of New Hampshire
InterOperability Laboratory
Ethernet Consortium*

*121 Technology Drive, Suite 2
Durham, NH 03824
Phone: (603) 862-0166
Fax: (603) 862-4181*

<http://www.iol.unh.edu/consortiums/fe>
<http://www.iol.unh.edu/consortiums/ge>

Fast Ethernet will only perform Groups 1 and 2.
Gigabit Ethernet will perform Groups 1, 2, and 3.

MODIFICATION RECORD

- **July 20, 2006 Version 3.0**
Matthew Hersh:
Updated the discussion, procedure and observable results for test:
 - Test #28.2.9 – mr_next_page_loaded
- **June 16, 2006 Version 2.9**
Matthew Hersh:
Updated the discussion, procedure and observable results for test:
 - Test #28.2.9 – mr_next_page_loaded
- **May 26, 2006 Version 2.8**
Matthew Hersh:
Updated procedure for test:
 - Test #28.2.8 – AN Link Partner Next Page Ability Register and Next Page Location Bits
- **June 6, 2005 Version 2.7**
Mike Henninger: Updated references to IEEE std. 802.3 - 2005
- **June 6, 2005 Version 2.6**
Matthew Hersh:
Updated observable results and possible problems for test:
 - Test #28.2.5 – Page Received Setting/ResettingUpdated the procedure for tests:
 - Test #28.2.7 – AN Next Page Transmit Register
 - Test #28.2.11 – Link Partner Next Page Able
 - Test #40.3.1 – 1000BASE-T MASTER/SLAVE Control Register bits 9.10:8
 - Test #40.3.2 – 1000BASE-T MASTER/SLAVE Control Register bits 9.12:11
- **April 12, 2000 Version 1.0.0 Initial Release**

Previous versions of the test suite can be found at:

<http://www.iol.unh.edu/services/testing/fe/testsuites/>

*The University of New Hampshire
InterOperability Laboratory*

ACKNOWLEDGMENTS

The University of New Hampshire would like to acknowledge the efforts of the following individuals in the development of this test suite.

Milen Andonov	University of New Hampshire
Andy Baldman	University of New Hampshire
Chris Bancroft	University of New Hampshire
Matthew Hersh	University of New Hampshire
Jeremy Kent	University of New Hampshire
Roy Lavender	University of New Hampshire
Eric Lynskey	University of New Hampshire
Geoff Mitchell	University of New Hampshire
Bob Noseworthy	University of New Hampshire
Jake O'Dell	University of New Hampshire
Ben Schultz	University of New Hampshire
Karen Tuttle	University of New Hampshire
Ben Verschueren	University of New Hampshire
Erica Williamsen	University of New Hampshire

INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functioning of their Clause 22, Clause 28, and Clause 40 Auto-Negotiation based products. The tests do not determine if a product conforms to the IEEE 802.3, nor are they purely interoperability tests. Rather, they provide one method to isolate problems within an auto-negotiating device. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other auto-negotiating devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in most auto-negotiating environments.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross-references to the IEEE 802.3 standards and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification

*The University of New Hampshire
InterOperability Laboratory*

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure

The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

The observable results section lists observables that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may effect test results in certain situations.

TABLE OF CONTENTS

MODIFICATION RECORD	I
ACKNOWLEDGMENTS	II
INTRODUCTION.....	III
TABLE OF CONTENTS.....	V
GROUP 1: CLAUSE 22 MANAGEMENT FUNCTION REQUIREMENTS.....	1
TEST #22.1.1: MAIN RESET	2
TEST #22.1.2: AUTO-NEGOTIATION ENABLE.....	3
TEST #22.1.3: AUTO-NEGOTIATION RESTART	4
TEST #22.1.4: AUTO-NEGOTIATION COMPLETE.....	5
TEST #22.1.5: LINK STATUS	6
TEST #22.1.6: AUTO-NEGOTIATION ABILITY.....	7
TEST #22.1.7: REPORT PHY CAPABILITIES	8
TEST #22.1.8 DUPLEX MODE.....	10
TEST #22.1.9 SPEED SELECTION	12
GROUP 2: CLAUSE 28 MANAGEMENT REGISTERS	14
TEST #28.2.1: AN ADVERTISEMENT REGISTER	15
TEST #28.2.2: AN LINK PARTNER ABILITY REGISTER	17
TEST #28.2.3: REMOTE FAULT	19
TEST #28.2.4: PARALLEL DETECTION FAULT	20
TEST #28.2.5: PAGE RECEIVED SETTING/RESETTING	22
TEST #28.2.6: LINK PARTNER AUTO-NEGOTIATION ABLE	24
TEST #28.2.7: AN NEXT PAGE TRANSMIT REGISTER	25
TEST #28.2.8: AN LINK PARTNER NEXT PAGE ABILITY REGISTER AND NEXT PAGE LOCATION BITS	27
TEST #28.2.9: MR_NEXT_PAGE_LOADED.....	29
TEST #28.2.10: NEXT PAGE ABLE	31
TEST #28.2.11: LINK PARTNER NEXT PAGE ABLE.....	32
GROUP 3: CLAUSE 40 MANAGEMENT REGISTERS	34
TEST #40.3.1: 1000BASE-T MASTER/SLAVE CONTROL REGISTER BITS 9.10:8.....	35
TEST #40.3.2: 1000BASE-T MASTER/SLAVE CONTROL REGISTER BITS 9.12:11	37
TEST #40.3.3: 1000BASE-T MASTER/SLAVE STATUS REGISTER	39

GROUP 1: CLAUSE 22 MANAGEMENT FUNCTION REQUIREMENTS

Scope: The following tests cover Auto-Negotiation operation specific to the management register set.

Overview: These tests are designed to verify that the device under test properly implements the Media Independent Interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 22 (MII) of IEEE 802.3. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS ARE PERFORMED FOR BOTH FAST ETHERNET AND GIGABIT ETHERNET CONSORTIUMS. THESE TESTS CANNOT BE PERFORMED IF REGISTER ACCESS IS NOT PROVIDED.

Test #22.1.1: Main Reset

Purpose: To verify that bit 0.15 controls the resetting of the PHY and Auto-Negotiation process.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 22.2.4.1.1, 28.2.4.1.8, 28.3.1, Table 22-7, Table 28-8, Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: August 17, 2004

Discussion: Bit 0.15 of the Control Register gives management the ability to reset all of the Control and Status Registers, as well as restarting the Auto-Negotiation process.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Wait until the DUT has begun to transmit FLPs.
2. Set bit 0.15 in Register 0.
3. Observe transmissions from the DUT.
4. Read Register 0 (Control Register) and Register 1 (Status Register).
5. Set Register 0 such that the value is different from the value found in step 4.
6. Establish a link with the DUT.
7. Set bit 0.15 in Register 0 and disconnect the cable before the DUT restarts Auto-Negotiation.
8. Read Register 0 and Register 1.

Observable Results:

- a. In step 3, the DUT should stop Auto-Negotiation, wait `break_link_timer`, and then restart Auto-Negotiation by sending FLPs.
- b. In step 8, the value read from Register 0 should identically match the value read in step 4. In step 8, the value read from Register 1 should identically match the value read in step 4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #22.1.2: Auto-Negotiation Enable

Purpose: To verify that bit 0.12 controls the enabling/disabling of the Auto-Negotiation process.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 22.2.4.1.4, 28.3.1, Table 22-7, Table 28-8, Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Management has the ability to enable Auto-Negotiation by setting bit 0.12 to one and to disable Auto-Negotiation by setting bit 0.12 to zero. If the management has set bit 0.12 to zero, then the DUT should never source FLPs, and a link will be established using bits 0.13 and 0.6 (speed selection), and bit 0.8 (duplex mode) of the Control Register. When bit 0.12 is set to one, the DUT should transmit FLPs and establish a link using the Auto-Negotiation process.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination

Procedure:

1. Write a value of one to bit 0.12.
2. Observe transmissions from the DUT.
3. Repeat steps 1 and 2, writing a value of zero to bit 0.12.
4. Repeat steps 1 and 2, writing a value of one to bit 0.12.

Observable Results:

- a. The DUT should commence Auto-Negotiation and transmit FLPs after step 1.
- b. The DUT should cease Auto-Negotiation and proceed to transmit valid link signaling (based on bits 0.6 and 0.13) after step 3. The DUT may wait `break_link_timer` before sourcing valid link signaling.
- c. The DUT should cease idle transmission, wait `break_link_timer`, and then transmit FLPs after step 4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #22.1.3: Auto-Negotiation Restart

Purpose: To verify that bit 0.9 controls the restarting of Auto-Negotiation.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 22.2.4.1.7, 28.3.1, Table 22-7, Table 28-8, Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 22, 2004

Discussion: The MII Control Register provides a means for management to restart Auto-Negotiation by writing a value of one to bit 0.9 of the register. This is a way to restart Auto-Negotiation without resetting the entire PHY.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send a continuous stream of FLPs to the DUT encoded with 01E1h.
2. While the traffic generator is sending FLPs, write a value of one to bit 0.9
3. Observe transmissions from the DUT

Observable Results:

- a. The DUT should cease transmission, wait approximately `break_link_timer`, and then start to transmit FLPs

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #22.1.4: Auto-Negotiation Complete

Purpose: To verify that bit 1.5 is properly set upon completion of Auto-Negotiation and entrance into the FLP LINK GOOD state.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses, 22.2.4.2.10, 28.3.1, Table 22-8, Table 28-8, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Once a link has been established, management needs to be made aware that frame transmission and reception can commence. Bit 1.5 is set when Auto-Negotiation is complete and a link has come up.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Disable Auto-Negotiation by writing a value of zero to bit 0.12.
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state.
3. Observe the status of bit 1.5
4. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state followed by valid link signaling in order to establish a link
5. Observe the status of bit 1.5
6. Repeat steps 2-5 with Auto-Negotiation enabled.

Observable Results:

- a. When Auto-Negotiation is disabled, the value of bit 1.5 should never be set to one.
- b. When Auto-Negotiation is enabled, the DUT should not set bit 1.5 until it has entered the FLP LINK GOOD state. Thus, in step 2 bit 1.5 should be zero, and in step 4 bit 1.5 should be one.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #22.1.5: Link Status

Purpose: To verify that bit 1.2 of the Status Register is set when a valid link has been established and is not set if a valid link has not been established.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses, 22.2.4.2.13, 28.2.6.1.1, 28.3.1, Table 22-8, Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: April 23, 2003

Discussion: Management is made aware that a valid link has been established by bit 1.2 of the MII Status Register. When this bit is set, it means that the DUT has entered the FLP LINK GOOD state, regardless of whether or not Auto-Negotiation is enabled or disabled.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT a series of FLPs and link signaling such that a link will be established.
2. Monitor the status of bit 1.2.
3. Restart Auto-Negotiation.
4. Send link signaling such that a link will be established through parallel detection.
5. Monitor the status of bit 1.2.
6. Turn off Auto-Negotiation (if possible).
7. Send the DUT an idle pattern to manually force a link.
8. Monitor the status of bit 1.2.

Observable Results:

- a. The DUT should not set bit 1.2 until the FLP LINK GOOD state has been entered, regardless of whether or not Auto-Negotiation has been used to establish a link.

Possible Problems: If management access is not provided, then this test cannot be performed.

*The University of New Hampshire
InterOperability Laboratory*

Test #22.1.6: Auto-Negotiation Ability

Purpose: To verify that the DUT maintains the value of one in bit 1.3.

References:

[1] IEEE Std 802.3, 2005 Edition - subclause 22.2.4.2.12, Table 22-8, Table 28-8

Resource Requirements:

- None

Last Modification: February 5, 2003

Discussion: Management is made aware that an Auto-Negotiation capable PHY is attached via the Status Register bit 1.3 *Auto-Negotiation Ability*. Thus, management is made aware of the PHYs capability, regardless of the management's desire to enable or disable Auto-Negotiation. While this bit may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII to discover the Auto-Negotiation capability of an attached PHY.

Test Setup: Access the DUT's Management Registers.

Procedure:

1. Disable Auto-Negotiation (set bit 0.12 to zero).
2. Read the DUT's Status Register bit 1.3.
3. Enable Auto-Negotiation (set bit 0.12 to one).
4. Read the DUT's Status Register bit 1.3.

Observable Results:

- a. Bit 1.3 should be set, regardless of whether Auto-Negotiation is enabled or not.

Possible Problems: If management access is not provided, then this test cannot be performed.

*The University of New Hampshire
InterOperability Laboratory*

Test #22.1.7: Report PHY Capabilities

Purpose: To verify that the PHY set bits 1.15:8 and 15.15:12 appropriately for the PHY's capabilities.

References:

- [1] IEEE Std 802.3, 2002 Edition - subclauses 22.2.4.2.1, 22.2.4.2.2, 22.2.4.2.3, 22.2.4.2.4, 22.2.4.2.5, 22.2.4.2.6, 22.2.4.2.7, 22.2.4.2.16, 22.2.4.4.1, 22.2.4.4.2, 22.2.4.4.3, 22.2.4.4.4, Table 22-8, Table 22-11

Resource Requirements:

- None

Last Modification: July 22, 2004

Discussion: Management is made aware that a PHY's signaling capabilities via the Status Register bits 1.15:9. If bit 1.8 is set, then the PHY has additional capabilities specified in the Extended Status Register (Register 15) bits 15.15:12. Thus, management is made aware of the PHY's capability, regardless of the management's desire to enable or disable that technology. While these bits may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII/GMII to discover the Auto-Negotiation capability of an attached PHY. (Note: an exposed GMII is not specified by 802.3)

Status Register technology capability bit definitions

Bit(s)	Name	Description	R/W
1.15	100BASE-T4	1=PHY able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1=PHY able to perform 100BASE-X FD	RO
1.13	100BASE-X Half Duplex	1=PHY able to perform 100BASE-X HD	RO
1.12	10BASE-T Full Duplex	1=PHY able to perform 10BASE-T FD	RO
1.11	10BASE-T Half Duplex	1=PHY able to perform 10BASE-T HD	RO
1.10	100BASE-T2 Full Duplex	1=PHY able to perform 100BASE-T2 FD	RO
1.9	100BASE-T2 Half Duplex	1=PHY able to perform 100BASE-T2 HD	RO
1.8	Extended Status	1=Extended status info in Register 15	RO
15.15	1000BASE-X Full Duplex	1=PHY able to perform 1000BASE-X FD	RO
15.14	1000BASE-X Half Duplex	1=PHY able to perform 1000BASE-X HD	RO
15.13	1000BASE-T Full Duplex	1=PHY able to perform 1000BASE-T FD	RO
15.12	1000BASE-T Half Duplex	1=PHY able to perform 1000BASE-T HD	RO

Test Setup: Access the DUT's Management Registers.

Procedure:

1. Read bits 1.15:8 and 15.15:12.

Observable Results:

*The University of New Hampshire
InterOperability Laboratory*

- a. Bits 1.15:9 and 15.15:12 should be set appropriately. If the DUT is 1000BASE-T capable, bit 1.8 should be set to one and valid 1000BASE-T abilities should be contained in Register 15. If the DUT is not 1000BASE-T capable, bit 1.8 should be cleared to zero and the contents of Register 15 should be ignored.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #22.1.8 Duplex Mode

Purpose: To verify that the DUT will resolve a link to the highest common duplex mode according to bit 0.8.

References:

- IEEE Std 802.3, 2005 Edition - subclauses 22.2.4.1.3, Table 22-7

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 22, 2004

Discussion: When Auto-Negotiation has been disabled setting bit 0.8 in the Control Register configures the PHY for full duplex operation, and clearing bit 0.8 configures the PHY for half duplex operation. When Auto-Negotiation has been enabled, bit 0.8 can be read or written, but its state has no effect on the link configuration. If a PHY is able to operate in only one duplex mode, the value of bit 0.8 should correspond to the mode in which the PHY can operate, and any attempt to change the setting of bit 0.8 should be ignored.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

Part a: Single Duplex support

1. Write a value of one to bit 0.15 to reset Register 0 to its default value.
2. Access Register 0 and read the default value of bit 0.8.

Part b: Auto-Negotiation on

3. Enable Auto-Negotiation by setting bit 0.12.
4. Establish a link with the DUT by sending FLPs advertising full duplex only at one supported speed. (i.e. 10BASE-T full duplex or 100BASE-TX full duplex)
5. For speeds >100Mbps:
 - Observe frames less than 512-bytes in length transmitted by the DUT.For speeds ≤100Mbps:
 - When the DUT enters the FLP LINK GOOD CHECK state, the Traffic Generator should provide the appropriate link signaling to the DUT. Cause the DUT to transmit a frame and upon transmission, source a frame from the Traffic Generator. Observe the transmission from the DUT.
6. Read bit 0.8.

*The University of New Hampshire
InterOperability Laboratory*

7. Repeat steps 2-5 for all different speeds and duplexes the DUT supports.

Part c: Auto-Negotiation off

8. Disable Auto-Negotiation by clearing bit 0.12.
9. Set bit 0.8 and establish a full duplex link with the DUT by sending appropriate link signaling at one supported speed. (i.e. 10BASE-T full duplex or 100BASE-TX full duplex)
10. For speeds >100Mbps:
 - Observe frames less than 512-bytes in length transmitted by the DUT.For speeds <=100Mbps:
 - When the DUT enters the FLP LINK GOOD CHECK state, the Traffic Generator should provide the appropriate link signaling to the DUT. Cause the DUT to transmit a frame and upon transmission, source a frame from the Traffic Generator. Observe the transmission from the DUT.
11. Repeat steps 8-10 for all different speeds and duplexes the DUT supports.

Observable Results:

- a. If the PHY is able to operate in only one duplex mode, the value of bit 0.8 should correspond to the mode in which the PHY can operate.
- b. INFORMATIVE: The DUT may or may not write bit 0.8 to reflect link configuration.
- c. The DUT should resolve a full duplex link when bit 0.8 has been set, and resolve a half duplex link when bit 0.8 has been cleared.

Possible Problems: If management access is not provided, then this test cannot be performed. In part (a), if the PHY does not maintain a default value in Register 0, this test cannot be performed.

Test #22.1.9 Speed Selection

Purpose: To verify that bits 0.6 and 0.13 of the Control Register are set appropriately once a valid link has been established manually.

References:

- IEEE Std 802.3, 2005 Edition - subclause 22.2.4.1.3, Table 22-7

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 22, 2004

Discussion: Link speed can be selected via either the Auto-Negotiation process, or manual speed selection. When Auto-Negotiation is disabled, and bit 0.6 (Speed Selection MSB) is set to zero, setting bit 0.13 (Speed Selection LSB) to one should configure the PHY for 100 Mb/s operation, and clearing bit 0.13 should configure the PHY for 10 Mb/s operation. When Auto-Negotiation is disabled and bit 0.6 is set to one, clearing bit 0.13 to zero should enable 1000 Mb/s operation. When Auto-Negotiation is enabled, bits 0.6 and 0.13 can be read or written, however, writing to these bits should have no effect on the configuration, and these bits may not reflect the operating speed of the link when read. The default values of bits 0.6 and 0.13 are the encoding of the highest speed at which the PHY can operate according to 1.15:9 and 15.15:12.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

Part a: Default values:

1. Write a value of one to bit 0.15 to reset Register 0 to its default value.
2. Access Register 0 and read bits 0.6 and 0.13.

Part b: Auto-Negotiation off

3. Disable Auto-Negotiation by writing a value of zero to bit 0.12.
4. Write a value of zero to bits 0.6 and 0.13.
5. Observe transmissions from the DUT.
6. Repeat steps 3-4 writing a value of one to bit 0.13 and a value of zero to bit 0.6.
7. Repeat steps 3-4 writing a value of zero to bit 0.13 and a value of one to bit 0.6.
8. Repeat steps 3-4 writing a value of one to both bit 0.13 and bit 0.6.

*The University of New Hampshire
InterOperability Laboratory*

Part c: Auto-Negotiation on

9. Enable Auto-Negotiation by writing a value of one to 0.12.
10. Establish a valid 100BASE-TX link with the DUT.
11. Access register 0 and attempt to write a one to bit 0.6 and a zero to bit 0.13.
12. Repeat step 9, however, write a value of zero to bit 0.6 and a one to bit 0.13.

Part d:

13. Enable Auto-Negotiation by writing a value of one to bit 0.12.
14. Establish a valid 100BASE-TX link with the DUT via Auto-Negotiation.
15. Write a value of 00**b** (where **b** stands for *binary*) to bits 0.6 and 0.13.
16. Read the value of bits 0.6 and 0.13.
17. Write a value of 11**b** to bits 0.6 and 0.13.
18. Read the value of bits 0.6 and 0.13.

Observable Results:

- a. The default value of bits 0.6 and 0.13 should reflect the highest speed capable of the PHY.
- b. After step 2, the DUT should transmit appropriate link signaling corresponding to bits 0.6 and 0.13.
- c. The writing of bits 0.6 and 0.13 should not have any effect on the link configuration.
- d. **INFORMATIVE:** When Auto-Negotiation is enabled, the DUT may or may not indicate the operating speed of the link through bits 0.6 and 0.13.

Possible Problems: If management access is not provided, then this test cannot be performed. In part (a), if the PHY does not maintain a default value in Register 0, this test cannot be performed.

GROUP 2: CLAUSE 28 MANAGEMENT REGISTERS

Scope: The following tests cover Auto-Negotiation operation specific to the management register set.

Overview: These tests are designed to verify that the device under test properly implements the Media Independent Interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 28 (Auto-Negotiation) of IEEE 802.3. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS ARE PERFORMED BY BOTH FAST ETHERNET AND GIGABIT ETHERNET CONSORTIUMS. THESE TESTS CANNOT BE PERFORMED IF REGISTER ACCESS IS NOT PROVIDED.

Test #28.2.1: AN Advertisement Register

Purpose: To verify that the Auto-Negotiation Advertisement Register (Register 4) is reflected in the Link Code Words transmitted by the DUT.

References:

- [1] IEEE Std 802.3, 2005 Edition – subclauses 28.2.4.1.3, 40.5.1.1, Annex 28A, Annex 28B, Annex 28D, Table 28-2, Table 40-3

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.

Last Modification: November 3, 2004

Discussion: For a device to advertise abilities that it possesses, it must be able to configure the abilities advertised during the Auto-Negotiation process so that they match the device's true capabilities. Register 4 of the MII is defined to contain these abilities, however, if the device does not use a MII then the logical equivalent must be provided. If the DUT implements Annex 40C, the Next Page bit within the base page may be set by the 1000BASE-T add-on as displayed in figure 40C-1. Therefore, bit 4.15 may not directly map to the DUT's transmitted Link Code Word.

AN Register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as 0	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Via management, access Register 4 and write the value FFFFh.
2. Access and read Register 4.
3. Observe transmission from the DUT.
4. Repeat steps 1-3 with other test values including (but not limited to) 0000h.

Observable Results:

*The University of New Hampshire
InterOperability Laboratory*

- a. Register 4 and the Link Code Words transmitted by the DUT should contain the bit values of 4.15, and 4.13-4.0 that was written to Register 4 after a restart in Auto-Negotiation. See comments below.
- b. Register 4 and the Link Code Words transmitted by the DUT should contain the bit value of zero for 4.14.

The following scenarios will result in a “Refer to Comments”:

- Bit 4.12 cannot be written. This bit is currently reserved for future use and it is advisable for this bit to be R/O.
- Bits 4.9:5 cannot be written. If the physical device does not support any of these abilities, then writing to these bits in the Advertisement Register is insignificant.
- Bits 4.4:0 cannot be written, however, the DUT must be able to advertise support for IEEE 802.3 Ethernet.

The following scenarios will result in a “Pass with Comments”:

- Bit 4.15 cannot be written. It is proper for bit 4.15 to be unset if bit 6.2 (Next Page Able) in the Expansion Register is set to zero indicating that the local device does not support Next Page exchange functionality.

The following scenarios will result in a “FAIL”:

- If the following bits cannot be written: bits 4.11:10.
- Bits 4.9:5 cannot be written. If this physical device supports any of these abilities then these bits must be R/W.
- If the transmitted Link Code Word does not exact reflect the value contained within Register 4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.2.2: AN Link Partner Ability Register

Purpose: To verify that the Auto-Negotiation Link Partner Ability Register is set according to Table 28-8 based upon the reception of Link Code Words by the DUT.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 28.2.4.1.4, 28.2.1.3, Annex 28A, Annex 28B, Annex 28D, Table 28-3

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: November 3, 2004

Discussion: For a device to resolve a proper link configuration, it must accurately receive its partner's abilities and relate them to management. Register 5 of the MII is defined to contain these abilities; if the DUT does not use a MII then the logical equivalent must be provided. After Parallel Detection is completed Register 5 should reflect the current link configuration.

Link Partner Ability Register bit definitions

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT enough Link Code Words to put the DUT into the COMPLETE ACKNOWLEDGE state.
2. Access and read Register 5.
3. Repeat steps 1-2 by sending values including (but not limited to) FFFFh, 0000h along with the same page with ACK in order to put the DUT into the COMPLETE ACKNOWLEDGE state.
4. Attempt to write FFFFh to Register 5, and then read the contents of Register 5.
5. Send 10BASE-T link signaling such that a link will be established through parallel detection.

*The University of New Hampshire
InterOperability Laboratory*

6. Access and read Register 5.
7. Repeat steps 5 and 6 with 100BASE-TX and 100BASE-T4 link signaling.

Observable Results:

- a. The bits of the Link Code Word received by the DUT should be contained in Register 5 exactly as they were received once the DUT has entered the COMPLETE ACKNOWLEDGE state.
- b. The DUT should not allow any of the bits of Register 5 to be written.
- c. After parallel detection, Register 5 should reflect the current link configuration of the DUT.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.2.3: Remote Fault

Purpose: To verify that the DUT sets bit 1.4 upon reception of a Link Code Word with the Remote Fault bit set.

References:

[1] IEEE Std 802.3, 2005 Edition - subclauses 22.2.4.2, 22.2.4.2.11, 28.2.3.5, Table 22-8

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 22, 2004

Discussion: A device that supports the Remote Fault function must indicate the reception of a Base Page with the Remote Fault bit set by setting bit 1.4 in the MII Status Register. In this way, management is made aware of a remote fault indication from the link partner. After management reads the Status Register, bit 1.4 should reset to zero. If the DUT does not support the Remote Fault function, no action is necessary.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Read the MII Status Register (Register 1) twice.
2. Use the Traffic Generator to send enough FLPs with the RF bit set to put the DUT through the COMPLETE ACKNOWLEDGE state.
3. Wait until DUT restarts Auto-Negotiation.
4. Read Register 1.
5. Read Register 1 again.
6. Establish a link with the DUT with the RF bit in the Link Partner's base page set to one.
7. Read Register 1 while the link is up.
8. Read Register 1 again.

Observable Results:

- a. In step 1, bit 1.4 should be cleared to zero.
- b. In steps 4, bit 1.4 should be set to one. In step 5, bit 1.4 should be cleared to zero.
- c. In step 7, bit 1.4 should be set to one. In steps 8, bit 1.4 should be cleared to zero.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support the Remote Fault function this test cannot be performed.

Test #28.2.4: Parallel Detection Fault

Purpose: To verify that the DUT sets bit 6.4 upon reception of a parallel detection fault.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 28.2.4.1.5, 28.3.1, Table 28-5, Table 28-8, Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: February 5, 2003

Discussion: Management is made aware that a parallel detection fault has occurred by reading bit 6.4 of the Auto-Negotiation Expansion Register (MII Register 6). Upon receiving such a fault, the DUT must set this bit. A value of 1 means that a fault has been detected via the Parallel Detection function, while a value of 0 indicates that a fault has not been detected via the Parallel Detection function. A parallel detection fault occurs if zero or more than one PMA is indicated to have link_status=READY when the autoneg_wait_timer expires during the parallel detection process. The Parallel Detection Fault bit should be reset upon a read to the Auto-Negotiation Expansion Register.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part a – for devices with a 100BASE-TX PMA

1. Send the DUT valid 100BASE-TX link signaling for <500ms such that the DUT stops sending FLPs.
2. Read the Auto-Negotiation Expansion Register (Register 6) twice.

Part b - for devices with a 100BASE-T4 PMA

3. Send the DUT valid 100BASE-T4 link signaling <500 ms such that the DUT stops sending FLPs.
4. Repeat step 2.

Part c - for devices with a 10BASE-T PMA

5. Send the DUT valid NLPs for <500 ms such that the DUT stops sending FLPs.
6. Repeat step 2.

Observable Results:

*The University of New Hampshire
InterOperability Laboratory*

- a-c. Bit 6.4 should be set to one the first time the Auto-Negotiation Expansion Register is read, and set to zero the second time the register is read.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support 10BASE-T, 100BASE-TX or 100BASE-T4 then this test cannot be performed.

Test #28.2.5: Page Received Setting/Resetting

Purpose: To verify that `mr_page_rx` is set when a new page is received and cleared when the Auto-Negotiation Expansion Register is read.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 28.2.4.1.5, 28.3.1, Table 28-5, Table 28-8, Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: June 9, 2005

Discussion: Management is made aware of the reception of a new page by reading bit 6.1 in the Auto-Negotiation Expansion Register. If bit 6.1 is set, then management can look at the contents of the received page and act accordingly. Upon reading of this register, this bit is cleared so that management may not read the register again and think that the same page is a new page.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT a constant stream of FLPs encoded with 81E1h.
2. Read bit 6.1 twice.
3. Repeat steps 1-3 with an encoding of C1E1h.
4. If the DUT supports Next Page Exchange, restart Auto-Negotiation and send enough FLPs encoded with C1E1h to enter COMPLETE ACKNOWLEDGE followed by a constant stream of FLPs encoded with E808h to again cause the DUT to enter COMPLETE ACKNOWLEDGE.
5. Read bit 6.1 (should be one).
6. Write the desired Next Page value to Register 7.
7. Read bit 6.1 (should be one).
8. Read bit 6.1 (should be zero).

Observable Results:

- a. After step 1, bit 6.1 should be zero for both reads.
- b. After step 3, bit 6.1 should be one for the first read and zero for the second read.
- c. After step 4, bit 6.1 should be one for the first two reads and zero for the third read.

*The University of New Hampshire
InterOperability Laboratory*

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support a Next Page Exchange, part (c) cannot be performed.

Test #28.2.6: Link Partner Auto-Negotiation Able

Purpose: To verify that the DUT sets bit 6.0 upon detection of link partner which is capable of Auto-Negotiation.

References:

- [1] IEEE Std 802.3, 2005 Edition – subclauses 28.2.4.1.5, 28.3.1, Table 28-5, Table 28-8, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 22, 2004

Discussion: A device's management is made aware that the Link Partner is capable of Auto-Negotiation when the DUT enters the ACKNOWLEDGE DETECT state and sets `mr_lp_autoneg_able` to true. This in-turn sets bit 6.0 in the Expansion Register to 1. Whenever the DUT re-enters the ABILITY DETECT state, `mr_lp_autoneg_able` should be reset to false (6.0 set to 0).

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Read bit 0 of the Expansion Register (Register 6).
2. Use the Traffic Generator to send a constant stream of identical FLPs without ACK set to put the DUT in the ACKNOWLEDGE DETECT state.
3. Read bit 0 of the Register 6.
4. Send nothing to the DUT and wait until the DUT re-enters the ABILITY DETECT state.
5. Read bit 0 of the Register 6.
6. Use the Traffic Generator to send a constant stream of FLPs alternating in content and without ACK set, to keep the DUT in the ABILITY DETECT state.
7. Read bit 0 of the Register 6.

Observable Results:

- a. In steps 1, 5 and 7 bit 6.0 should be set to zero. In step 3, bit 6.0 should be set to one.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.2.7: AN Next Page Transmit Register

Purpose: To verify that the Auto-Negotiation Next Page Transmit Register, set according to Table 28-6, is properly reflected in the Next Pages transmitted by the DUT.

References:

[1] IEEE Std 802.3, 2005 Edition - subclauses 28.2.3.4, 28.4.1.6, Table 28-6

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: June 6, 2005

Discussion: During a Next Page exchange, management must have the ability to control the contents of the pages to be transmitted. The AN Next Page Transmit Register (MII Register 7) is used to specify these abilities, however, if the device does not use a MII then the logical equivalent must be provided. The definition of Register 7 is provided below for convenience.

Next Page Transmit Register bit definitions

Bit(s)	Name	Description	R/W
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code Field	See 28.2.3.4	R/W

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Set the NP bit in the DUT's Base Page (bit 4.15).
2. Send a constant stream of FLPs to the DUT containing the abilities C1E1h.
3. Via management, read the Next Page Transmit Register (Register 7) and write a value of FFFFh.
4. Observe transmission from the DUT.
5. Write a value of one to bit 0.9 to restart Auto-Negotiation.
6. Repeat steps 2 through 4 using values including (but not limited to) 0000h.

*The University of New Hampshire
InterOperability Laboratory*

Observable Results:

- a. The Next Pages transmitted by the DUT should have bits 7.15, 7.13, 7.12, and 7.10:0 set corresponding to the value written to Register 7.
- b. The Next Pages transmitted by the DUT should have bit 7.14 set to zero, and bit 7.11 set to the opposite of the value of bit 4.11 in the initial Link Code Word sent by the DUT.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.2.8: AN Link Partner Next Page Ability Register and Next Page Location Bits

Purpose: To verify that the Auto-Negotiation Link Partner Received Next Page Register is set according to Table 28-7 based upon the reception of Next Pages by the DUT, and to verify that the DUT properly stores received Next Pages in the correct register based on bits 6.6:5.

References:

- [1] IEEE Std 802.3aj, 2005 Edition - subclauses 28.2.3.4, 28.2.4.1.7, 28.2.4.1.4, 28.2.4.1.5, Tables 28-5, 28-7

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 20, 2006

Discussion: A DUT should store received Next Pages based on bits 6.6 and 6.5. If bit 6.6 is set to zero, the location of received Next Pages may be stored in Register 5 or Register 8. If bit 6.6 is set, then received Next Pages must be stored in Register 5 if bit 6.5 is set to zero, or Register 8 if bit 6.5 is set to one. For a device to resolve a proper link configuration, it must accurately receive its partner's Next Page abilities and relate them to management. The AN Link Partner Ability Next Page Register of the GMII is defined to contain these abilities, however, if the DUT does not use a GMII then the logical equivalent must be provided. The definition of Register 8 is provided below for convenience.

Auto-Negotiation Link Partner Next Page Ability Register bit definitions

Bit(s)	Name	Description	R/W
8.15	Next Page	See 28.2.3.4	RO
8.14	Reserved	See 28.2.3.4	RO
8.13	Message Page	See 28.2.3.4	RO
8.12	Acknowledge 2	See 28.2.3.4	RO
8.11	Toggle	See 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

Receive Next Page Location bit definitions

Bit(s)	Name	Description	R/W
6.6	Receive Next Page Location Able	See 28.2.4.1.5 in 802.3aj	RO
6.5	Receive Next Page Storage Location	See 28.2.4.1.5 in 802.3aj	RO

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

*The University of New Hampshire
InterOperability Laboratory*

Procedure:

1. Read bits 6.6:5 of the Expansion Register (Register 6).
2. Write to bits 6.6:5 such that the value differs from what was read in step 1. Then read Register 6.
3. Set the NP bit in the DUT's Base Page (bit 4.15).
4. Send the DUT enough FLPs with the Next Page bit set so that the DUT enters the COMPLETE ACKNOWLEDGE state, followed by a constant stream of FLPs encoded with 6008h.
5. It may be necessary to write any value (typically 2001) to Register 7 to cause the DUT to enter the NEXT PAGE WAIT state and thus eventually return to the COMPLETE ACKNOWLEDGE state.
6. Via management, access and read the Link Partner Received Next Page Register (Register 5 or 8 based on bits 6.6:5).
7. Repeat steps 2 through 4 using Next Pages including (but not limited to) 2808h, FFFFh and 0000h. If the toggle bit (D11) is set to a value of zero in the Next Pages (as in a Next Page value of 0000h), it should be set to a value of one in the Base Pages.
8. Write the value FFFFh to the Auto-Negotiation Link Partner Received Next Page Register. Then read the Auto-Negotiation Link Partner Received Next Page Register.

Observable Results:

- a. A write to bits 6.6:5 should not affect their contents.
- b. The DUT should store the received Next Pages in the appropriate register according to bits 6.6:5.
- c. The bits of the Next Pages received by the DUT should be contained in Register 5 or Register 8 exactly as they were received.
- d. A write to the Auto-Negotiation Link Partner Received Next Page Register should not affect its contents.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.2.9: mr_next_page_loaded

Purpose: To verify that mr_next_page_loaded is set upon write to the Auto-Negotiation Next Page Transmit Register, and cleared in the states NEXT PAGE WAIT and TRANSMIT DISABLE.

References:

[1] IEEE Std 802.3, 2005 Edition - subclauses 28.2.4.1.8, 28.3.1, Table 28-8, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: June 16, 2006

Discussion: The mr_next_page_loaded variable is a key parameter in the transition from states COMPLETE ACKNOWLEDGE to NEXT PAGE WAIT. It prevents the Auto-Negotiation protocol from proceeding until management has had time to load the AN Next Page Transmit Register with the next page to be transmitted. This occurs after the management has had time to read the previous Next Page received from its link partner (in the AN Link Partner Ability Next Page Register). The variable mr_next_page_loaded is automatically set when management writes the AN Next Page Transmit Register, but should be cleared in the TRANSMIT DISABLE or NEXT PAGE WAIT states. This test observes that the value of mr_next_page_loaded is being set and reset appropriately, and that the DUT behaves properly according to the value of this bit.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A: Resetting in the TRANSMIT DISABLE state:

1. Enable Next Page advertisement (write a logic one to bit 4.15).
2. Restart Auto-Negotiation (write a logic one to bit 0.9).
3. Write '2201h' to the Next Page Transmit Register (Register 7).
4. Restart Auto-Negotiation.
5. Use the Traffic Generator to send a constant stream of FLPs encoded with 'C1E1h' to cause the DUT to enter the COMPLETE ACKNOWLEDGE state.
6. Observe transmissions from the DUT.

Part B: Setting mr_next_page_loaded:

7. Write '2301h' to the Next Page Transmit Register.
8. Observe transmissions from the DUT.

Part C: Resetting in the NEXT PAGE WAIT state:

9. Use the Traffic Generator to send a constant stream of FLPs encoded with 'E808'.

*The University of New Hampshire
InterOperability Laboratory*

10. Observe transmissions from the DUT.

Part D: Resetting while remaining in the NEXT PAGE WAIT STATE:

11. Write '2401h' to the Next Page Transmit Register.

12. Observe transmissions from the DUT.

13. Write '2501h' to the Next Page Transmit Register.

14. Observe transmissions from the DUT.

Observable Results:

- a. Resetting in TRANSMIT DISABLE state: In step 6, the DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its Base Page with the Acknowledge bit set.
- b. In step 8, the DUT should commence transmissions of its first Next Page, with the proper Toggle and Acknowledge bit values.
- c. In step 10, the DUT should remain the COMPLETE ACKNOWLEDGE state and continue to send its first Next Page with the Acknowledge bit set.
- d. In steps 12 and 14, the DUT should remain in the NEXT PAGE WAIT state and continue to send its second Next Page (2401h).

Possible Problems: If the DUT does not support Next Page exchange, then this test cannot be performed. If management access is not provided, then this test cannot be performed.

*The University of New Hampshire
InterOperability Laboratory*

Test #28.2.10: Next Page Able

Purpose: To verify that the DUT sets bit 6.2 if it is capable of a Next Page exchange.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 28.2.4.1.5, 28.2.4.1.8, 28.3.1, Table 28-5, Table 28-8, Figure 28.16

Resource Requirements:

- None

Last Modification: July 22, 2004

Discussion: A PHY which supports Next Page exchange must indicate this capability to management by setting bit 6.2 in the Expansion Register (MII Register 6), regardless of whether a Next Page exchange is desired. While this bit may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII to discover any Next Page exchange capability of an attached PHY.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Disable Next Page Advertisement (clear bit 4.15 to zero).
2. Read bit 6.2 of the Expansion Register (Register 6).
3. Enable Next Page Advertisement (set bit 4.15 to one).
4. Read bit 6.2 of Register 6.

Observable Results:

- a. Bit 6.2 must be set if the DUT supports a Next Page exchange, regardless of whether a Next Page exchange is currently desired.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.2.11: Link Partner Next Page Able

Purpose: To verify that the DUT sets bit 6.3 upon reception of a Base Page which has bit 15 set.

References:

- [1] IEEE Std 802.3, 2005 Edition - subclauses 28.2.4.1.5, 28.2.4.1.8, 28.3.1, Table 28-5, Table 28-8, Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: June 9, 2005

Discussion: A device's management is made aware that the Link Partner is capable of a Next Page exchange, and also desires a Next Page exchange when the DUT enters the COMPLETE ACKNOWLEDGE state. Upon entrance, the DUT sets `mr_lp_np_able` to true, this in-turn sets bit 6.3 in the Expansion Register to 1. Whenever the DUT re-enters the ABILITY DETECT state, `mr_lp_np_able` should be reset to false (6.3 set to 0).

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Disable Next Page Advertisement (set bit 4.15 to zero).
2. Read bit 6.3 of the Expansion Register (Register 6).
3. Use the Traffic Generator to send a constant stream of identical FLPs with ACK set and NP not set to put the DUT in the COMPLETE ACKNOWLEDGE state.
4. Read bit 6.3 of Register 6.
5. Cease transmission of FLPs and allow the DUT to restart Auto-Negotiation (bit 4.15 should still be set to zero).
6. Use the Traffic Generator to send a constant stream of identical FLPs with ACK and NP set to put the DUT in the COMPLETE ACKNOWLEDGE state.
7. Read bit 6.3 of Register 6.
8. Repeat step 6 after enabling Next Page Advertisement (set bit 4.15 to one) and restarting Auto-Negotiation (set bit 0.9 to one).
9. Read bit 6.3 of Register 6.
10. Restart the Auto-Negotiation process (write a value of one to bit 0.9) and read bit 6.3 of Register 6.

Observable Results:

*The University of New Hampshire
InterOperability Laboratory*

- a. Bit 6.3 should not be set in steps 2 and 4.
- b. Bit 6.3 should be set to one after steps 7 and 9, and reset to zero after step 10.

Possible Problems: If management access is not provided, then this test cannot be performed.

GROUP 3: CLAUSE 40 MANAGEMENT REGISTERS

Scope: The following tests cover Auto-Negotiation operation specific to the management register set.

Overview: These tests are designed to verify that the device under test properly implements the Media Independent Interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 40 (1000BASE-T) of IEEE 802.3. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS ARE PERFORMED BY THE GIGABIT ETHERNET CONSORTIUM ONLY. THESE TESTS CANNOT BE PERFORMED IF REGISTER ACCESS IS NOT PROVIDED.

Test #40.3.1: 1000BASE-T MASTER/SLAVE Control Register bits 9.10:8

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Control Register bits 9.10:8 properly control the advertised Port type and duplex.

References:

[1] IEEE Std 802.3, 2005 Edition - subclause 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: June 9, 2005

Discussion: In order for 1000BASE-T devices to automatically configure themselves, they must complete the exchange of a Base Page and three Next Pages during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MII Register 4 (Base Page Advertised Ability Register) as well as MII Register 7 (Next Page Transmit Register). However, such an approach would require each systems management to be capable of properly following Clause 28's Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 1000BASE-T PHYs also incorporate the option of having an automatic embedded Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 1000BASE-T port. The system accomplishes this by writing to the MASTER/SLAVE Control Register (GMII Register 9). To specify what type of device the system is (multiport or single port) as well as the desired duplex mode for the port, the system simply writes to bits 9:10-8 (see table below). Once set, the system can enable the port, reset the port, or restart Auto-Negotiation and the embedded Next Page exchange controller will do the rest of the page exchange work. Recall that these bits are only meaningful if an embedded controller is in use. If one is not present, or disabled, then the system's management entity is required to properly complete the Next Page exchange via the properly timed writing of Register 7. In such an event, it is recommended that the contents of Register 9 accurately reflect the abilities advertised in the second Next Page of the 1000BASE-T exchange.

1000BASE-T MASTER/SLAVE Control Register bit definitions for ability advertisement

Bit(s)	Name	Description	Type
9.10	Port type	1=Multiport device 0=single - port device	R/W
9.9	1000BASE-T Full Duplex	1=Advertise PHY is 1000BASE-T full duplex capable 0=Advertise PHY is not 1000BASE-T full duplex capable	R/W
9.8	1000BASE-T Half Duplex	1=Advertise PHY is 1000BASE-T half duplex capable 0=Advertise PHY is not 1000BASE-T half duplex capable	R/W

*The University of New Hampshire
InterOperability Laboratory*

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Via management access, write to GMII Register 9 bits 10-8 (or equivalent) the value '111***b***' (where *b* stands for *binary*).
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state, followed by enough Null Message Pages (with proper Toggle bit values) to allow the DUT to transmit all of its Next Pages
3. Monitor the Next Pages transmitted by the DUT.
4. Repeat steps 1 through 3 changing the value written until all values have been tested.

Observable Results:

- a. Bits U2 - U4 in the second Next Page (third overall page) transmitted by the DUT should match the value written in Step 1, without exception.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed.

Test #40.3.2: 1000BASE-T MASTER/SLAVE Control Register bits 9.12:11

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Control Register bits 9.12:11 properly control MASTER-SLAVE Manual Configuration.

References:

[1] IEEE Std 802.3, 2005 Edition: subclause 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: June 9, 2005

Discussion: In order for 1000BASE-T devices to automatically configure themselves, they must complete the exchange of a Base page and three Next Pages during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MII Register 4 (Base Page Advertised Ability Register) as well as MII Register 7 (Next Page Transmit Register). However, such an approach would require each system's management to be capable of properly following Clause 28's Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 1000BASE-T PHYs also incorporate the option of having an automatic embedded Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 1000BASE-T port. The system accomplishes this by writing to the MASTER/SLAVE Control Register (GMII Register 9). To specify that the port should be forced to be either MASTER or SLAVE, the system must set bit 9.12 to 1, and set 9.11 to either 1 or 0 (see table below). Once set, the system can enable the port, reset the port, or restart Auto-Negotiation and the embedded Next Page exchange controller will do the rest of the page exchange work. Recall that these bits are only meaningful if an embedded controller is in use. If one is not present, or disabled, then the system's management entity is required to properly complete the Next Page exchange via the properly timed writing of Register 7. In such an event, it is recommended that the contents of Register 9 accurately reflect the abilities advertised in the second Next Page of the 1000BASE-T exchange.

**1000BASE-T MASTER/SLAVE Control register bit definitions for
MASTER-SLAVE Manual Configuration**

Bit(s)	Name	Description	Type
9.12	MASTER-SLAVE Manual Config Enable	1=Enable MASTER-SLAVE Manual Configuration 0=Disable MASTER-SLAVE Manual Configuration	R/W
9.11	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0= Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one.	R/W

*The University of New Hampshire
InterOperability Laboratory*

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Via management access, write to GMII Register 9 bits 12-11 (or equivalent) the value '11*b*' (where *b* stands for *binary*)
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state, followed by enough Null Message Pages (with proper Toggle bit values) to allow the DUT to transmit all of its Next Pages
3. Monitor the Next Pages transmitted by the DUT.
4. Repeat steps 1 through 3 changing the value written to '00*b*', and '10*b*'.
5. Repeat steps 1 through 3 changing the value written to '01*b*'.

Observable Results:

- a. Bits U0 & U1 in the second Next Page (third overall page) transmitted by the DUT should match the value written in step 1, except for the value written in step 5.
- b. In step 5, the DUT may either set U0 to 0, and U1 to 1 (which should be ignored since U0=0) or the DUT may set both U0 and U1 to 0.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed.

*The University of New Hampshire
InterOperability Laboratory*

Test #40.3.3: 1000BASE-T MASTER/SLAVE Status Register

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Status Register conforms to the definition in Table 40-3.

References:

[1] IEEE Std 802.3, 2005 Edition - subclause 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- 1000BASE-T Traffic Generator: A system capable of properly completing the 1000BASE-T Next Page exchange and establishing a valid 1000BASE-T link.

Last Modification: January 13, 2000

Discussion: Once a 1000BASE-T device completes Auto-Negotiation, status information specific to the 1000BASE-T link must be properly represented in the MASTER-SLAVE Status Register (GMII Register 10).

1000BASE-T MASTER/SLAVE Status Register bit definitions

Bit(s)	Name	Description	Type
10.15	MASTER-SLAVE configuration fault	1=MASTER-SLAVE configuration fault detected 0=No MASTER-SLAVE configuration fault detected	RO/LH/ SC
10.14	MASTER-SLAVE configuration resolution	1=Local PHY configuration resolved to MASTER 0=Local PHY configuration resolved to SLAVE	RO
10.13	Local Receiver Status	1=Local Receiver OK (loc_rcvr_status=OK) 0= Local Receiver not OK (loc_rcvr_status=NOT_OK)	RO
10.12	Remote Receiver Status	1=Remote Receiver OK (rem_rcvr_status=OK) 0= Remote Receiver not OK (rem_rcvr_status=NOT_OK)	RO
10.11	LP 1000T FD	1=Link Partner is capable of 1000BASE-T full duplex 0=Link Partner is not capable of 1000BASE-T full duplex	RO
10.10	LP 1000T HD	1=Link Partner is capable of 1000BASE-T half duplex 0=Link Partner is not capable of 1000BASE-T half duplex	RO
10.9:8	Reserved	Reserved	RO
10.7:0	Idle Error Count	Count of each occurrence of rxerror_status=ERROR. Cleared on read. Held at all ones in case of overflow	RO/SC

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Read GMII Register 10 (or equivalent) twice.
2. Via management access, write to GMII Register 10 (or equivalent) the value 'FFFFh'.
3. Read GMII Register 10 (or equivalent).

*The University of New Hampshire
InterOperability Laboratory*

4. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T Next Page exchange with the DUT and establish a link. Advertise 1000BASE-T full duplex and Half Duplex capability.
5. Read Register 10 bits 10.11 and 10.10. Repeat 4 and 5 until all four bit combinations are tested.
6. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T Next Page exchange with the DUT and establish a link, such that the DUT should be MASTER. If necessary, use the line monitor to verify that the DUT should resolve to MASTER.
7. Read Register 10 bit 14.
8. Repeat step 6 and 7, changing the Next Page exchange such that the DUT should be SLAVE.
9. Configure the DUT to be manual_MASTER. Use the 1000BASE-T Traffic Generator to produce a proper 1000BASE-T Next Page exchange with the DUT, advertising that the Traffic Generator is a manual_MASTER. This should cause the DUT to detect a configuration fault.
10. Read Register 10 bit 15, then read register 10 again.
11. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T Next Page exchange with the DUT and establish a link.
12. Read Register 10 bits 10.13 and 10.12
13. With the 1000BASE-T link still established, attempt to degrade the quality of the link between the two devices by any means, but do not break the link. Either by a controlled noise injection, or an uncontrolled noise injection (such as by very briefly loosening the RJ-45 plug & jack connection.)
14. Read Register 10 bits 7:0, if non-zero, read again. Repeat 13 and 14 until a non-zero value is read.

Observable Results:

- a. The value read step 3 should be identical to the final value read in step 1.
- b. In step 5, the reported link partner duplex capability should match the capability indicated in the received UP1 Next Page.
- c. In step 7, bit 14 should be set to one, in step 8, bit 15 should be set to 0.
- d. In step 10, bit 15 should initially be set. After the second read, the bit should be cleared.
- e. In step 12, bits 13 and 12 should both be set once the link is established.
- f. In step 14, on the first read, following the event of errors, the counter should indicate the number of errors (MSB is bit 7). Following the second read the value should be zero.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed. In step 13 and 14, the ability to induce errors in either a controlled or uncontrolled manner without causing a link failure may not be possible for a given device.