# 40 AND 100 GIGABIT ETHERNET CONSORTIUM

**Clause 86A nPPI**
**40GBASE-SR4, 40GBASE-LR4**
**& 100GBASE-SR10 Module PMD Test Suite**
***Version 1.0***
*Technical Document*


*Last Updated: April 7, 2014*

***40 and 100 Gigabit Ethernet Consortium***
***University of New Hampshire***
***InterOperability Laboratory***

***121 Technology Drive, Suite 2***
***Durham, NH 03824***
***Phone: (603) 862-0090***
***Fax: (603) 862-4181***
*https://www.iol.unh.edu/services/testing/40and100gec/*

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*The University of New Hampshire*
*InterOperability Laboratory*

# MODIFICATION RECORD

April 7, 2014 Version 1.0

Michael Klempa: Initial draft.

# ACKNOWLEDGMENTS

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| | |
|---|---|
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| Curtis Donahue | UNH InterOperability Laboratory |

# INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the functionality of the Physical Medium Dependent (PMD) sublayer of their products.

These tests are designed to determine if a product conforms to specifications defined in Clause 86A of the IEEE 802.3-2012 Standard. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

**Purpose**

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

**References**

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

**Resource Requirements**

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

**Last Modification**

This specifies the date of the last modification to this test.

**Discussion**

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

**Test Setup**

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

**Test Procedure**

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

**Observable Results**

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

**Possible Problems**

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

# GROUP 1: TX ELECTRICAL SIGNALING REQUIREMENTS

**Overview:**

The tests defined in this section verify the transmitter electrical signaling characteristics of the Physical Medium Dependent (PMD) layer defined in Clause 86A of IEEE 802.3-2012.

**Test 86A.1.1 – Signaling Speed**

**Purpose:** To verify that the baud rate of the DUT is within the conformance limits.

**References:**

[1] IEEE Std. 802.3-2012, Table 86-2 – Summary of 40GBASE-SR4 and 100GBASE-SR10

**Resource Requirements:** See Appendix I

**Last Modification:** July 1, 2013

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the signaling speed, which is 10.3125 Gbaud +/- 100 ppm per lane. This translates to 10.3125 Gbaud +/- 1.03125 Mbaud, with a nominal Unit Interval (UI) of 96.96 ps.

The signal being transmitted by the DUT may be any valid 40GBASE-SR4 or 100GBASE-SR10 signal.

**Test Setup:** See Appendix I

**Test Procedure:**

1. Configure the DUT to send a valid signal or test pattern.
2. Connect the DUT's transmitter to the DSO.
3. Measure the average TX signaling speed.

**Observable Results:**

a. The signaling speed shall be within 10.3125 Gbaud +/- 1.03125 Mbaud

**Possible Problems:** None.

**Test 86A.1.2 – Single Ended Output Voltage**

**Purpose:** To verify that the single ended common output voltage of the DUT is within the conformance limits

**References:**

[1] IEEE Std. 802.3-2012, Table 86A-3 – Module electrical output specifications
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.1 – Output amplitude
[3] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

**Resource Requirements:** See Appendix I

**Last Modification:** April 7, 2014

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR4 devices. This specification includes conformance requirements for the single ended output voltage defined in [2].

In this test, the single-ended output voltage is measured at the Transmit Compliance Point of the DUT. The signal being transmitted by the DUT may be any valid 40GBASE-SR4 or 100GBASE-SR4 signal, however the test pattern 4 (PRBS9) defined in [3] will be used, primarily out of convenience, as this pattern is also used for several other tests in this group.

**Test Setup:** See Appendix I

**Test Procedure:**

1. Configure the DUT to send test pattern 4 (PRBS9).
2. Connect the DUT's transmitter to the DSO.
3. Measure the single-ended output voltage of SLi<p> or SLi<n> at the test point.

**Observable Results:**

a. The single ended output voltage shall be between -0.3 V and 4 V with respect to the signal shield.

**Possible Problems:** None

**Test 86A.1.3 – AC Common Mode Output Voltage**

**Purpose:** To verify that the AC common mode output voltage of the DUT is within the conformance limits

**References:**

[1] IEEE Std. 802.3-2012, Table 86A-3 – Module electrical output specifications
[2] IEEE Std. 802.3-2012, subclause 86A.5.3.1 – AC common-mode voltage
[3] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

**Resource Requirements:** See Appendix I

**Last Modification:** April 7, 2014

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR4 devices. This specification includes conformance requirements for maximum out AC common-mode voltage defined in [2].

In this test, the differential amplitude is measured while the DUT is connected to the DSO. The common mode voltage can be found by averaging the signal+ and signal- at any time. RMS AC common-mode voltage may be calculated by applying the histogram function over 1 UI to the common mode signal.

**Test Setup:** See Appendix I

**Test Procedure:**

1. Configure the DUT to send test pattern 3 (PRBS31).
2. Connect the DUT's transmitter to the DSO.
3. Measure the common mode amplitude.
4. Apply a histogram function over 1 UI of the signal.

**Observable Results:**

a. The AC common mode output voltage shall be no greater than 7.5 mV, RMS.

**Possible Problems:** None

**Test 86A.1.4– Transition Time**

**Purpose:** To verify that the rising and falling edge transition times are within the conformance limits.

**References:**

[1] IEEE Std. 802.3-2012, Table 86A-3 – Module electrical output specifications
[2] IEEE Std. 802.3-2012, subclause 86A.5.3.3 – Transition time
[3] IEEE Std. 802.3-2012, Table 86A-6 – Test Patterns
[4] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

**Resource Requirements:** See Appendix I

**Last Modification:** April 7, 2014

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR4 devices. This specification includes conformance requirements for the rising and falling edge transition times defined in [2].

In this test, the transition time is measured while the DUT is connected to the DSO. The transition times are to be measured at the 20% and 80% levels as defined in [2]. Reference [2] also requires that the measurement be done using the square wave test pattern defined in [3] and [4], with no equalization and a run of at least eight consecutive ones.

**Test Setup:** See Appendix I

**Test Procedure:**

1. Configure the DUT so that it is sourcing the square wave test pattern with no equalization.
2. Connect the DUT's transmitter to the DSO.
3. Capture a run of at least eight consecutive ones.
4. Measure the rising and falling edge transition times.

**Observable Results:**

a. The rising and falling edge transition times shall be greater than 28 ps.

**Possible Problems:** None

**Test 86A.1.5 – Jitter Output**

**Purpose:** To verify that the DC common mode output voltage of the DUT is within the conformance limits

**References:**

[1] IEEE Std. 802.3-2012, Table 86A-3 – Module electrical output specifications
[2] IEEE Std. 802.3-2012, subclause 86.8.3.3.1 – J2 Jitter
[3] IEEE Std. 802.3-2012, subclause 86.8.3.3.2 – J9 Jitter
[4] IEEE Std. 802.3-2012, Table 86A-6
[5] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

**Resource Requirements:** See Appendix I

**Last Modification:** April 7, 2014

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR10 devices. This specification includes conformance requirements for J2 and J9 defined.

In this test, the jitter output tolerance is measured while the DUT is connected to the DSO. References [2], [3], and [4] also require that the DUT be transmitting test pattern PRBS31 [5].

**Test Setup:** See Appendix I

**Test Procedure:**

1. Configure the DUT to send test pattern 3 (PRBS31).
2. Connect the DUT's transmitter to the DSO.
3. Measure the J2 and J9 jitter.

**Observable Results:**

a. The J2 shall be no greater than 0.42 UI.
b. The J9 shall be no greater than 0.65 UI.

**Possible Problems:** None

**Test 86A.1.6 – Transmitter Eye Mask**

**Purpose:** To verify that the bit error ratio (BER) of the DUT's receiver is within the conformance limits

**References:**

[1] IEEE Std. 802.3-2012, Table 86A - 3 – Module electrical output specifications
[2] IEEE Std. 802.3-2012, subclause 86A.5.3.6 – Eye mask for TP1a and TP4
[3] IEEE Std. 802.3-2012, subclause 83A.3.4.2 – Input signal definition
[4] IEEE Std. 802.3-2012, subclause 86.8.3.2 – Eye diagrams
[5] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition
[6] IEEE Std. 802.3-2012, subclause 86A.5.3.8.1 – Introduction

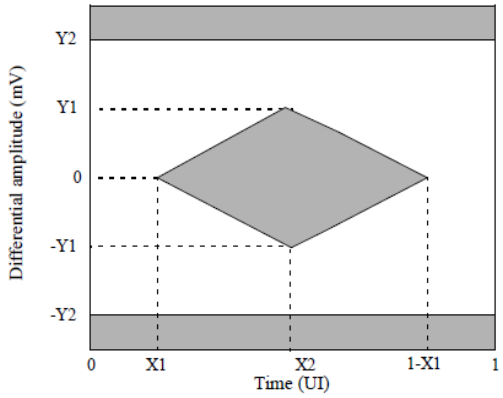
**Resource Requirements:** See Appendix I

**Last Modification:** April 7, 2014

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR4 devices. This specification includes conformance requirements for the eye diagram defined in [2].

In this test, the eye diagram is measured while the DUT is connected to DSO. Reference [3] also requires that the DUT be transmitting test pattern 3 (PRBS31) or scrambled idle as defined in [4] and [5] during this test.




X1 = 0.29 UI X2 = 0.5 UI Y1 = 150 mV Y2 = 425 mV

**Test Setup:** See Appendix I

**Test Procedure:**

1. Configure de-emphasis on the DUT to the "off" state as defined by [3].
2. Configure the DUT so that it is sourcing test pattern 3 (PRBS31) or scrambled idle.
3. Connect a crosstalk source to all remaining lanes.
4. Connect the DUT's transmitter to DSO.
5. Capture the eye diagram.

**Observable Results:**

a. The receiver shall match the eye diagram with a hit ratio of $5x10^{-5}$

**Possible Problems:** None

# GROUP 2: RX ELECTRICAL SIGNALING REQUIREMENTS

**Overview:**

The tests defined in this section verify the receiver electrical signaling characteristics of the Physical Medium Dependent (PMD) layer defined in Clause 86A of IEEE 802.3-2012.

**Test 86A.2.1 – Module Input Signal Tolerance**

**Purpose:** To verify that the bit error ratio (BER) of the DUT's receiver is within the conformance limits

**References:**

[1] IEEE Std. 802.3-2012, Table 86A - 2 – nPPI module electrical input specifications at TP1 and TP1a
[2] IEEE Std. 802.3-2012, Table 86A – 6 – Test patterns and related subclauses
[3] IEEE Std. 802.3-2012, subclause 86A.5.3.8 – Host Input Signal Tolerance

**Resource Requirements:** See Appendix I

**Last Modification:** April 8, 2014

**Discussion:**
Reference [1] specifies the compliance characteristics for 40GBASE-R and 100GBASE-R modules. This specification includes conformance requirements for the receiver tolerance defined in [3]. A major problem in communicating of multi-channel transceivers is interference. The interfering signal can come from a variety of sources including: a) Crosstalk from other data channels running the same kind of signals as the channel of interest. This type of interference is usually subdivided into:1) Far-end crosstalk (FEXT) coming from data traveling in the same general direction as the channel of interest.2) Near-end crosstalk (NEXT) originating from a channel with a transmitter near the receiver of the channel of interest. b) Self interference caused by reflections due to impedance discontinuities, stubs, etc. This is a form of intersymbol interference (ISI) that is beyond what a reasonable equalizer can compensate. c) Alien crosstalk which is defined to be interference from unrelated sources such as clocks, other kinds of data, power supply noise, etc. For the channel to work, the receiver must be able to extract correct data from the lossy channel in the presences of interference. The ability of the receiver to extract data in the presence of interference is an important characteristic of the receiver and needs to be measured. This ability is called interference tolerance.

In this test, BER is measured while the DUT is subjected to a compliant input signal with interference as specified in [3]. The nPPI jitter tolerance test setup in Figure 86A–8 or its equivalent shall meet the receiver eye mask defined in Table 86A–2. Random jitter is added to the test signal using an interference generator which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The random interference generator must have a minim power spectrum -3 dB point of 6 GHz with a crest factor of no less than 7. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask defined in Table 86A–2. All nPPI lanes shall be active during jitter tolerance testing. The PRBS31 pattern defined in 83.5.10 or scrambled idle defined in 82.2.10 is used for evaluating nPPI jitter tolerance.

**Test Setup:** See Appendix I

**Test Procedure:**

1. Configure the DUT so that it is sourcing test pattern 3 (PRBS31).
2. Connect the DUT's receiver to a jitter source that is capable of operating as defined in [1] and [3].
3. Calculate the BER based on the received bits.

**Observable Results:**

b. The receiver shall operate with a BER of better then $10^{-12}$

**Possible Problems:** None

# GROUP 3: IMPEDANCE REQUIREMENTS

**Overview:**

The tests defined in this section verify the impedance characteristics of the Physical Medium Dependent (PMD) layer defined in Clause 86A of IEEE 802.3.

**Test 86A.3.1 – Differential Input and Output Return Loss**

**Purpose:** To verify that the differential output return loss of the DUT is within the conformance limits

**References:**

[1] IEEE Std. 802.3-2012, subclause 86A.4.1.1 – Differential Return Losses
[2] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

**Resource Requirements:** See Appendix I

**Last Modification:** April 7, 2014

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR4 devices. This specification includes conformance requirements for the differential output return loss.

For the purpose of this test, the differential output return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 10 MHz to 11.1 GHz, the differential return loss of the driver shall not exceed the limit given in Equation 86A-1:

$$Return\_loss(f) \geq \begin{cases} 12 - 2\sqrt{f} & 0.01 \leq f < 4.11 \\ 6.3 - 13\log_{10}\left(\frac{f}{5.5}\right) & 4.11 \leq f \leq 11.1 \end{cases} \text{ dB}$$

**Test Setup:** See Appendix I

**Test Procedure:**

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing normal IDLE signaling [2].
3. Connect the DUT's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11 GHz.
5. Compute the return loss from the reflection coefficient values.

**Observable Results:**

a. The differential output return loss shall exceed the limits described by Equation 86A-1.
b. The differential input return loss shall exceed the limits described by Equation 86A-1.

**Possible Problems:** None

**Test 86A.3.2 – Differential to Common Mode Input Return Loss**

**Purpose:** To verify that the common-mode output return loss of the DUT is within the conformance limits

**References:**

[1] IEEE Std. 802.3-2012, Table 86A-2 – Host electrical input specifications
[2] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

**Resource Requirements:** See Appendix I

**Last Modification:** July 10, 2013

**Discussion:**

Reference [1] specifies the characteristics for 40GBASE-SR4 and 100GBASE-SR4 devices. This specification includes conformance requirements for the differential to common-mode output return loss.

For the purpose of this test, the common-mode output input loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the receiver. The reference impedance for differential return loss measurements is 100 Ω, and the common mode reference is 25Ω. For this test use TP4a.

**Test Setup:** See Appendix I

**Test Procedure:**

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing normal IDLE signaling [2].
3. Connect the DUT's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
5. Compute the return loss from the reflection coefficient values.

**Observable Results:**

a. The differential to common mode input return loss shall be greater than 10 dB.

**Possible Problems:** None

**Test 86A.3.3 – Termination Mismatch**

**Purpose:** To verify that the termination of the DUT is within the conformance limits.

**References:**

[1] IEEE Std. 802.3-2012, Table 86A-3 – Module electrical output specifications
[2] IEEE Std. 802.3-2012, subclause 86A.5.3.2- Termination mismatch
[3] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

**Resource Requirements:** See Appendix I

**Last Modification:** April 7, 2014

**Discussion:**

Reference [1] specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR4 devices. This specification includes conformance requirements for the maximum termination mismatch at 1MHz defined in [2].

For the purpose of this test, the termination mismatch is defined as the percentage difference between the two low-frequency impedances to common of a differential electrical port.

$$\Delta Z_M = 2 * \frac{|Z_p - Z_n|}{Z_p - Z_n} * 100\% \qquad (EQ.86A - 10)$$

**Test Setup:** See Appendix I

**Test Procedure:**

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's transmitter to the VNA sourcing square wave pattern [3].
3. Observe the positive and negative impedances of the DUT at 1MHz.
4. Using the values from the positive and negative impedances compute the termination mismatch with equation 86A - 10.

**Observable Results:**

a. The termination mismatch shall be less than 5%.

**Possible Problems:** None

# APPENDICES

**Overview:**

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

**Scope:**

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

**Appendix I - Test Fixtures and Setups**

**Purpose:** To specify the measurement hardware, test fixtures, and setups used in this test suite

**References:**

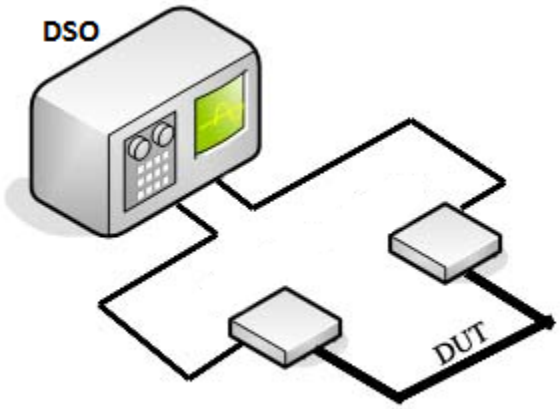
[1] IEEE Std. 802.3-2012, Annex 86A

**Last Modification:** September 11, 2013

**Setup A**

**Equipment List:**

1. Digital Storage Oscilloscope, 20 GHz bandwidth (minimum)
2. Post Processing Capabilities
3. 50Ω matched coax cables
4. Module compliance board

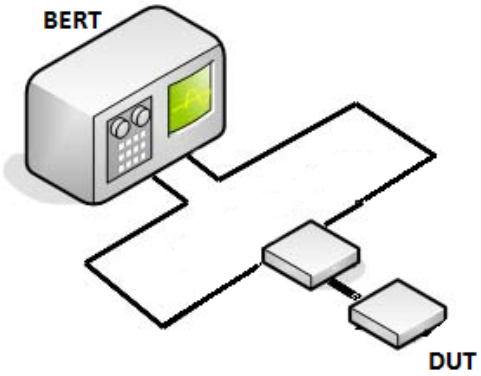



**86A I: Setup A used for Group 1**

**Setup B**

**Equipment List:**

1. BERT Scope
2. Post Processing Capabilities
3. 50Ω matched coax cables
4. Host compliance board




**86A I: Setup B used for Group 2**

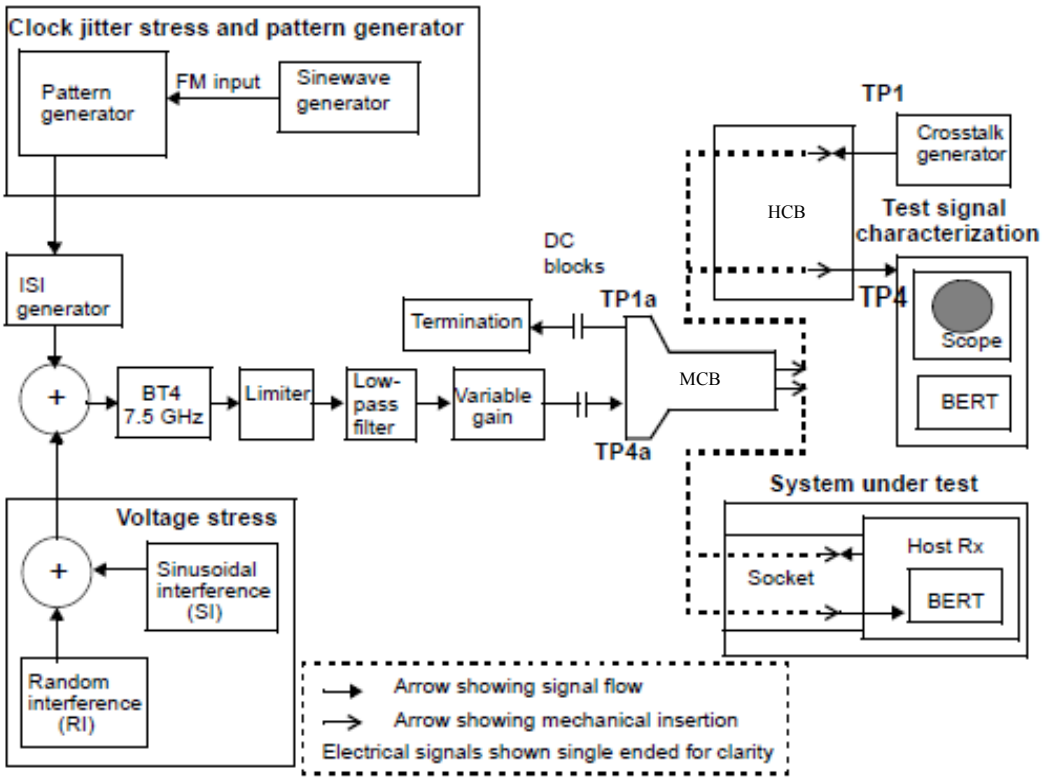


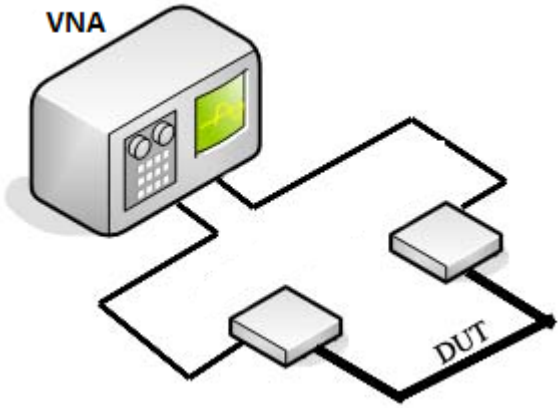

**Figure 86A–8—Example jitter tolerance test configuration**

**83B I: Figure 86A - 8**

**Setup C**

**Equipment List:**

1. Vector Network Analyzer
2. Post Processing Capabilities
3. 50Ω matched coax cables
4. Module compliance board




**86A I: Setup C used for Group 3**