40 AND 100 GIGABIT ETHERNET CONSORTIUM

Clause 83A
40GBASE-R and 100GBASE-R PMA Test Suite
Version 0.1

Technical Document

Last Updated: April 8, 2014

40 and 100 Gigabit Ethernet Consortium

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MODIFICATION RECORD

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Alexander McQuade: Informal preliminary draft.

April 8, 2014 Version 1.0

Michael Klempa Initial draft.

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Alexander McQuade	UNH InterOperability Laboratory
Michael Klempa	UNH InterOperability Laboratory
Jeff Lapak	UNH InterOperability Laboratory
Curtis Donahue	UNH InterOperability Laboratory

INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the functionality of the Physical Medium Attachment (PMA) sublayer of their 40GBASE-R and 100GBASE-R products.

These tests are designed to determine if a product conforms to specifications defined in Clause 83A of the IEEE 802.3 2012 Standard. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 40GBASE-R and 100GBASE-R environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

Test Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

GROUP 1: ELECTRICAL SIGNALING REQUIREMENTS

Overview:

The tests defined in this section verify the electrical signaling characteristics of the Physical Medium Attachment (PMA) layer defined in Clause 83A of IEEE 802.3-2012.

Test 83A.1.1 – Signaling Speed

Purpose: To verify that the baud rate of the DUT is within the conformance limits.

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.1.2 – Rate of Operation

Resource Requirements: See Appendix I

Last Modification: July 1, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the signaling speed, which is 10.3125 Gbaud +/- 100 ppm per lane. This translates to 10.3125 Gbaud +/- 1.03125 Mbaud, with a nominal Unit Interval (UI) of 96.96 ps.

Reference [2] specifies the overall signaling speed for 40GBASE-R and 100GBASE-R devices. This specification includes the number of lanes in parallel from the transmitter to achieve the necessary speeds for XLAUI and CAUI.

In this test, the signaling speed is measured while the DUT is connected to the DSO. The signal being transmitted by the DUT may be any valid 40GBASE-R or 100GBASE-R signal.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT to send a valid signal or test pattern.
2. Connect the DUT's transmitter to the DSO.
3. Measure the average TX signaling speed.

Observable Results:

a. The signaling speed per lane shall be within 10.3125 Gbaud +/- 1.03125 Mbaud

Possible Problems: None.

Test 83A.1.2 – Single-Ended Output Voltage

Purpose: To verify that the single ended output voltage of the DUT is within the conformance limits

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.1 – Output amplitude
[3] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the single ended output voltage defined in [2].

In this test, the single-ended output voltage is measured at the Transmit Compliance Point of the DUT. The signal being transmitted by the DUT may be any valid 40GBASE-R or 100GBASE-R signal, however the test pattern 4 (PRBS9) defined in [3] will be used, primarily out of convenience, as this pattern is also used for several other tests in this group.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT to send test pattern 4 (PRBS9).
2. Connect the DUT's transmitter to the DSO.
3. Measure the single-ended output voltage of SLi<p> or SLi<n> at the test point.

Observable Results:

a. The single-ended output voltage shall be between -0.4 V and 4 V with respect to ground.

Possible Problems: None

Test 83A.1.3 – Maximum Differential Output Voltage

Purpose: To verify that the differential output amplitude of the DUT transmitter is within the conformance limits.

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.1 – Output amplitude
[3] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the differential output amplitude defined in [2].

In this test, the maximum differential peak-to-peak output voltage is measured while the DUT is connected to the DSO. The signal being transmitted by the DUT may be any valid 40GBASE-R or 100GBASE-R signal. However a PRBS9 pattern [3] will be used.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT to send a test pattern 4 (PRBS9).
2. Connect the DUT's transmitter to the DSO.
3. Measure the maximum peak-to-peak differential output voltage.

Observable Results:

a. The maximum differential peak-to-peak output voltage shall be less than 760 mV, regardless of equalization setting.

Possible Problems: None

Test 83A.1.4 – Transition Time

Purpose: To verify that the rising and falling edge transition times are within the conformance limits.

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.2 – Rise/fall time
[3] IEEE Std. 802.3-2012, subclause 83.5.10 – PMA test patterns

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the rising and falling edge transition times defined in [2].

In this test, the transition time is measured while the DUT is connected to the DSO. The transition times are to be measured at the 20% and 80% levels as defined in [2]. Reference [2] also requires that the measurement be done using the square wave test pattern defined in [3], with no equalization and a run of at least eight consecutive ones.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT so that it is sourcing the square wave test pattern with no equalization.
2. Connect the DUT's transmitter to the DSO.
3. Capture a run of at least eight consecutive ones.
4. Measure the rising and falling edge transition times.

Observable Results:

a. The rising and falling edge transition times shall be greater than or equal to 24 ps.

Possible Problems: None

Test 83A.1.5 – De-emphasis

Purpose: To verify that the de-emphasis of the DUT transmitter is within the conformance limits.

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.1 – Output amplitude
[3] IEEE Std. 802.3-2012, subclause 86.8.2 – Test patterns and related subclauses
[4] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for de-emphasis defined in [2].

In this test, the VMA is measured at the Transmitter Compliance Test point of the DUT. The signal being transmitted by the DUT may be a square wave or test pattern 4 (PRBS9) defined in [3] and [4].

$$De-emphasis\ (dB) = 20\log_{10}\left(\frac{Differential\ peak-to-peak\ amplitude}{VMA}\right) \qquad (EQ.\ 83A-3)$$

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT to send a square wave or test pattern 4 (PRBS9).
2. Connect the DUT's transmitter to the DSO.
3. Measure the VMA.
4. Using Equation 83A-3 calculate the DUT's de-emphasis.

Observable Results:

a. The de-emphasis shall be between 4.4 dB and 7 dB.

Possible Problems: None

Test 83A.1.6 – Minimum VMA

Purpose: To verify that the minimum VMA of the DUT transmitter is within the conformance limits.

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.1 – Output amplitude
[3] IEEE Std. 802.3-2012, subclause 83A.3.3.2 – Rise/fall time
[4] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for minimum VMA defined in [2].

In this test, the transition time is measured while the DUT is connected to the DSO. The transition times are to be measured at the 20% and 80% levels as defined in [3]. Reference [3] also requires that the measurement be done using the square wave test pattern defined in [4], with a run of at least eight consecutive ones.

$$Minimum\ VMA\ (mV) = (234.64 - 2.13 + 0.18x^2) * 1.32\left(10^{\frac{-y}{20}}\right) \qquad (EQ. 83A-4)$$

Where

x = rise or fall time (whichever is larger) in ps
y = de-emphasis value in dB

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT to send a square wave or test pattern 4 (PRBS9).
2. Connect the DUT’s transmitter to the DSO.
3. Observe the transmitted de-emphasis from test 83.1.4.
4. Measure the rise or fall time (whichever is larger) in ps.
5. Using Equation 83A-3 calculate the DUT’s minimum VMA.

Observable Results:

a. The minimum VMA shall be greater than equation 83A-4 using the values obtained in steps 3 and 4 of the test procedure.

Possible Problems: None

Test 83A.1.7 – AC Common Mode Output Voltage

Purpose: To verify that the AC common mode output voltage of the DUT is within the conformance limits

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 86A.5.3.1 – AC common-mode voltage
[3] IEEE Std. 802.3-2012, Table 86-11 – Test-pattern definition

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for maximum out AC common-mode voltage defined in [2]. The pattern used will be PRBS31 as defined in [3].

In this test, the differential amplitude is measured while the DUT is connected to the DSO. The common mode voltage can be found by averaging the signal+ and signal- at any time. RMS AC common-mode voltage may be calculated by applying the histogram function over 1 UI to the common mode signal.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT to send test pattern 3 (PRBS31).
2. Connect the DUT's transmitter to the DSO.
3. Measure the common mode amplitude.
4. Apply a histogram function over 1 UI of the signal.

Observable Results:

a. The AC common mode output voltage shall be no greater than 15 mV, RMS.

Possible Problems: None

Test 83A.1.8 – Transmit Jitter

Purpose: To verify that the peak-to-peak transmit jitter of the DUT is within the conformance limits

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.5– Transmitter eye mask and transmitter jitter definition
[3] IEEE Std. 802.3-2012, subclause 83A.5.1 – Transmit jitter
[4] IEEE Std. 802.3-2012, subclause 83.5.10 – PMA test patterns (optional)
[5] IEEE Std. 802.3-2012, subclause 82.2.10 – Test-pattern generators

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the peak-to-peak transmit jitter defined in [2] and [3].

In this test, the peak-to-peak transmit jitter is measured while the DUT is connected to the DSO. Reference [3] also requires that the DUT be transmitting test pattern PRBS31 as defined in [4] or scrambled idle as defined in [5] during this test.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT so that it is sourcing test pattern 3 (PRBS31) or scrambled idle.
2. Set the de-emphasis on the DUT to the "off" state as defined by [3]
3. Connect the DUT's transmitter to DSO.
4. Measure the random jitter, deterministic jitter, duty cycle distortion, and total transmit jitter.

Observable Results:

a. The Deterministic Jitter value shall not exceed 0.17 UI.
b. The Total Jitter value shall not exceed 0.32 UI.

Possible Problems: None

Test 83A.1.9 – Transmitter Eye Diagram

Purpose: To verify that the transmitter meets the eye mask conformance limits

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.5– Transmitter eye mask and transmitter jitter definition
[3] IEEE Std. 802.3-2012, subclause 83A.5.1 – Transmit jitter
[4] IEEE Std. 802.3-2012, subclause 83.5.10 – PMA test patterns (optional)
[5] IEEE Std. 802.3-2012, subclause 82.2.10 – Test-pattern generators

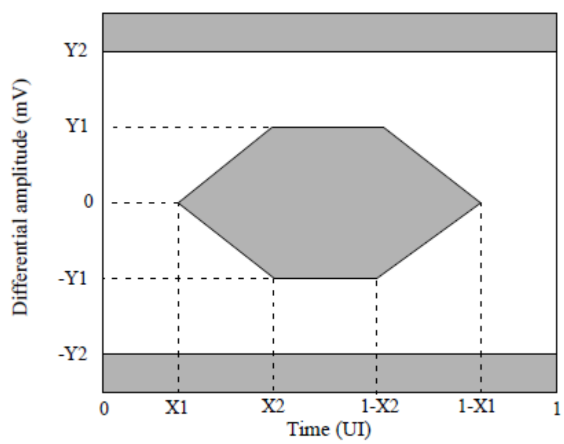
Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the eye diagram defined in [2] and [3].

In this test, the eye diagram is measured while the DUT is connected to DSO. Reference [3] also requires that the DUT be transmitting test pattern PRBS31 as defined in [4] or scrambled idle as defined in [5] during this test.



X1 = 0.16 UI X2 = 0.38 UI Y1 = 200 mV Y2 = 380 mV

Test Setup: See Appendix I

Test Procedure:

1. Configure de-emphasis on the DUT to the "off" state as defined by [3].
2. Configure the DUT so that it is sourcing test pattern 3 (PRBS31) or scrambled idle.
3. Make sure all the DUT's transmit lanes are active and all receive lanes are receiving maximum amplitude and fastest rise time as defined in [1]
4. Connect the DUT's transmitter to DSO.
5. Capture the eye diagram.

Observable Results:

a. The eye diagram should stay within the mask shown above.

Possible Problems: None

GROUP 2: RX ELECTRICAL SIGNALING REQUIREMENTS

Overview:

The tests defined in this section verify the receiver electrical signaling characteristics of the Physical Medium Dependent (PMD) layer defined in Clause 83B of IEEE 802.3-2012.

Test 83A.2.1 – Receiver Tolerance

Purpose: To verify that the bit error ratio (BER) of the DUT's receiver is within the conformance limits

References:

[1] IEEE Std. 802.3-2012, Table 83A - 2 – Specifications at module compliance points
[2] IEEE Std. 802.3-2012, Table 86A – 6 – Test patterns
[3] IEEE Std. 802.3-2012, subclause 83A.5.2 - Receiver tolerance
[4] IEEE Std. 802.3-2012, subclause 83.5.10 – PMA test patterns (optional)

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the compliance characteristics for 40GBASE-R and 100GBASE-R modules. This specification includes conformance requirements for the receiver tolerance defined in [3]. A major problem in communicating of multi-channel transceivers is interference. The interfering signal can come from a variety of sources including: a) Crosstalk from other data channels running the same kind of signals as the channel of interest. This type of interference is usually subdivided into:1) Far-end crosstalk (FEXT) coming from data traveling in the same general direction as the channel of interest.2) Near-end crosstalk (NEXT) originating from a channel with a transmitter near the receiver of the channel of interest. b) Self interference caused by reflections due to impedance discontinuities, stubs, etc. This is a form of intersymbol interference (ISI) that is beyond what a reasonable equalizer can compensate. c) Alien crosstalk which is defined to be interference from unrelated sources such as clocks, other kinds of data, power supply noise, etc. For the channel to work, the receiver must be able to extract correct data from the lossy channel in the presences of interference. The ability of the receiver to extract data in the presence of interference is an important characteristic of the receiver and needs to be measured. This ability is called interference tolerance.

In this test, BER is measured while the DUT is subjected to a compliant input signal with interference as specified in [3]. The XLAUI/CAUI jitter tolerance test setup in Figure 83A–15 or its equivalent shall meet the receiver eye mask defined in Table 83A–2. Random jitter is added to the test signal using an interference generator which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from 50 MHz to 6 GHz with a crest factor of no less than 5. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask defined in Table 83A–2. All XLAUI/CAUI lanes shall be active during jitter tolerance testing. The PRBS31 pattern defined in [4] or scrambled idle defined in 82.2.10 is used for evaluating XLAUI/CAUI jitter tolerance.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT so that it is sourcing test pattern 3 (PRBS31).
2. Connect the DUT's receiver to a jitter source that is capable of operating as defined in [3].
3. Calculate the BER based on the received bits.

Observable Results:

a. The receiver shall operate with a BER of better then 10^{-12}

Possible Problems: None

GROUP 3: IMPEDANCE REQUIREMENTS

Overview:

The tests defined in this section verify the impedance characteristics of the Physical Medium Attachment (PMA) layer defined in Clause 83 of IEEE 802.3ap.

Test 83A.3.1 – Differential Input and Output Return Loss

Purpose: To verify that the differential output return loss of the DUT is within the conformance limits

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.3– Differential output return loss
[3] IEEE Std. 802.3-2012, subclause 83A.3.4.3– Differential input return loss
[4] IEEE Std. 802.3-2012, subclause 83.5.10 – PMA test patterns (optional)

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the differential output return loss, which are specified in [2].

For the purpose of this test, the differential input and output return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 10 MHz to 11.1 GHz, the differential return loss of the driver shall exceed Equation 83A-5. The reference impedance for differential return loss measurements is 100 Ω

$$Return\_loss(f) \geq \begin{Bmatrix} 12 & 0.01 \leq f \leq 2.125 \\ 6.5 - 13.33\log_{10}\left(\frac{f}{5.5}\right) & 2.125 \leq f \leq 11.1 \end{Bmatrix} (dB) \qquad (EQ.83A-5)$$

Test Setup: See Appendix I

Test Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing normal IDLE signaling [4].
3. Connect the DUT's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
5. Compute the return loss from the reflection coefficient values.

Observable Results:

a. The differential output return loss shall exceed the limits described by Equation 83A-5.
b. The differential input return loss shall exceed the limits described by Equation 83A-5.

Possible Problems: None

Test 83A.3.2 – Common-Mode Output Return Loss

Purpose: To verify that the common-mode output return loss of the DUT is within the conformance limits

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 83A.3.3.4– Common-mode output return loss
[3] IEEE Std. 802.3-2012, subclause 83.5.10 – PMA test patterns (optional)

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the common-mode output return loss defined in [2].

For the purpose of this test, the common-mode output return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 10 MHz to 11.1 GHz, the common-mode return loss of the driver shall exceed Equation 83A-6. The reference impedance for common-mode return loss measurements is 25 Ω.

$$Return\_loss(f) \geq \left\{ \begin{array}{cc} 9 & 0.01 \leq f \leq 2.125 \\ 3.5 - 13.33\log_{10}\left(\frac{f}{5.5}\right) & 2.125 \leq f \leq 7.1 \\ 2 & 7.1 \leq f \leq 11.1 \end{array} \right\} (dB) \qquad (EQ.83A-6)$$

Test Setup: See Appendix I

Test Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing normal IDLE signaling [3].
3. Connect the DUT's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
5. Compute the return loss from the reflection coefficient values.

Observable Results:

a. The common-mode output return loss shall exceed the limits described by Equations 83A-6.

Possible Problems: None

Test 83A.3.3 – Maximum Termination Mismatch at 1MHz

Purpose: To verify that the common-mode output return loss of the DUT is within the conformance limits

References:

[1] IEEE Std. 802.3-2012, subclause 83A.3.3 – Transmitter Characteristics
[2] IEEE Std. 802.3-2012, subclause 86A.5.3.2 – Termination mismatch
[3] IEEE Std. 802.3-2012, subclause 83.5.10 – PMA test patterns (optional)

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for 40GBASE-R and 100GBASE-R devices. This specification includes conformance requirements for the maximum termination mismatch at 1MHz defined in [2].

For the purpose of this test, the termination mismatch is defined as the percentage difference between the two low-frequency impedances to common of a differential electrical port.

$$\Delta Z_M = 2 * \frac{|Z_p - Z_n|}{Z_p - Z_n} * 100\% \qquad (EQ. 86A - 10)$$

Test Setup: See Appendix I

Test Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing low frequency signaling [3].
3. Connect the DUT's positive transmitter to the VNA.
4. Observe the Impedance for the positive channel.
5. Repeat steps 3 and 4 for the negative channel.
6. Using the values from the positive and negative impedances compute the termination mismatch with equation 86A - 10.

Observable Results:

a. The termination mismatch shall be no greater than 5%.

Possible Problems: None

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Appendix I - Test Fixtures and Setups

Purpose: To specify the measurement hardware, test fixtures, and setups used in this test suite

References:

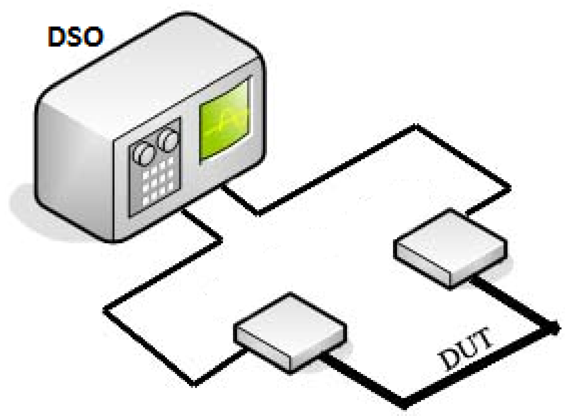
[1] IEEE Std. 802.3-2012, Annex 86A

Last Modification: September 11, 2013

Setup A

Equipment List:

1. Digital Storage Oscilloscope, 20 GHz bandwidth (minimum)
2. Post Processing Capabilities
3. 50Ω matched coax cables
4. Module compliance board

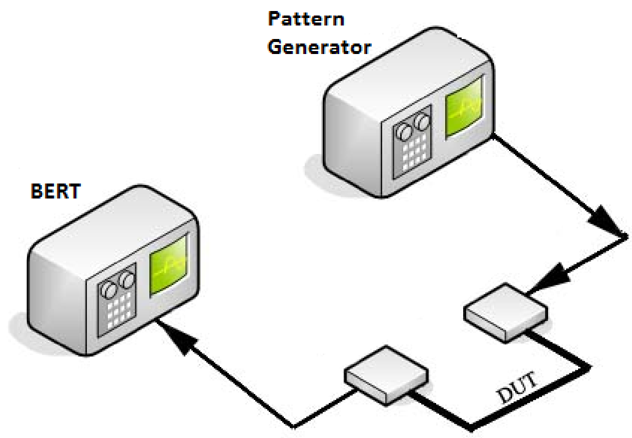


86A I: Setup A used for Group 1

Setup B

Equipment List:

1. BERT Scope
2. Pattern Generator
3. Post Processing Capabilities
4. 50Ω matched coax cables
5. Module compliance board

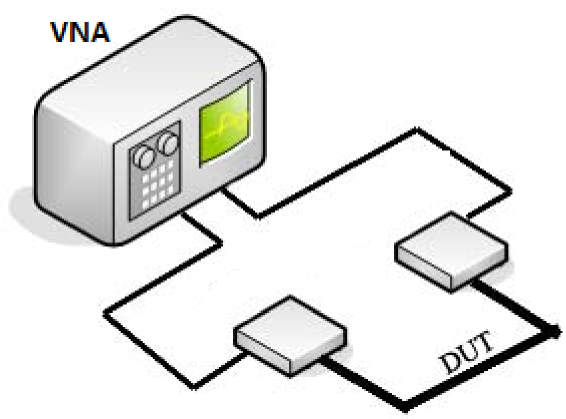


86A I: Setup B used for Group 2

Setup C

Equipment List:

1. Vector Network Analyzer
2. Post Processing Capabilities
3. 50Ω matched coax cables
4. Module compliance board



86A I: Setup C used for Group 3