GIGABIT ETHERNET CONSORTIUM

Clause 40 1000BASE-T Energy Efficient Ethernet Test Suite

Version 1.0

Technical Document

Last Updated: December 10, 2010 3:43 PM

Gigabit Ethernet Consortium

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MODIFICATION RECORD

Revision	Release Date	Author	Comments
1.0	12/10/2010	Curtis Donahue Jon Beckwith	• Initial public release

ACKNOWLEDGMENTS

The University of New Hampshire would like to acknowledge the efforts of the following individuals in the development of this test suite.

Jon Beckwith	UNH InterOperability Laboratory
Eric-Thomas Arroyo	UNH InterOperability Laboratory
Curtis Donahue	UNH InterOperability Laboratory

INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the functionality of the PCS and PMA sublayers of their Energy Efficient Ethernet (EEE) capable 1000BASE-T Gigabit Ethernet products.

These tests are designed to determine if a product conforms to specifications defined in Clause 40 of the IEEE 802.3™az-2010 Standard. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 1000BASE-T EEE environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3™ standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

Test Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

GROUP 1: LPI ELECTRICAL MEASUREMENTS

Overview:

The tests defined in this section verify the LPI mode voltage and timing parameters defined for Energy Efficient capable 1000BASE-T PHYs in sections 40.4.5.2, 40.6, and 78.2 of the IEEE Std 802.3az-2010^{TM}.

These tests are designed to verify that the device under test transmits low power idle signaling with the proper timing and voltage parameters. All tests in this section utilize the setup found in Appendix 40.A.

Test 40.1.1 – Sleep time

Purpose: To verify the amount of time the DUT transmits the SLEEP signal is within the conformance limits.

References:

[1] IEEE std 802.3az-2010™, subclause 78.2 – LPI mode timing parameters description
[2] Ibid., subclause 40.4.5.2 – Timers

Resource Requirements: See Appendix 40.A

Last Modification: July 2, 2010

Discussion:

Reference [1] specifies the length of time, T_s, the phy transmits the SLEEP signal before shutting down all transmitters and entering the QUIET state. The value measured in this test is the value the DUT used for its' lpi_update_timer and lpi_postupdate_timer.

The lpi_update_timer is used to control the amount of time the DUT remains in the UPDATE state and the tx_mode is set to SEND_I. This timer is measured by decoding the refresh signals, beginning with the time that the DUT begins sending IDLE and ending with the time when the DUT sets loc_update_done=TRUE. The lpi_postupdate_timer is used to allow for an appropriate amount of time for the remote device to signal rem_update_done. This timer is measured by decoding the refresh signals, beginning with the time that the DUT begins sending loc_update_done=TRUE and ending with the time when the DUT enters the WAIT_QUIET state.

Test Setup: See Appendix 40.A

Test Procedure:

Part a) Master mode

1. Establish a 1000BASE-T EEE link with the DUT forced into master mode.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.
4. Capture SLEEP waveform.
5. Decode the waveform prior to the quiet state.
6. Measure T_s.
7. Repeat for multiple captures.

Part b) Slave mode

1. Establish a 1000BASE-T EEE link with the DUT forced into slave mode.
2. Establish a link between EEE capable 1000BASE-T DUT and LP.
3. Force DUT to request low power idle mode.
4. Force test station to request low power idle mode.
5. Capture SLEEP waveform.
6. Decode the waveform prior to the quiet state.
7. Measure T_s.
8. Repeat for multiple captures.

Observable Results

Part a) Master mode

a. T_s should be greater than 232µs and less than 253.2µs.
b. See Table 40.1.1 for additional sleep timing parameters.

Part b) Slave mode

a. T_s should be greater than 182µs and less than 203.2µs.
b. See Table 40.1.1 for additional sleep timing parameters.

Table 40.1.1			
Timers		**Minimum value (μs)**	**Maximum value (μs)**
lpi_update_timer	Case 1: Master	230	250
	Case 2: Slave	180	200
lpi_postupdate_timer		2.0	3.2

Possible Problems: None

Test 40.1.2 – Quiet time

Purpose: To verify the amount of time the DUT remains silent in the QUIET state is within the conformance limits.

References:

[1] IEEE std 802.3az-2010™, subclause 78.2 – LPI mode timing parameters description
[2] Ibid., subclause 40.4.5.2 – Timers

Resource Requirements: See Appendix 40.A

Last Modification: July 2, 2010

Discussion:

Reference [1] specifies the length of time, T_q, the DUT is in the QUIET state. The value measured in this test is the value of the DUT used for its' lpi_waitwq_timer and lpi_quiet_timer.

The lpi_quiet_timer defines the maximum amount of time the PHY will remain quiet. This timer is measured as the amount of time in-between the refresh signals. Since 1000BASE-T uses a wake transient at the beginning of refresh signals, let the beginning of the wake transient signal be defined as the beginning of the WAKE state. As the PHY will remain quiet during both WAIT_QUIET and QUIET, there is no way to distinguish between them at the MDI. For this reason, the total quiet time is measured as the sum of the two timers.

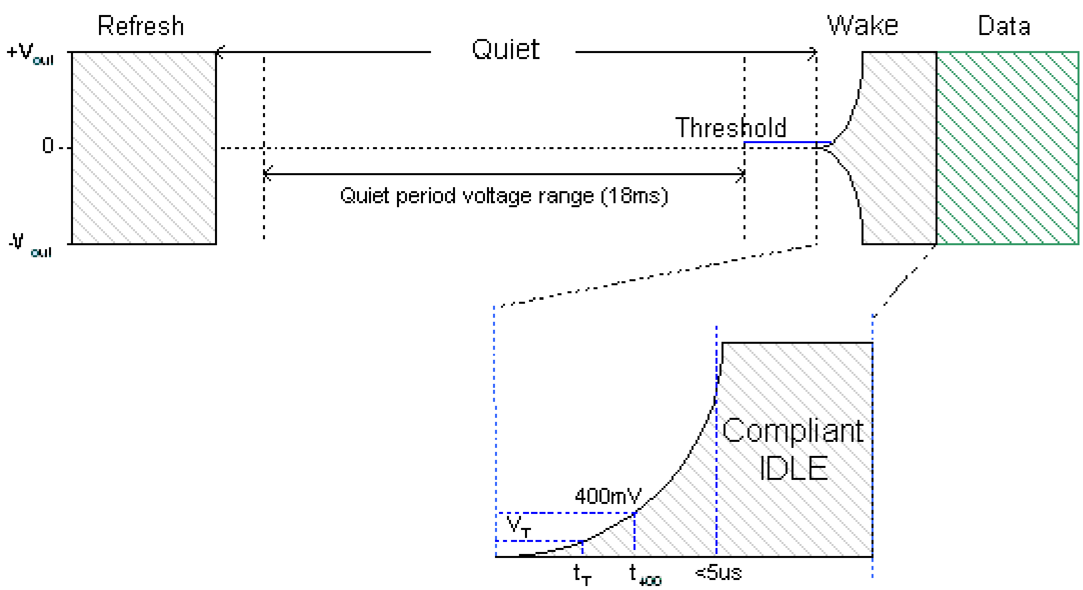


Figure 40.1.2-1: Quiet Period Voltage and tx_quiet deassertion threshold

Test Setup: See Appendix 40.A

Test Procedure:

1. Establish a 1000BASE-T EEE link.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.
4. Capture QUIET waveform.
5. Measure T_q.
6. Repeat for multiple captures.

Observable Result:

a. T_q should be greater than (20ms + 10µs) and less than (24ms + 12µs).
b. INFORMATIVE: Measure the peak transmit voltage during quiet period. There should be no stray signaling or transitions observed.

Possible Problems: The DUT may prematurely exit the quiet state if there are frames being sent. In these circumstances, the measured quiet time may not reflect the value of T_q and should not be included as part of the measurement.

Test 40.1.3 – Refresh time

Purpose: To verify the amount of time the DUT transmits the refresh signal is within the conformance limits.

References:

[1] IEEE std 802.3az-2010™, subclause 78.2 – LPI mode timing parameters description
[2] Ibid., subclause 40.4.5.2 – Timers

Resource Requirements: See Appendix 40.A

Last Modification: December 10, 2010

Discussion:

Reference [1] specifies the time, T_r, that the DUT transmits the REFRESH signal before entering the QUIET state. The values measured in this test are the values the DUT uses for its' lpi_waketx_timer, lpi_wakemz_timer, lpi_update_timer, and lpi_postupdate_timer.

The lpi_waketx_timer defines the time that a PHY will transmit IDLE upon entering the WAKE state to ensure detection by the remote PHY receiver. This timer is measured as the amount of time between entry and exit from the WAKE state. The lpi_wakemz_timer defines the time a PHY requires to achieve compliant operation following activation. This timer is measured as the amount of time between entry into the WAKE_SILENT state, when the DUT is silent, and the beginning of training (IDLE) signaling, signifying entry into WAKE_TRAINING. Lpi_update_timer and lpi_postupdate_timer are described in Test 40.1.1.

Test Setup: See Appendix 40.A

Test Procedure:

Part a) Master mode

1. Establish a 1000BASE-T EEE link with the DUT forced into master mode.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.
4. Capture REFRESH waveform.
5. Decode the waveform prior to the quiet state.
6. Measure T_r.
7. Repeat for multiple captures.

Part b) Slave mode

1. Establish a 1000BASE-T EEE link with the DUT forced into slave mode.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.
4. Capture REFRESH waveform.
5. Decode the waveform prior to the quiet state.
6. Measure T_r.
7. Repeat for multiple captures.

Observable Results:

Part a) Master mode

a. T_r should be greater than 248.5μs and less than 269.7μs.
b. See Table 40.1.3 for additional refresh timing parameters

Part b) Slave mode

a. T_r should be greater than 198.5μs and less than 219.7μs.
b. See Table 40.1.3 for additional refresh timing parameters.

Table 40.1.3			
Timers		**Minimum value (μs)**	**Maximum value (μs)**
lpi_waketx_timer		1.2	1.4
lpi_wakemz_timer		4.25	5.0
lpi_wake_timer		N/A	16.5
lpi_update_timer	**Case 1: Master**	230	250
	Case 2: Slave	180	200
lpi_postupdate_timer		2.0	3.2

Possible Problems: The DUT may prematurely exit the refresh state if there are frames being sent. In these circumstances, the measured refresh time may not reflect the value of T_r and should not be included as part of the measurement.

Test 40.1.4 – Transmit wake time

Purpose: To verify that the amount of time the DUT transmits the wake signal is within the conformance limits.

References:

[1] IEEE std 802.3az-2010™, subclause 78.2 – LPI mode timing parameters description
[2] Ibid., table 78-4 – Summary of LPI timing parameters
[3] Ibid., figure 78-4 – LPI mode timing parameters and their relationship to minimum system wake time

Resource Requirements: See Appendix 40.A

Last Modification: December 10, 2010

Discussion:

Reference [1] specifies the time, T_{phy_wake}, that the DUT transmits the WAKE signal after exiting LPI and before resuming normal data transmission. Here WAKE is signified by 1000BASE-T IDLE, and can be measured explicitly as the duration of transmitted IDLE between the last QUIET period and the first data frame. Reference [2] defines a minimum system readiness time, $T_{w\_sys\_tx}$, that indicates the amount of time the DUT should transmit the WAKE signal. Reference [3] defines the $T_{w\_sys\_tx}$ (repeated in eq. 40.1.4 below for convenience) from the GMII, and incorporates a $T_{phy\_shrink\_tx}$ value. Since this test observes the signal at the MDI, $T_{phy\_shrink\_tx}$ is zero, and hence $T_{w\_sys\_tx}$ should be equal to $T_{w\_sys\_rx}$(min)+$T_{phy\_shrink\_rx}$(max).

$$T_{w\_sys\_tx}(\text{min}) = T_{w\_sys\_rx}(\text{min}) + T_{phy\_shrink\_tx}(\text{max}) + T_{phy\_shrink\_rx}(\text{max}) \qquad \text{(eq. 40.1.4)}$$

Test Setup: See Appendix 40.A

Test Procedure:

Part a) Master mode

1. Establish a 1000BASE-T EEE link with the DUT forced into master mode.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.
4. Cause the DUT to send a frame.
5. Measure the amount of time the DUT transmits IDLE signaling prior to the frame.
6. Repeat multiple times, and record the results.

Part b) Slave mode

1. Establish a 1000BASE-T EEE link with the DUT forced into slave mode.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.
4. Cause the DUT to send a frame.
5. Measure the amount of time the DUT transmits IDLE signaling prior to the frame.
6. Repeat multiple times, and record the results.

Observable Results:

Part a) Master mode

a. T_{phy_wake}, the amount of time the DUT should transmit IDLE before a frame, should be greater than 11.5μs.

Part b) Slave mode

a. T_{phy_wake}, the amount of time the DUT should transmit IDLE before a frame, should be greater than 4.26μs.

Possible Problems: None

Test 40.1.5 – Wake state levels

Purpose: To verify that the WAKE state Idle pattern exceeds 65% of the transmit levels of compliant Idle signaling for a minimum of 500 ns.

References:

[1] IEEE Std 802.3az-2010TM, subclause 40.6.1.2.7 – Transmitter operation following a transition from the QUIET to the WAKE state
[2] Ibid., subclause 40.4.5.2 – Timers
[3] Ibid, figure 40-15b – PHY Control state diagram, part b

Resource Requirements: See Appendix 40.A

Last Modification: December 10, 2010

Discussion:

Reference [3] specifies that at the beginning of the WAKE state the PHY transmits Idle symbols for duration lpi_waketx_timer, specified in Reference [2]. This signal is referred to as the “wake transient” and allows the local device to turn circuitry back on, and the remote device to detect a wake event and begin turning circuitry back on. Reference [1] states that while the device is transmitting Idle at the beginning of WAKE the transmit levels shall exceed 65% of compliant Idle symbol levels for at least 500ns.

As the IDLE signal for 1000BASE-T is {+2, 0, -2}, the minimum compliant IDLE signal level can be represented as the minimum limit for point A in the Test Mode 1 waveform. Reference [4] states that the minimum limit for point A is 670mV, and in this case the wake transient signal must exceed 65% of 670mV, or 435.5mV, for a duration of no less than 500ns. The effects of the passive line tap must be removed for this measurement.

Test Setup: See Appendix 40.A

Test Procedure:

1. Establish a 1000BASE-T EEE link.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.
4. Capture the REFRESH signal and isolate the wake transient portion.
5. Record the time the voltage levels exceed 65% of the transmit levels of a compliant Idle signal.
6. Repeat for multiple captures.

Observable Results:

a. The value of WAKE state Idle should exceed 435.5mV for a minimum of 500 ns.

Possible Problems: None

Test 40.1.6 – Transmitter Timing Jitter

Purpose: To measure the peak-to-peak transmit jitter present on a 1000BASE-T EEE-capable device while operating in low power idle mode.

References:

[1] IEEE Std 802.3az-2010™, subclause 40.2.4 – PHY Control function
[2] Ibid., subclause 40.6.1.2.5 – Transmitter timing jitter
[3] Ibid., figure 40-15b – PHY Control state diagram, part b
[4] UNH-IOL 1000BASE-T PMA Test Suite, Test #40.1.5 – Transmitter Timing Jitter, Full Test (Exposed TX_TCLK)

Resource Requirements: See Appendix 40.A

Last Modification: December 10, 2010

Discussion:

Reference [1] specifies PHY control for 1000BASE-T Energy Efficient Ethernet PHYs, and reference [2] defines the jitter specifications for 1000BASE-T, including EEE. The state diagram used by EEE-capable 1000BASE-T PHYs can be found in reference [3].

Reference [2] states that when the PHY supports the optional EEE capability, the unfiltered jitter requirements shall also be satisfied during the LPI mode, with the exception that clock edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states are not considered in the measurement. It is possible that the PHY may turn off the TX_TCLK during these states, to conserve additional power. For a Master PHY operating in the LPI mode, the unjittered reference shall be continuous.

Reference [4] outlines a testing methodology for measuring jitter in 1000BASE-T devices. The testing procedure outlined here differs only that the measurements are to be made while the device is operating in low power idle mode. For devices with TX_TCLK access, a measurement is made in MASTER mode as well as SLAVE mode, using the TX_TCLK signal and the measurement methodology described in reference [4].

When no access to the TX_TCLK is provided, an alternate method must be employed, which measures the jitter present on the LPI signaling itself to make the measurement. As this signal is scrambled PAM-5 IDLE, a symbol timing recovery algorithm which recovers a clock must be employed. This alternate method is currently under research and details surrounding this algorithm and its' implementation can be found in appendix 40.C.

Test Setup: See Appendix 40.A

Test Procedure:

Case 1.) TX_TCLK access is provided

1. Connect the TX_TCLK to the DSO.
2. Establish a 1000BASE-T EEE link with the DUT forced into master mode.
3. Force DUT to request low power idle mode.
4. Force test station to request low power idle mode.
5. Capture the TX_TCLK waveform, ensuring to remove any edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states from the measurement.
6. Measure the jitter on the TX_TCLK
7. Repeat until 100ms of edge data has been acquired and record the peak-to-peak jitter
8. Repeat steps 1-7 with the DUT configured for SLAVE mode.

Case 2.) No TX_TCLK access is provided

1. Establish a 1000BASE-T EEE link with the DUT forced into master mode.
2. Force DUT to request low power idle mode.
3. Force test station to request low power idle mode.

4. Capture a refresh cycle using the test setup shown in figure 40.A-1.
5. Recover the clock from the refresh period signaling, ensuring to remove any edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states from the measurement
6. Measure the jitter on the recovered clock.
7. Repeat until 100ms of edge data has been acquired and record the peak-to-peak jitter
8. Repeat steps 1-7 with the DUT configured for SLAVE mode.

Observable Results:

a. The unfiltered peak-to-peak transmit jitter shall be less than 1.4ns.

Possible Problems: None

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Appendix 40.A – 1000Base-T EEE Transmitter Test Setup

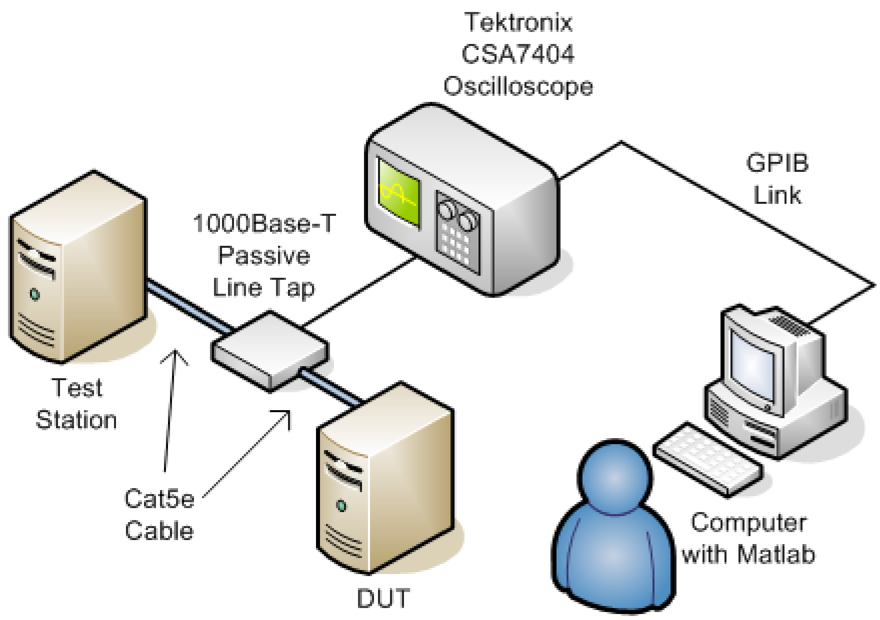
Purpose: To provide description of the test setup used to perform transmitter characterization

Resource Requirements:

- Digital storage oscilloscope, Tektronix CSA7404 or equivalent
- UNH-IOL passive line tap, or equivalent bi-directional tap
- 50 Ω SMA cables, matched length
- 50 Ω line terminations

Discussion:

The transmitter test setup can be seen in figure 40.A-1 below. Using two short cat5e UTP cables the DUT and the test station are linked through the passive line tap. Matched length SMA cables connect the line tap to a Tektronix DSO (CSA7404 or equivalent) which monitors the link as LPI operation begins. For more information on the passive line tap see Appendix 40.B.



Appendix 40.B – 1000Base-T Passive Line Tap

Purpose: To provide a description of the passive line tap used in 1000Base-T EEE PMA testing

Discussion:

The UNH-IOL developed a passive line tap which employs directional couplers and baluns to separate bi-directional traffic being transferred over a single wire. Using such a non-invasive device allows for the measurement of LPI signaling with minimal distortion to either EEE enabled devices' signal. A block diagram of the passive line tap is found below in Figure 40.B-1.

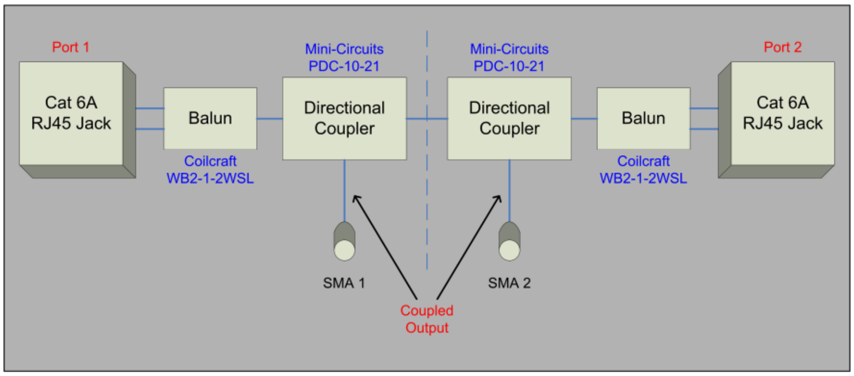


Figure 40.B-1: Passive Line Tap Block Diagram

Appendix 40.C – Transmitter Timing Jitter (EEE-mode, no TX_TCLK access)

Purpose: To provide a description of the clock recovery methodology used to perform jitter testing for 1000BASE-T EEE devices when no TX_TCLK access is provided.

Discussion:

This appendix is currently undergoing development.