POWER OVER ETHERNET

Power Sourcing Equipment
Parametric Test Suite
Version 2.11

Technical Document

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MODIFICATION RECORD

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March 3, 2003	-Version 1.1 Veena Venugopal
April 16, 2003	-Version 1.2 Veena Venugopal
July 23, 2003	-Version 1.3 Veena Venugopal
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June 27, 2007	-Version 2.3 David Schwarzenberg
July 2, 2008	-Version 2.4 Gerard Nadeau, David Schwarzenberg, Zachary Clifton
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INTRODUCTION

Overview
The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers identify problems related to the functional and electrical characteristics of the Power Sourcing Equipment defined in the IEEE Std 802.3™-2012 standard.

Note: Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other compliant devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in most IEEE Std 802.3™-2012 **environments.**

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment. However the different groups typically tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose
The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References
This section specifies source material *external* to the test suite, including specific sub-clauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements
The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification
This specifies the date of the last modification to this test. The Last Modification date is not necessarily updated for typographical, or reference update modifications, but is intended to indicate more substantive changes.

Discussion
The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup
The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure
The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results
The observable results section lists specific items that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable result, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable result.

Possible Problems
This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

Group 1: Detection Characteristics

Scope: This group of tests verifies the electrical and functional characteristics during the detection mode of Power Sourcing Equipment.

Overview: These tests are designed to identify problems with IEEE Std 802.3™-2012 Clause 33 compliant devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment's detection sequence.

33.1.1: Valid PSE Pinout

Purpose: To verify that pinout of the Power Sourcing Equipment is valid.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.1, Figures 33–4, 33–5, 33–6, 33–7, Table 33–2.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE1, PSE2

Resource Requirements:
- Oscilloscope

Last Modification: December 11, 2009

Discussion: A PSE can be located with or on a link segment that is separate from the DTE/Repeater; these two locations are known as Endpoint PSE and Midspan PSE respectively. Regardless of the PSE location, detection and power can be applied with either Alternative A or Alternative B pinouts. These pinouts are defined in the Table 33–2, reprinted below.

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{Port}	Positive V_{Port}	
2	Negative V_{Port}	Positive V_{Port}	
3	Positive V_{Port}	Negative V_{Port}	
4			Positive V_{Port}
5			Positive V_{Port}
6	Positive V_{Port}	Negative V_{Port}	
7			Negative V_{Port}
8			Negative V_{Port}

Table 33–2 – PSE pinout alternatives

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Determine the Location of the PSE, Endpoint or Midspan.
2. Connect the PD simulator using Alternative A
3. Attempt to power the PD simulator.
4. Switch Alternative and repeat steps 1–2.

Observable Results:
- The DUT should implement the correct pinout given its location on the link segment.

Possible Problems: None

33.1.2: Open Circuit Voltage

Purpose: To verify that the open circuit voltage at the PI of the PSE during detection mode is below the conformance limit.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5.1 and Table 33–4.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE13

Resource Requirements:
- Oscilloscope

Last Modification: December 11, 2009

Discussion: During the detection mode, the open circuit voltage (V_{oc}) of the PSE should not exceed 30V.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Measure the open circuit voltage at the PI of the DUT using a high impedance probe.

Observable Results:
- V_{oc} (the open circuit voltage) should not exceed 30 Volts.

Possible Problems: None

33.1.3: Detection Circuit

Purpose: To verify the Thevenin equivalent detection circuit of the PSE detection source.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5.1, Figures 33–11, 33–12
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE17

Resource Requirements:
- 45kΩ test load
- Current Source
- Current Meter
- Oscilloscope

Last Modification: July 21, 2015

Discussion: The PSE should detect the PD by probing via the PSE PI. The PSE's detection circuit can have a Thevenin equivalent circuit consistent with Figure 33–11 or 33–12, in all detection states. This is intended to prevent a PSE to PSE connection from detecting a valid PD signature.

Test Setup: The PSE is connected to the PD simulator with a 1m length of Category 5 cable. A current source and current meter is connected to the PI of the PD simulator.

PSE Detection Source (Figure 33–12): The PSE is connected to the PD simulator with a 1m length of Category 5 cable. An oscilloscope is connected across the PI of the PD simulator. A 45kΩ load is attached to the PD's PI.

Alternative PSE Detection Source (Figure 33–13): The PSE is connected to the PD simulator with a 1m length of Category 5 cable. A current meter is connected to the PI of the PD simulator. A current source is connected to the PI of the PD simulator to inject current to the V_{PSE+} port.

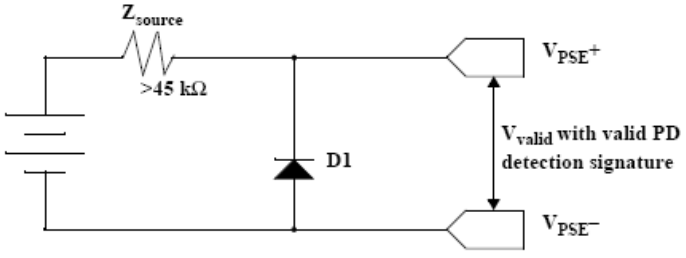

Figure 33–11—PSE detection source

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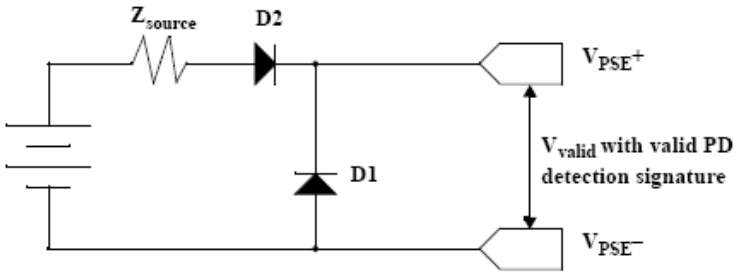

Figure 33–12—Alternative PSE detection source

Procedure:

1. Connect the current source to the PI
2. Measure the current flowing into the V_{PSE+} port of the PSE
3. If current was not accepted in step 2, measure the maximum output voltage of the open circuit PI. Otherwise, the test is complete.
4. Disconnect the current source
5. Connect the 45kΩ test load to the PI
6. Measure the maximum output voltage of the loaded PI

Observable Results:

- If the DUT does not accept current into the V_{PSE+} port, the DUT follows Figure 33–12.
- Otherwise, the DUT should accept current into the V_{PSE+} port and the DUT should show a loaded PI voltage of less than half of the open circuit PI voltage, according to Figure 33–11.

Possible Problems: None

33.1.4: Backdriven Current

Purpose: To verify the detection circuit of the PSE can withstand maximum backdriven current over the range of V_{OC}.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5.1
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE14

Resource Requirements:
- PD Simulator
- Current Source

Last Modification: July 21, 2015

Discussion: The PSE must be able to handle a PSE to PSE connection. The standard specifies this as the DUT receiving a backdriven current of 5mA over the range of V_{OC}. After the maximum backdriven current has been applied, the DUT should still be capable of detecting an attached PD.

Test Setup: The PSE is connected to the PD simulator with a 1m length of Category 5 cable. A current meter is connected to the PI of the PD simulator.

Procedure:
1. Using the 5mA source, inject a current into the PSEs V_{PSE+} port for 10 seconds.
2. Disconnect the current source from the PSE and attach a valid PD signature
3. Observe if the PSE correctly detects the PD and supplies power
4. Disconnect the valid PD
5. Re-connect the current source and inject current into the PSEs V_{PSE-}.
6. Disconnect the current source
7. Re-connect the PSE to a valid PD
8. Observe if the PSE correctly detects the PD and supplies power

Observable Results:
- The DUT should not be affected by the backdriven current.

Possible Problems: None.

33.1.5: Detector Circuit Output Current

Purpose: To verify that the short circuit output current of the PSE during PD detection is within the conformance limits.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5.1, Table 33–4
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE13

Resource Requirements:
- PD Simulator
- Oscilloscope
- Current meter

Last Modification: December 11, 2009

Discussion: The PSE should limit its output current during detection such that in the event of a short circuit condition, the PSE will not be damaged. The output current for the PSE detection circuit should not exceed 5mA. This value assures the PSE and any attached media will not be damaged.

Test Setup: The DUT is connected to the PD simulator, configured as a short circuit.

Procedure:
1. Using the current probe, measure the short circuit current at the PI.
2. Repeat step 1 for all probe voltages sourced by the DUT.

Observable Results:
- I_{SC} (short circuit output current) should not exceed 5 mA.

Possible Problems: None

33.1.6: Detector Circuit Output Voltage

Purpose: To verify that the test voltages of the PSE detection circuit conform to the specifications defined in Table 33–4.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5.2, Table 33–4
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE17, PSE18, PSE19

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: While the PSE is probing the link segment for a valid PD detection signature, the detection voltage V_{detect} at the PSE PI should be within the V_{valid} voltage range of 2.8 to 10 Volts. The loaded circuit values are measured with a valid PD signature attached to the PSE. The PSE should make at least 2 measurements with V_{detect} values that create at least a ΔV_{test} difference of 1 Volt.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI. Confirm that the DUT is operating in PD detection mode and transmitting probe voltages.

Procedure:
1. Supply a valid signature using the PD simulator board at the PI of the DUT
2. Measure the probe voltages at the PI of the DUT.
3. Measure the slew rate of the probe voltages.

Observable Results:
- In step 2, V_{VALID} (the loaded PI output detection voltages) should be between 2.8 and 10 volts.
- In step 2, ΔV_{TEST} should be at least 1 volt.
- In step 3, V_{SLEW} (the slew rate of the probe voltages) should be less than 0.1 V/µs

Possible Problems: None

33.1.7: PD Detection Timing

Purpose: To verify that the PSE probes its PI with valid detection pulses and completes an entire detection sequence within the proper time period.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5.1, Table 33–4, Table 33–11.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE4

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: While the PSE is probing the link segment for a valid PD detection signature, the PSE is required to make at least 2 measurements within V_{detect} values. During these measurements, the time between any two valid test points should be at least 2ms (T_{BP}), while the total time taken for the PSE to complete detection should not be greater than 500ms (T_{det}).

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI. Confirm that the DUT is in PD detection mode and transmitting probe voltages.

Procedure:
1. Measure the pulse width of the entire detection sequence.
2. Measure the time between any two valid detection voltages.

Observable Results:
- In step 1, T_{DET} should not be greater than 500ms.
- In step 2, T_{BP} should be at least 2 ms.

Possible Problems: None

33.1.8: PD Signature Detection Limits

Purpose: To verify that the DUT will properly detect a PD's signature impedance.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5.3; Subclause 33.2.5.4; Table 33–5, Table 33-6.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE29, PSE20

Resource Requirements:
- PD Simulator
- Voltmeter

Last Modification: December 11, 2009

Discussion: The PSE should detect a valid signature for a link segment that has the characteristics of R_{good} and C_{good} between the powering pairs. The PSE should detect an invalid signature for a link segment that has the characteristics of R_{bad} and C_{bad} between the powering pairs. The PSE should only provide power if the PD presents a valid signature which is compliant with Table 33–5 and Table 33-6 which are synthesized here for convenience.

Item	Parameter	Minimum	Maximum
7	R_{good} (KΩ)	19.0	26.5
8	R_{bad} (KΩ)	15.0	33
10	C_{good} (nF)		150
11	C_{bad} (µF)	10.0	

Table 33–5 and 33–6

Test Setup: The DUT is connected to the PD Simulator with a 1m length of Category 5 cable.

Procedure:
Part a: Input Resistance Minimums
1. Adjust the PD simulator to have a valid input signature capacitance (0.1µF)
2. Increase the signature resistance from R_{bad}min until the DUT supplies power to the PD
3. Record the value at which the PSE accepts the PD signature resistance.
4. Decrease the signature resistance below R_{good}min until the DUT does not supply power to the PD
5. Record the value at which the PSE rejects the PD signature resistance.

Part b: Input Resistance Maximums
6. Increase the signature resistance above R_{good}max until the DUT does not supply power to the PD
7. Record the value at which the PSE rejects the PD signature resistance.
8. Decrease the signature resistance from R_{bad}max until the DUT supplies power to the PD.
9. Record the value at which the PSE accepts the PD signature resistance.

Part c: Input Capacitance "Must Accept"

10. Set the PD signature model to have a resistance between R_{good}min and R_{good}max (25kΩ).
11. Set the PD signature model to have a capacitance of C_{sig}max less than 150nF
12. Connect the PD signature model to the PI of the DUT and observe the voltage at the PI.

Part d: Input Capacitance "Must Reject"

13. Set the PD signature model to have a capacitance of greater than C_{bad}min (10 µF)
14. Connect the PD signature model to the PI of the DUT and observe the voltage at the PI.

Observable Results:

- In step 3 and 5, $R_{accept(min)}$ should be between 15kΩ and 19kΩ
- In step 7 and 9, $R_{accept(max)}$ should be between 26.5kΩ and 33kΩ
- In step 12, the DUT should accept the PD signature and should provide power
- In step 14, the DUT should reject the PD signature and should not provide power

Possible Problems: None.

33.1.9: Physical Layer Classification

Purpose: To verify a PSE supporting classification properly performs PD classification detection.

Reference:
[1] IEEE Std 802.3™-2012: Subclause 33.2.6.1, Table 33–7, Table 33–9.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE25, PSE26, PSE27, PSE28, PSE29, PSE31

Resource Requirements:
- PD simulator
- Oscilloscope

Last Modification: April 22, 2011

Discussion: The PSE may attempt to classify the PD. Also, the PD may provide information to allow features such as load management to be implemented. For a PSE that performs 1-event classification, the PSE should probe the PD with a voltage between 15.5 and 20.5 volts limited to 100mA. A PSE that performs 2-event classification must present two class events in the 15.5 to 20.5 Volt range separated by a mark event of 7 to 10 Volts. The class events are limited to 100mA, and the mark event is limited to the range of 5mA to 100mA. The PSE should measure I_{Class} and classify the PD based on the observed current as dictated by Table 33–9, which is printed here for convenience.

Measure I_{class}	Classification
0mA to 5.00mA	Class 0
>5.00mA and <8.00ma	May be Class 0 or 1
8.00mA to 13.0mA	Class1
>13.0mA and <16.0mA	May be Class 0,1 or 2
16.0mA to 21.0mA	Class 2
>21.0mA and <25.0mA	May be Class 0,2 or 3
25.0mA to 31.0mA	Class 3
>31.0mA and <35.0mA	May be Class 0,3 or 4
35.0mA to 45.0mA	Class 4
>45.0mA and <51.0mA	May be Class 0 or 4

Table 33–9

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Configure the PD simulator to draw Class 0 currents.
2. Measure classification sequence voltages using an oscilloscope.
3. Determine the observed classification level through the management of the DUT

4. Repeat steps 1-3 for Class 0 through Class 4
5. Configure the PD simulator to draw 150mA Class current.
6. Measure the $I_{CLASS-LIM.}$
7. Determine the observed classification level through the management of the DUT

Observable Results:

- In step 2, there should be one class pulse, $V_{CLASS,}$ which should be between 15.5 and 20.5 Volts.
- In step2, for class 4 current draws a 2-Event classification DUT, should provide two class pulses of V_{CLASS} between 15.5 and 20.5 Volts. They should be separated by V_{Mark}, which should be between 7 and 10 volts.
- In step 3, the DUT should accurately classify the PD.
- In step 7, if the current drawn is equal to or greater than 51mA, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2 PSE shall return to the IDLE state.
- In step 6, I_{CLASS_LIM} should be between 51 and 100mA for both Type 1 and Type 2 PSEs. I_{MARK_LIM} should be between 5 and 100mA for all mark events.

Possible Problems: If the DUT does not perform classification, then the DUT should assign the PD to Class 0.

33.1.10: Physical Layer Classification Timing

Purpose: To verify that a PSE capable of classifying a PD performs classifications within the specified timing constraints.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.6.1, Table 33–10
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE4, PSE30, PSE32

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 9, 2014

Discussion: After successful detection of a PD, a PSE supporting 1-event classification must complete classification within 6 to 75ms (T_{pdc}). For a PSE that supports 2-event classification, each of the two class events (T_{CLE1} and T_{CLE2}) should complete within 6 to 30ms. Following the first class event, the first mark event (T_{ME1}) should complete within 6 to 12ms. Following the second class event, a second mark event (T_{ME2}) occurs that must endure for a period exceeding 6ms. Classification should complete within 400 ms after completion of detection (T_{pon}). If the PSE fails to power the PD within T_{pon}, it must reinitiate detection prior to power up.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Measure the length of the classification pulses.

Observable Results:
- For 1-event classification the T_{PDC} should be between 6 and 75ms.
- For 2-event classification T_{CLE1} and T_{CLE2} should be between 6 and 30ms.
- For 2-event classification, T_{ME1} should be between 6 and 12ms
- For 2-event classification, T_{ME2} should be greater than 6ms.

Possible Problems: This test does not apply to a DUT that does not perform PD classification.

33.1.11: Allowed Classification Permutations

Purpose: To verify whether the PSE fits a valid classification permutation.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.6, Table 33–8
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE21

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: August 9, 2013

Discussion: A PSE shall meet one of the allowable classification permutations in Table 33–8.

Permutations			PSE allowed?	PD allowed?
PSE/PD Type	Physical Layer classification	Data Link Layer classification		
Type 2	2-Event	No	Yes	No
		Yes	Yes	Yes
	1-Event	No	No	No
		Yes	Yes	No
	None	No	No	No
		Yes	No	No
Type 1	2-Event	No	No	Yes
		Yes	No	Yes
	1-Event	No	Yes	Yes
		Yes	Yes	Yes
	None	No	Yes	No
		Yes	Yes	No

Table 33-8

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Based on the classification voltage waveform determine whether the PSE is using a 1-Event or a 2-Event Physical Layer classification.
2. Monitor Network Activity for several minutes to determine whether the DUT is utilizing Data Link Layer classification.
3. If Data Link Layer Classification is observed, request maximum power with Data Link Layer Classification
4. Determine the PSE Type by observing the maximum power available at the PI

Observable Results:

- The DUT should be an allowable type as specified by table 33-8

Possible Problems: None.

33.1.12: New Detection Cycle

Purpose: To verify that if the PSE is unable to supply power within T_{pon} then, it initiates and successfully completes a new detection cycle before powering on.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.4.1, Table 33–11.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE4, PSE19

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: The PSE may apply power after a valid sequence of detection and optional classification. However if the PSE is unable to supply power within a time interval of 400ms (tpon_timer), then it must initiate a new valid detection cycle before applying power. The 'tpon_timer' timer is used to limit the time for power turn-on, which is referred to as T_{pon} in Table 33–11.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Supply a valid signature at the DUT's PI for a time approximately lesser than the T_{pon} of the DUT. (Refer to Test # 33.1.7 for the value of turn on time for the DUT.)
2. Connect an invalid signature at the DUT's PI for at least 2sec.
3. Reconnect the valid signature at the DUT's PI.
4. Observe the waveform on the oscilloscope.
5. Measure the detection time.
6. Measure T_{pon}.

Observable Results:
- The DUT should complete a full detection cycle before applying power to the PD simulator.

Possible Problems: None

33.1.13: Alternative B Backoff Cycle

Purpose: To verify that if a PSE that implements Alternative B fails to detect a valid detection signature at its PI, it will back off for no less than T_{dbo} and apply a voltage V_{off} less than 2.8VDC during the backoff.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.4.1, Table 33–11.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE5

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: A PSE that implements Alternative B will start the 'tdbo_timer' if it fails to detect a valid signature at its PI. The 'tdbo_timer' is used to regulate backoff upon detection of an invalid signature as is referred to as T_{dbo} in Table 33–11. During this backoff period, the PSE must not apply a voltage V_{off} greater than 2.8Vdc to the PI. A PSE that implements Alternative B detection must not resume detection mode until at least one backoff cycle has elapsed.

Test Setup: The PSE is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Connect an invalid signature at the DUT's PI.
2. Measure the DC voltage between the consecutive valid detection sequences.
3. Measure the time between consecutive valid detection sequences.

Observable Results:
- In step 2, the DUT must not apply a voltage V_{off} greater than 2.8 Vdc at its PI.
- In step 3, $T_{dbo} > 2$ sec.

Possible Problems: This test does not apply to a PSE that implements Alternative A.

Group 2: Power Feed Characteristics

Scope: This group of tests verifies the electrical and functional characteristics during of the Power Sourcing Equipment while feeding power.

Overview: These tests are designed to identify problems with IEEE DraftP802.3at™/D3.3 Clause 33 compliant devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment.

33.2.1: Power Feed Ripple and Noise

Purpose: To verify the power feeding ripple and noise are within the conformance limits.

References:
[1] IEEE Std 802.3at™-2009: Subclause 33.2.7.3, Table 33–11
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE52

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: The PSE should source power at all rated levels with noise and ripple that are below the levels specified in Table 33–11 (printed here for convenience). Excessive noise may cause attached PDs to behave abnormally.

Parameter	Min	Max
Power feeding Ripple and noise (Vpp)		
f < 500Hz		0.50
500Hz ≤ f < 150KHz		0.20
150KHz ≤ f < 500KHz		0.15
500KHz ≤ f <1 MHz		0.10

Table 33–11

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Adjust the PD to sink .44 watts.
2. Measure the amount of pair-to-pair ripple and noise voltage at the PI of the PSE.
3. Measure the amount of common-mode ripple and noise voltage at the PI of the PSE.
4. Adjust the PD to sink maximum allowable power.
5. Repeat steps 3 and 4.

Observable Results:
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 0-500Hz will be less than 0.50 volts
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 500Hz-150kHz will be less than 0.20 volts
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 150kHz-500kHz will be less than 0.15 volts
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 500kHz-1MHz will be less than 0.10 volts

33.2.2: Load Regulation

Purpose: To verify that the PSE performs load regulation while supplying power on its PI.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.1, Table 33–11
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE48

Resource Requirements:
- PD Simulator
- Oscilloscope
- DC Electric Load

Last Modification: August 12, 2013

Discussion: The PSE should perform voltage regulation while supplying power to a PD over the PI. The output voltage of the PSE must stay between 44 and 57 volts for a Type 1 device or 50 to 57 volts for a Type 2 device while the load changes at a rate of 15 to 35mA/µs. The PSE must not produce any transients greater than 3.5V/µs. These requirements prevent the voltage supply from exceeding the operating range of a PD.

Test Setup: Connect the DUT to the PD Simulator with a 1m length of Category 5 cable. Connect the multimeter to the PI of the PD simulator to measure voltage and current.

Procedure:
1. Connect the PSE to the PD simulator with a valid signature and the load set to draw 10mA.
2. For a Type 1 device, rapidly adjust the current draw of the PD from 10mA to 350mA. This transition needs to occur within 340 / 35 µs (approximately 9.7 µs) to 340 / 15 µs (approximately 22.7µs).
   For a type 2 device, rapidly adjust the current draw of the PD from 10mA to 600mA. This transition needs to occur within 590 / 35 µs (approximately 16.9 µs) to 590 / 15 µs (approximately 39.3µs)
3. Observe the voltage transients and output voltage of the PSE at the PI.

Observable Results:
- In step 3, the voltage transients seen should not exceed 3.5V/µs.
- In step 3, the DUT output voltage at the PI should be within the range of 44 to 57 volts for a Type 1 device or 50 to 57 volts for a Type 2 device.

Possible Problems: None.

33.2.3: Voltage Transients

Purpose: To verify that the Type 2 PSE maintains proper output voltages for transient conditions.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.2, Table 33–49
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE57, PSE58, PSE59

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: July 29, 2013

Discussion: The Type 2 PSE must maintain an output voltage that varies by less than K_{trans_lo} below V_{port}min for transient conditions lasting between 30 to 250μs. Transients lasting more than 250μs should meet the static V_{port} specification.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Confirm that the detection of the PD has been successfully completed.
2. Apply transients between 30 and 250μs and measure V_{port}.
3. Apply transients above 250μs and measure V_{port}.

Observable results:
- For a Type-2 PSE, V_{PORT} should not go below 46.2 Volts for any transient between 30 and 250μs. V_{PORT} should not go below 50V for any transient lasting more than 250μs

Possible Problems: This test only applies to Type 2 PSEs. A Type 2 PSE may remove power from the PI if V_{port} is below 50V.

33.2.4: Power Turn On Timing

Purpose: To verify that the PSE starts applying power within T_{pon} after it has successfully detected the PD.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.12, Table 33–11
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE4, PSE9

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: The PSE must power on the PD after detection within T_{pon}. If the PSE fails to power the PD within 400ms (T_{pon}), it must reinitiate the detection sequence.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Confirm that the detection of the PD has been successfully completed.
2. Measure the time delay between the end of detection and when the PSE starts applying power.

Observable results:
- In step 2, T_{pon} should not be greater than 400ms.

Possible Problems: None.

33.2.5: Apply Power

Purpose: To verify that the PSE applies power on the same pairs as those used for detection after completing a valid detection.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.5, Table 33-11
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE9, PSE10

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: A PSE detects the PD by probing it via the PSE's PI. A PSE should apply power only after it has completed the detection of a PD. The power should be supplied on the same pairs as those used for detection.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Supply a valid signature at the DUT's PI for a time approximately equal to T_{det} of the DUT.
2. Confirm that the DUT performs valid detection sequence before powering the PD simulator.
3. Check the pairs on which DUT supplies power.

Observable Results:
- In step 2, the DUT must power the PD simulator only after a proper detection sequence.
- In step 3, the DUT should supply power on the same pairs as that it performed detection for the PD simulator.

Possible Problems: None

33.2.6: Current Unbalance

Purpose: To verify that the current unbalance between the two conductors of the power pairs of the PSE over the current load range is within the permissible range.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.11, Table 33–11.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE61

Resource Requirements:
- PD Simulator
- Oscilloscope
- Two Matching current probes
- DC Electronic Load

Last Modification: July 21, 2015

Discussion: A PSE supplies power via its PI to the PD using either Alternative A or Alternative B pinout. Ideally the current flowing on both the conductors per power pair should be the same, however due to practical limitations this is not possible. Thus, the current output unbalance between the two conductors per power pair should not exceed 3% of I_{cable} for a Type 1 PSE and 3% of I_{peak} for a Type 2 PSE.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. Attach the current probes to each wire of the TX pair and allow the DUT to power the PD simulator. Attach the DC Electronic load to the PD simulator.

Procedure:
1. Verify that the DUT is supplying power to the PD simulator.
2. Connect the DC Electronic load to the DUT.
3. Set the PD simulator to draw at least 10mA.
4. Measure the current on both the twisted pairs at the PI of the DUT.
5. Vary the load so that the PD simulator draws the maximum current that the DUT can supply.
6. Measure the current on both conductors per power pairs at the PI of the DUT.

Observable Results:
- In step 4 and step 6 for a Type 1 device, I_{UNB} should not be greater than 3% of I_{cable}.
- In step 4 and step 6 for a Type 2 device, I_{UNB} should not be greater than 3% of I_{peak}.

Possible Problems: None

Group 3: Error Detection and Power Removal

Scope: This group of tests verifies the electrical and functional characteristics during error detection and power removal.

Overview: These tests are designed to identify problems with IEEE Std 802.3™-2012Clause 33 compliant devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment.

33.3.1: Overload Current Detection Range

Purpose: To verify that I_{CUT} is within the specified limits.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.6, Table 33–11
Resource Requirements:

- PD Simulator
- Oscilloscope
- Current probe

Last Modification: December 11, 2009

Discussion: The PSE monitors the current (I_{Port}) drawn by the PD. If I_{Port} exceeds the overload current detection range I_{CUT} for greater than 75ms (T_{ovld}), the PSE should remove power from its PI. I_{CUT} has a minimum value of P_{Class}/V_{Port} and a Type 1 maximum of 400mA or a Type 2 maximum of $(400/350)*(P_{Port}/V_{Port})$. This is an optional specification.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the current probe. The current probe is connected to the PD simulator at the PI.

Procedure:

1. Verify that the PD is drawing current greater than or equal to I_{Min} from the DUT.
2. Measure the V_{Port} at the PI of the PSE.
3. Decrease the load resistance gradually until the DUT removes power from its PI.
4. Measure the current (I_{CUT}) at which the DUT stops supplying power

Observable Results:

- For Type 1 PSEs, I_{CUT} should be between P_{Class}/V_{Port} and 400mA
- For Type 2 PSEs, I_{CUT} should be between P_{Class}/V_{Port} and $(400/350)*(P_{Port}/V_{Port})$

Possible Problems: None

33.3.2: Overload Time Limit

Purpose: To verify that T_{cut} is within specified limits.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.7, Table 33–11, Figure 33-14

Resource Requirements:
- PD Simulator
- Oscilloscope
- Current probe

Last Modification: December 11, 2009

Discussion: The PSE monitors the current (I_{Port}) drawn by the PD. If I_{Port} exceeds the overload current detection range I_{CUT} for greater than T_{cut}, the PSE may remove power from its PI. This limit is optional.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Connect the PD to the DUT with the load set to maximum.
2. Vary the load until the $I_{Port} \geq I_{CUT}$.
3. Disconnect the load.
4. Make sure the PSE is powering, and connect the load.
5. Measure the resulting current waveform with the Oscilloscope.

Observable Results:
- In step 5, T_{cut} should be between 50ms and 75ms (inclusive).

Possible Problems: None

33.3.3: Output Current at Short Circuit Condition

Purpose: To verify that the output current at short circuit condition falls within the specified amplitude and timing.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.7, Table 33–1, Table 33-11, Figure 33-14
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE56, PSE57, PSE58

Resource Requirements:
- PD Simulator
- Oscilloscope
- Current probe

Last Modification: August 14, 2013

Discussion: The PSE monitors the current (I_{Port}) drawn by the PD at the PI. If I_{Port} meets or exceeds the "PSE lowerbound template", the PSE should remove power from its PI. The PSE should remove power before the current exceeds the "PSE upperbound template" in Figure 33-14 reprinted below for convenience.

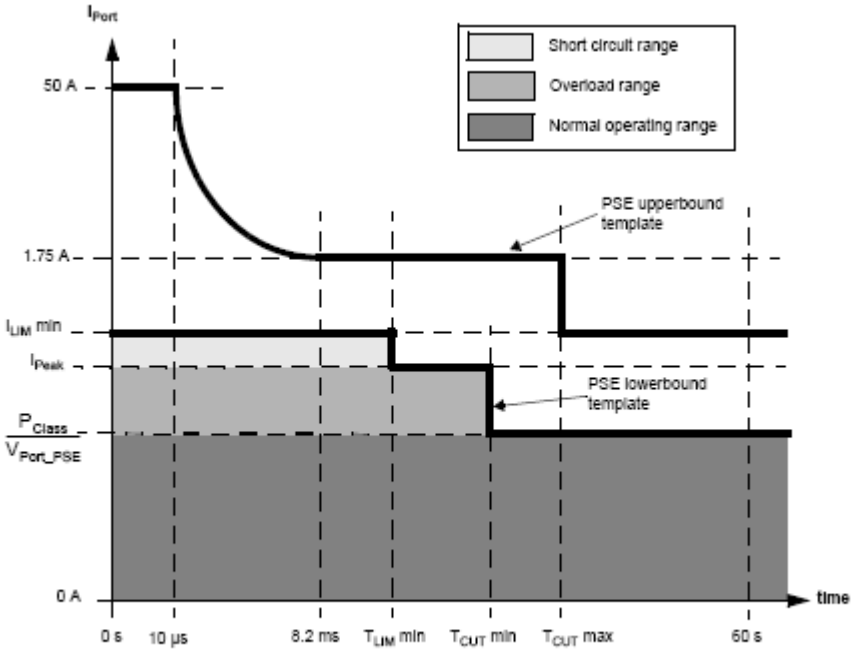

Figure 33–14—POWER_ON state PI operating current templates

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the current probe. The current probe is connected to the PD simulator at the PI.

Procedure:

1. Verify that the PSE is powered and outside of startup mode.
2. Apply a load that violates the "PSE upperbound template"
3. Measure the resulting current draw with the current probe.
4. Repeat steps 1-3 with different current draws that violate the PSE upperbound template
5. Confirm that the DUT does not remove power when below the PSE lowerbound template.

Observable Results:

- In step 3, the DUT should limit I_{PORT} when it exceeds the PSE upperbound template
- In step 5, the DUT should not remove power when below the PSE lowerbound template

Possible Problems: In step 2, it is possible that the PSE will limit the current draw at the PI, and thus drawing certain currents along the upperbound template may not be possible. The PSE may also remove power if the voltage at the PI decreases below a normal V_{port} range. This behavior is still conformant, but may also prohibit us from testing certain currents in the upperbound template.

33.3.4: Output Current in Startup Mode

Purpose: To verify that the inrush current during startup conforms to the specified values. Also, to ensure the PSE removes power within the conformant time limit when it detects a short circuit condition.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.5, Table 33–11, Figure 33-13
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE54, PSE55

Resource Requirements:
- PD Simulator
- Oscilloscope
- Current probe

Last Modification: August 14, 2013

Discussion: The standard defines the output current, I_{INRUSH}, in startup mode. Startup mode is defined as the transition to the POWER_UP state to the lesser of T_{INRUSH} or the conclusion of the PD inrush currents. During startup, for PI voltages above 30 V, the minimum I_{INRUSH} requirement is 400mA. For PI voltages between 10 V and 30 V, the minimum I_{INRUSH} requirement is 60 mA. For PI voltages between 0V and 10V, the I_{INRUSH} requirement is between 5mA and 450mA. The whole process is limited by $T_{INRUSH,}$ which is limited between 50 and 75 ms. Also, all of the measurements must be taken after 1ms to ignore startup transients. See Figure 33-13.

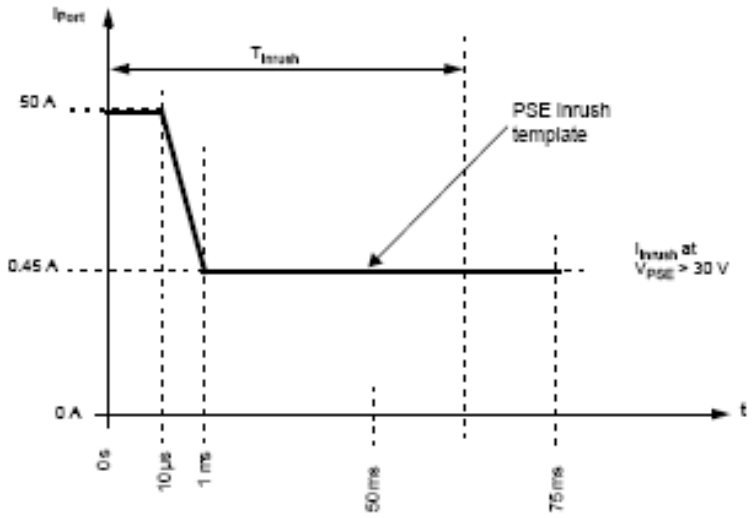

Figure 33–13—I_{Inrush} current and timing limits in POWER_UP state

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the current probe. The current probe is connected to the PD simulator at the PI.

Procedure:

1. Configure PD simulator to short when voltages are above 40 Volts.
2. Allow DUT to power up.
3. Measure resulting current waveform.
4. Repeat for 31V, 22V,9.9V and 7V.

Observable Results:

- In step 3 for voltages above 30V, I_{INRUSH} should be between 400mA and 450mA (inclusive).
- In step 3 for voltages between 10V and 30V, I_{INRUSH} should be between 60mA and 450mA (inclusive).
- In step 3 for voltages below 10V, I_{INRUSH} should be between 5mA and 450mA (inclusive).
- In step 3, all waveforms must be between 50ms and 75ms (inclusive)

Possible Problems: Shorting the DUT for voltages in the detection and classification range may cause improper detection and/or classification.

33.3.5: Error Delay Timing

Purpose: To verify that the PSE waits for at least the minimum conformant time before attempting subsequent detection after it removes power due to the detection of the error condition.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.4.5,Table 33–11, Figure 33–9.

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: August 13, 2013

Discussion: If the PSE detects an error condition during its normal operation when the PSE is supplying power to the PD, it must remove power from its PI. The error condition can be a short circuit or an overload condition. The PSE must wait for at least 750ms (T_{ed}) before it commences with valid detection sequence after power removal.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
Part a: Short circuit condition
1. Verify that the DUT is supplying power to the PD simulator.
2. Create a short circuit condition at the PD simulator for at least 75ms.
3. Measure the time duration from when the DUT removes power and when the DUT attempts subsequent detection.

Part b: Overload Condition:
4. Verify that the DUT is supplying power to the PD simulator.
5. Create an overload condition by increasing the current draw greater than 400mA for a Type 1 PSE or 684mA for a Type 2 PSE for greater than 75ms.
6. Measure the time duration from when the DUT removes power and when the DUT attempts subsequent detection.

Observable Results:
- In step 3, $T_{ed} \geq 750$ms.
- In step 6, $T_{ed} \geq 750$ms.

Possible Problems: None

33.3.6: Range of T_{MPDO} Timer

Purpose: To verify that the PSE correctly monitors the PD Maintain Power Signature.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.9.1.1, Subclause 33.2.9.1.2 Table 33–11, Figure 33–9, Figure 33–12.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE65, PSE68

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: Once a PSE has entered the 'POWER_ON' state, it must receive an 'mr_mps_valid' from the link partner within a specified amount of time. If this message is not received, it will enter the 'IDLE_MPS' state and remove power from the link segment before attempting a new detection sequence. This time is defined by the device's 'tmpdo_timer' and is required to be between 300ms and 400ms. This test is designed to verify that the device under test enters the 'IDLE_MPS' state from the 'POWER_ON' state when an mr_mps_valid message is not received from its link partner in the acceptable range of time.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
Part 1: DC disconnect
1. Attach a valid signature to the PI of the DUT such that the DUT enters the 'POWER_ON' state.
2. Reduce the current drawn by the PD to 2mA for $t \leq 300ms$.
3. Observe whether the DUT entered the 'IDLE_MPS' state.
4. Repeat steps 1–3 varying t until the DUT enters the 'IDLE_MPS' state.
5. Find the t for which the PSE removes power.

Part 2: AC disconnect
6. Attach a valid signature to the PI of the DUT such that the DUT enters the 'POWER ON' state.
7. Disconnect the PD from the PI of the DUT.
8. Measure the time taken by the DUT to remove power.

Observable Results:
Part 1:
- In step 5, verify that $300ms \leq T_{MPDO} \leq 400$ ms.

Part 2:
- In step 8, verify that 300 ms $\leq T_{MPDO} \leq 400$ ms.

Possible Problems: None.

33.3.7: PD MPS Dropout Current Limits (I_{Min} measurement)

Purpose: To verify that the PSE correctly monitors the PD Maintain Power Signature.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.9.1.2, Table 33–11
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE66, PSE69

Resource Requirements:
- PD Simulator
- Multimeter

Last Modification: December 11, 2009

Discussion: The PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD is disconnected. The PSE may monitor the AC MPS component, the DC MPS component, or both signature components. If the PSE monitors the DC MPS component, the DUT should remove power from the PI if the current drawn by the PD drops below 5mA ($I_{MIN1\ (max)}$) for more than 400 ms (T_{MPDO}). The PSE may remove power if the current drawn by the PD is between 5mA and 10mA($I_{MIN2\ (max)}$) for greater than 400ms(T_{MPDO}).

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The multimeter is connected to the PD simulator at the PI to measure current.

Procedure:
1. Set the PD Simulator to draw 10mA of current from the DUT
2. Decrease the current draw of the PD simulator from 10mA to less than 5mA for 400ms, in steps of 0.1mA.
3. Observe the output voltage at the PI of the DUT during each step.
4. Record the current draw at which the PSE removes power.

Observable Results:
- In Step 4, if the current drawn by the PD simulator is between 5mA and 10mA, the DUT may disconnect power from the PI.
- In Step 4, if the current drawn by the PD simulator is less than 5mA, the DUT must disconnect power from the PI.

Possible Problems: This test does not apply if the DUT performs only AC disconnect.

33.3.8: PD MPS Time for Validity

Purpose: To verify that the PSE waits for at least the minimum MPS validity time when it monitors the DC MPS component.

References:
[1] IEEE Std 802.3™-2012: Subclause33.2.9, Table 33–11
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE70

Resource Requirements:
- PD Simulator
- Oscilloscope
- Current probe

Last Modification: December 11, 2009

Discussion: The PSE can monitor either the DC or AC MPS component to verify if the PD is still drawing the minimum current (I_{MIN2}) that is required by the PSE. A PSE that monitors the DC MPS component of the signature will remove power from its PI if it detects that the PD is drawing current less than its I_{MIN1} (5mA) for greater than 400ms. In order to maintain a valid MPS signature, the PD can draw less than the I_{MIN1} (5mA) for 300ms and then draw more than its I_{MIN2} max (10mA) for the next 60ms(T_{MPS}) or more. This improves the power efficiency of the PSE.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the current probe. The current probe is connected to the PD simulator at the PI.

Procedure:
1. Verify that the DUT is supplying power to the PD simulator.
2. Confirm that the PD simulator is drawing more than 10 mA.
3. Set the PD simulator to draw more than 10 mA for a period of 60ms (T_{MPS}) and then drop the current back to less than 5 mA for the next 300ms. Cycle this sequence.
4. Confirm that the DUT does not remove power from the PI.

Observable Results:
- In step 4, for $T_{MPS} \geq$ 60ms the DUT does not remove power.

Possible Problems: If the DUT does not support DC MPS, then this test does not apply.

33.3.9: AC MPS Signal Parameters

Purpose: To verify that the PI AC probing signals fall within the conformance limits.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.9.1 Table 33–12, Figure 33C.15.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Items PSE64

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: Once power has been applied to the link section, the PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD has been disconnected. The PSE may monitor the AC MPS component, the DC MPS component, or both signature components. This test has been designed to verify that a PSE that monitors the AC MPS component meets the AC signal parameters as specified in Item 1(a-c) of Table 33–12, which has been printed here for convenience. These parameters can be measured as depicted in Figure 33C.15, which is also printed here for convenience.

Item	Parameter		Min	Max
	AC Signal Parameters			
1a	PI probing AC Voltage	V_open (Vpp)	1.9	10% of the average value of VPort within the limits of Table 33–11, item 1
		V_open1 (Vp)		30V, VPort≤44V
1b	AC Probing Signal Frequency	Fp (Hz)		500
1c	AC Probing Signal Slew Rate	SR (V/μs)		0.1 (Positive or negative)

Table 33–12

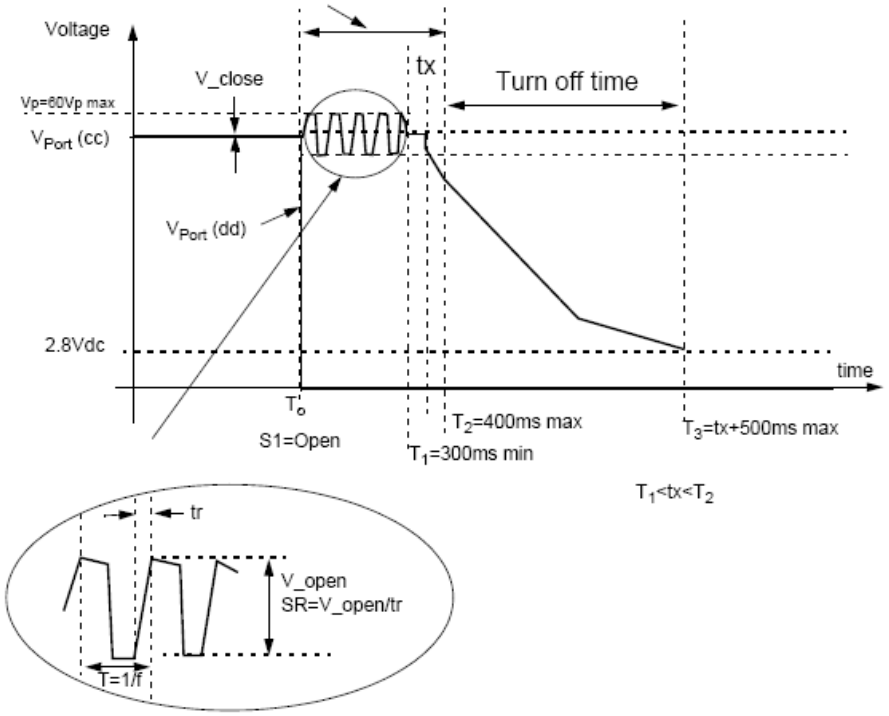

Figure 33C.15

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:

1. Attach a valid signature (less than or equal to 27KΩ) to the PI of the DUT.
2. Verify that the DUT is supplying power to the PD simulator
3. Disconnect the signature from the PI of the DUT.
4. Measure the PI probing AC voltage (V_open).
5. Measure the PI probing signal frequency.
6. Compute the AC probing signal slew rate (SR).
7. Measure the peak value (Vp).

Observable Results:

- 1.9V ≤V_open ≤10% of average value of V_{port} (44V <V_{Port} <57V).
- The PI probing frequency should not be greater than 500Hz.
- The slew rate should not be greater than 0.1V/µs.
- The peak value (Vp) should be less than 60Volts

Possible Problems: If the DUT does not support AC MPS, then this test does not apply.

33.3.10: AC MPS Signature

Purpose: To verify that the PSE that implements AC MPS component correctly monitors the PD Maintain Power Signature.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.9.1.1 Table 33–12, Figure 33–15, Figure33–16.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE64, PSE65

Resource Requirements:
- PD Simulator

Last Modification: December 11, 2009

Discussion: The PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD is disconnected. The PSE may monitor the AC MPS component, the DC MPS component, or both signature components. A PSE that monitors AC MPS component will remove power it if detects an AC impedance at the PI equal to or greater than 1980 KΩ (|Zac2|) as defined in Table 33–12, which is printed below for convenience. It may or may not remove power if it detects an AC impedance between 27K(|Zac1|) and |Zac2|. The PSE will maintain power if it detects an impendence less than or equal to |Zac1|. The PSE will remove power from its PI if the AC MPS signature is absent for more than 400ms (T_{MPDO}).

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC Maintain Power Signature					
4a	Shall not remove power from the PI	$\|Z_{ac1}\|$	KΩ		27	F_p= 5Hz, Testing voltage >2.5V. See Figure 33–16. Impedance shall have non-negative resistive component and a net capacitive reactive component.
4b	Shall remove power from the PI	$\|Z_{ac2}\|$	KΩ	1980		See Figure 33–17.

Table 33–12

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Allow the DUT to power the testboard and supply a valid current draw
2. Place an impedance in the Zac1 range across the PI
3. Remove the valid current draw and confirm that the DUT is still powering.
4. Repeat steps 2 and 3 for multiple values across the Zac1 range.
5. Place an impedance of 27KΩ across the PI

6. Repeat steps 3 and 5 increasing the impedance until the DUT disconnects

Observable Results:

- In Step 3, the DUT should supply power onto its PI.
- In Step 6, the impedance (Z) should be between 27KΩ and 1980KΩ (inclusive).

Possible Problems: If the DUT does not implement AC MPS disconnect, then this test does not apply.

33.3.11: Turn Off Time Limits

Purpose: To verify that the PSE disconnects power within T_{Off} through a test resistor.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.2.7.8, 33.2.9.1, Table 33–11
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.2, Item PSE59

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: December 11, 2009

Discussion: When the DUT is disconnected from a valid maintain power signature it should remove power within T_{Off} through a test resistor of 320kΩ attached to the PI. T_{Off} is defined as the discharge time from 1 Volt less than static V_{Port} to 2.8Vdc.

Test Setup: The DUT is connected to the PD simulator with a 1m length of Category 5 cable. The oscilloscope is connected to the PD simulator at the PI.

Procedure:
1. Verify that the DUT is supplying power to the PD simulator.
2. Disconnect DUT with a 320kΩ test resistor attached to the PI.
3. Measure the discharge time when the DUT removes power from its PI.

Observable Results:
- In step 3, $T_{Off} \leq 500ms$.

Possible Problems: For AC MPS the DUT can observe the test resistor as a valid MPS and will remain in powering mode.

Group 4: PSE Transmitter and Receiver Characteristics

Scope: This group of tests deals with conformance parameters specific to the transmitter and receiver of a PSE.

Overview: These tests are designed to identify problems with IEEE *Draft*P802.3at™/D3.3 Clause 33 compliant devices. Specifically, the problems related to the functional and electrical characteristics of Power Sourcing Equipment devices.

33.4.1: Midspan PSE Return Loss

Purpose: To verify that the return loss of a Midspan PSE is greater than the minimum conformant value.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.4.9.1.3, Table 33–20.
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.4 Item PSEEL12, Subclause 33.8.3.5 Item PSEEL11

Resource Requirements:
- Vector Network Analyzer (VNA)
- 125MHz Balun

Last Modification: December 11, 2009

Discussion: Return loss is a measure of reflected signal that results from mismatched impedances in a transmission line. The Midspan PSE is an addition to the standard Ethernet link segment or transmission line. If the impedance of the Midspan is not properly matched, the Midspan can degrade the Ethernet signaling. The Midspan's return loss must be sufficiently high to avoid this risk. The requirements are reproduced below for convenience.

Table 33–20—Connector return loss

Frequency	Return loss
1 MHz ≤ f < 20 MHz	23 dB
20 MHz ≤ f ≤ 100 MHz	14 dB

Test Setup:

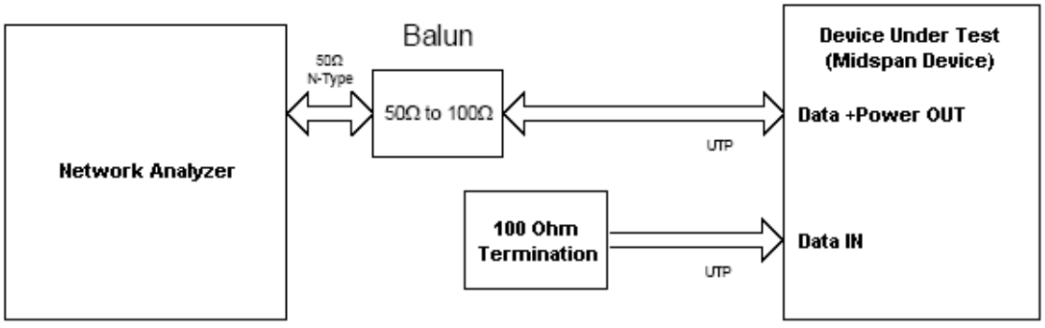

Figure 33.4.1 – Test Setup for Midspan Return Loss

Procedure:
1. Calibrate the VNA for a return loss measurement from 1-100MHz.
2. Connect the DUT to the VNA according to the setup shown in the figure 33.4.1
3. Over the frequency ranges specified in table 33–14, perform S_{11} measurements on the transmit pairs of the Midspan.

4. Repeat the measurements on the receive pairs.

Observable Results:

- The DUT must exhibit the minimum return loss over the specified frequency range.

Possible Problems: None

33.4.2: Midspan PSE Insertion Loss

Purpose: To verify that the insertion loss of a Midspan PSE is less than the maximum conformant value.

References:
[1] IEEE Std 802.3™-2012: Subclause 33.4.9.1.2—,Equation 33-19.
[2] IEEE Std 802.3™-2012: Subclause 33.9.3.5, Item PSEEL11

Resource Requirements:
- Vector Network Analyzer
- 125MHz Balun

Last Modification: December 11, 2009

Discussion: From the standard: "Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. Insertion loss should be measured for Midspan PSE devices for the transmit and receive pairs from 1 to 100MHz, and should meet the values determined by Equation 33–19. However, for frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB." The Midspan PSE is an addition to the standard Ethernet link segment. It must not degrade the Ethernet signaling. The Midspan's insertion loss must be sufficiently low to avoid this risk.

$$\text{Insertion\_loss}_{conn} \leq 0.04\ \text{SQRT}(f)\ \text{dB} \qquad \text{Eq. 33–19}$$

Test Setup:

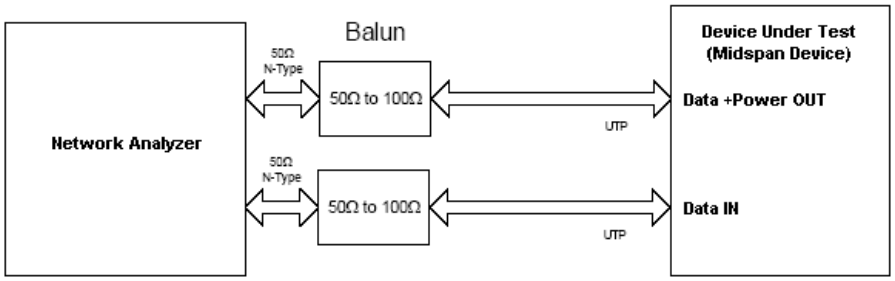

Figure IOL33.4.2 – Test Setup for Midspan Insertion Loss

Procedure:
1. Calibrate the VNA for a two port transmission measurement
2. Connect the DUT to the VNA according to the setup shown in figure 33.4.2
3. Perform S_{21} measurement from 1-100MHz on the transmit pairs of the Midspan.
4. Repeat the measurement on the receive pairs.

Observable Results:
- The DUT must exhibit the maximum insertion loss as described by equation 33–19 and the general requirement of 0.1dB.

33.4.3: Midspan PSE Near-End Cross-Talk (NEXT)

Purpose: To verify that the NEXT between the transmit and receive pairs of the DUT is within conformance limits.

References:
[1] IEEE Std 802.3™-2012: Section 33.4.9.1.1, Equation 33-18
[2] IEEE Std 802.3™-2012: Subclause 33.9.3.5, Item PSEEL10

Resource Requirements:
- Vector Network Analyzer
- 125MHz Balun

Last Modification: December 11, 2009

Discussion: The standard states: "NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. NEXT loss should be measured for Midspan PSE devices for the transmit and receive pairs from 1MHz to 100MHz and should meet the values determined by Equation (33–18). However, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\text{NEXT conn} \geq 40 - 20\log(f/100)\ \text{dB} \qquad \text{Eq. 33–18}$$

Test Setup:

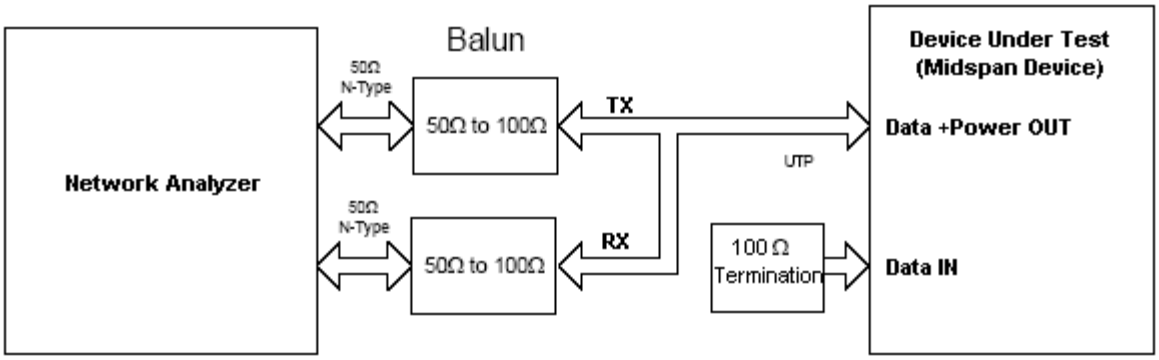

Figure IOL33.4.3 –Test Setup for Midspan NEXT

Procedure:
1. Setup DUT in test fixture as shown in figure 33.4.3
2. Perform transmission calibration on VNA
3. Measure NEXT for 1-100MHz.

Observable Results:
- The NEXT loss should exceed the requirement enumerated by equation 33–12. When the requirement for NEXT loss is greater than 65 dB (as governed by equation 33–12), the requirement reverts to the 65 dB minimum.

33.4.4: PSE Impedance Balance

Purpose: To verify that the common-mode to differential-mode impedance balance of the transmit and receive pairs of the PI is greater than the specified limits.

References:
[1] IEEE Std 802.3™-2012: Section 33.4.3, Figure 33–22, Equation 33-15, 33-16, 33-17
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.4, Item EL13

Resource Requirements:
- Vector Network Analyzer
- Impedance Balance Test Circuit
- 125MHz Balun

Last Modification: December 11, 2009

Discussion: The standard defines impedance balance as a measurement of the common-mode-to-differential-mode offset of the PI. Impedance balance is further defined by the following equation:

$20\log_{10}(E\text{cm}/E\text{dif})$ Eq. 33–17

*E*cm is an externally applied sinusoidal voltage as shown in Figure 33–20 [shown below] and *E*dif is the voltage of the resulting waveform due only to the applied sine wave. The test circuit is reprinted for convenience below:

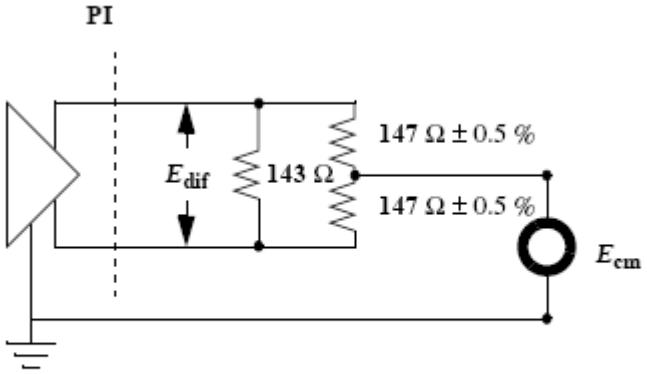

Figure 33–20—PI impedance balance test circuit

The impedance balance of the transmit and receive pairs should meet or exceed the following minimum requirements:

10 Mb/s PHY	100 Mb/s or greater PHY
$29 - 17\log10(f/10)$ dB	$34 - 19.2\log10(f/50)$ dB
Equation 33–15	Equation 33–16

where f is the frequency in MHz.

Test Setup:

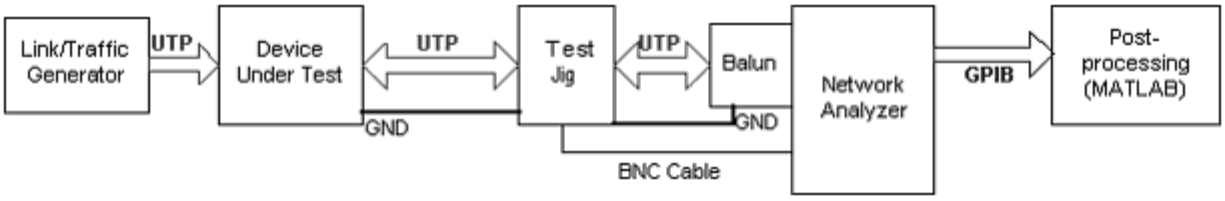

Figure IOL33.4.4 Impedance Balance Test Setup

Procedure:

1. Setup the DUT as shown in figure 33.4.4
2. Measure E_{dif} over the specified frequency range.
3. Compute the Impedance Balance.
4. Repeat the measurement with the receive pairs of the PSE.

Observable Results:

- The common-mode to differential-mode impedance balance of the transmit and receive pairs is defined as $20\log_{10}(E_{CM}/E_{D\_OUT})$ where Ecm is an externally applied sinusoidal voltage and E_{D_OUT} is the voltage of the resulting waveform due only to the applied sine wave. This can be seen in figure 33–20.
- The common-mode to differential-mode impedance balance for a 10Mb/s transmitter and receiver should exceed $29\text{-}17\log_{10}(f/10)$ (where f is the frequency in MHz) over the frequency range of 1.0 MHz to 100 MHz
- The common-mode to differential-mode impedance balance for a 100Mb/s transmitter and receiver should exceed $34\text{-}19.2\log_{10}(f/50)$ (where f is the frequency in MHz) over the frequency range of 1.0 MHz to 100 MHz

Possible Problems: None

33.4.5: PSE Common Mode Output Voltage

Purpose: To verify that the common mode AC output voltage at the PI is below the conformant limits.

References:
[1] IEEE Std 802.3™-2012: Section 33.4.4, Figure 33-23, 33-24
[2] IEEE Std 802.3™-2012: Subclause 33.8.3.4, Item EL14

Resource Requirements:
- Vector Network Analyzer

Last Modification: December 11, 2009

Discussion: From the standard: "The magnitude of the common-mode AC output voltage measured according to Figure 33–21 and Figure 33–22 at the transmit PI while transmitting data and with power applied, *E*cm_out, should not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater. The frequency of the measurement should be from 1 MHz to 100 MHz."
The common-mode AC output voltage shall be measured while the PHY is transmitting data operating with the following load:

The PI that supplies power is terminated as illustrated in Figure 33–22. The PSE load, R, in Figure 33–22 is adjusted so that the PSE output current, Iout, is 10 mA and then 350 mA, while measuring Ecm_out on the PI.

Test Setup:

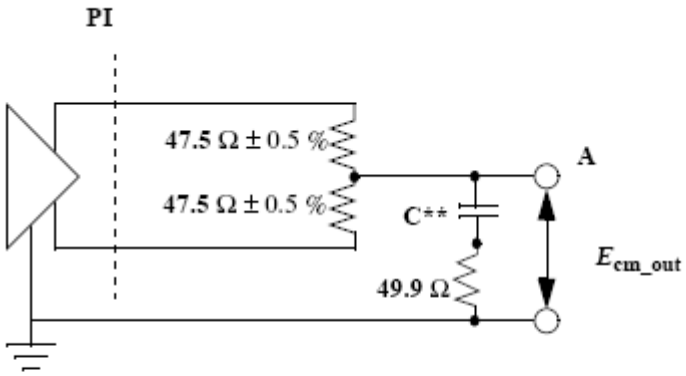

Figure 33–21—Common-mode output voltage test

Procedure:

1. Configure the device to transmit in 10 Mb/s
2. Using Smartbits, force the device to send data
3. Set up the DUT with the appropriate test jig
4. Measure the common mode AC output voltage
5. Repeat steps 1–4 with device transmitting at 100Mb/s

Observable Results:

- The magnitude of the common-mode AC output voltage, *E*cm_out, should not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater.
- The magnitude of the common-mode AC voltage should not exceed 50mV peak-to-peak measured at all other PIs.

Possible Problems: None