University of New Hampshire InterOperability Laboratory
Power Over Ethernet Consortium

Superseded

As of April 16, 2003 the Power Over Ethernet Consortium Clause 33 Physical Layer Interoperability Conformance Test Suite version 1.1 has been superseded by the release of the Clause 33 Power Sourcing Equipment Parametric Conformance Test Suite version 1.2. This document along with earlier versions, are available on the Power Over Ethernet Consortium test suite archive page.

Please refer to the following site for both current and superseded test suites:

http://www.iol.unh.edu/testsuites/ethernet/archive.html

Power Over Ethernet

Physical Layer Interoperability
Test Suite

Technical Document

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MODIFICATION RECORD

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INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers identify problems that IEEE p802.3af D4.0 devices may have in establishing link and exchanging packets with each other. The tests do not determine if a product conforms to the IEEE p802.3af D4.0 standard. Rather, they provide one method to verify that the two devices can exchange packets within the bit error ratio specifications established by the IEEE p802.3af D4.0 standard when operating over a worst-case compliant channel. The interoperability test suite focuses on two areas of functionality to simulate a real-world environment: the exchange of packets to produce a packet error ratio that is low enough to meet a desired bit error ratio while power is being supplied over the link channel, and the ability to detect and establish a link at the optimal speed between two devices that make up a link segment while power is being supplied over the link channel. A third area covers specific cable testing.

Note: Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other compliant devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in most environments.

Cable Plants

The intent of interoperability testing is to insure that the DUT will perform as expected in a real world network. Testing in a real world network is often variable. Each technology has a standard, which defines the allowable cable characteristics for that technology. To account for all of the possible cable plant scenarios in the real world, a "worst case cable plant" which is very close to the limit of the TIA/EIA cable standards is used. The cable plants are tuned to be between 1-5% above the margins specified in ANSI-TIA-EIA-568-B-2001 or other applicable specifications. A shorter patch cable is also included in testing to insure that short links between devices are also viable.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose
The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References
The references section lists cross-references to the IEEE p802.3af D4.0 standard and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements
The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification
This specifies the date of the last modification to this test.

Discussion
The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup
The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure
The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results
The observable results section lists specific items that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable result, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable result.

Possible Problems
This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

The University of New Hampshire
InterOperability Laboratory

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APPLICATION TABLE

The following table denotes whether or not the listed test is applicable to the given physical layer speed.

Table 1-1 Application of Tests to Given Physical Speeds

	10BASE-T	100BASE-TX	1000BASE-T
GROUP 1: POINT-TO-POINT INTEROPERABILITY			
Test #1.1.1: Link Speed Detection	√	√	√[1]
Test #1.1.2: Packet Error Ratio Estimation	√	√	√[1]
Test #1.1.3: Endurance Stress Test	√	√	√[1]

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[1] Note: When a Midspan device is employed 1000BASE-T speeds may be unusable, due to the internal configuration of such devices.

GROUP 1: POINT-TO-POINT INTEROPERABILITY

Scope: The following tests cover Physical layer interoperability specific to 10BASE-T, 100BASE-TX, 100BASE-FX, 1000BASE-T, and 1000BASE-X devices.

Overview: These tests are designed to identify problems that IEEE p802.3af D4.0compliant devices may have in establishing link and exchanging packets with each other.

Test #1.1.1: Link Speed Detection

Purpose: To determine if the DUT establishes the best possible link with a reference set of stations.

References:
[1] IEEE Std. 802.3, 2000 Edition Clause 28.2.3.3
[2] Annex 28B.3

Resource Requirements:
- A reference set of stations that can be used as link partners.
- Link monitoring facilities that are able to determine the signaling being used on the link.
- Local management indicators on the DUT and reference set that indicate the state of the link as perceived by the different stations.
- A channel with known characteristics within allowable margins.

Last Modification: January 10, 2003

Discussion: The ability to detect and establish a link at the optimal speed is dependent on the two devices that make up the link segment, and providing and detecting the signaling method or connection information being passed. The large majority of Fast Ethernet and Gigabit Ethernet products use IEEE Std. 802.3, 2000 Edition Clause 28 Auto-Negotiation while some use different proprietary schemes to detect the link partner's speed or do not detect link speed at all. This test procedure addresses three conditions in which link speed detection should work. The first procedure covers the case where the DUT is initialized before the remote station and there is no signal on the DUT's receiver. The second procedure covers the case where the DUT is initialized after the remote station and there is a signal from this remote station on the DUT's receiver. The third procedure covers the final case where the DUT is in an operational state and is connected to a station that is also in an operational state. These three conditions are checked, as there may be different signals on the line during the boot up sequences of the devices that could cause the DUT to detect and establish a link at the wrong speed. This test also exams the cases where the DUT is linked to a link partner then disconnected to an alternate device and then reconnected to the link partner in order to determine that the DUT will link at the optimal speed independent of the previous connection speed.

This test is an interoperability test. Failure of this test does not mean that the DUT is non-conformant. It does suggest that a problem in the ability of two devices to work "properly" together exists and further work should be done to isolate the cause of the failure.

Table 1-2 Minimum Media Specifications by Technology (UTP)

Technology	Media Type
10BASE-T	Category-3
100BASE-TX	Category-5
1000BASE-T	Category-5

Table 1-3 Application of Test Sections to Given Physical Connections

	PD to PSE	PD to Midspan to Testing Station	PSE to Legacy	PSE to PSE
Test #1.1.1: Link Speed Detection				
Part A: Case 1		√	√	√
Part A: Case 2	√	√	√	√
Part A: Case 3	√	√	√	√
Part B:		√	√	√

Test Setup: Connect the DUT to another device via the appropriate media channel as outlined in Table 1-2, while supplying power over the channel (except for legacy device interoperablilty testing).

Procedure:
Part A
Case 1: The DUT receives no signal from the link partner during initialization. (Note: This case is only applicable to PSEs and PDs receiving power from a Midspan device.)

1. Power off the DUT and the link partner.
2. Connect a compliant high attenuation media channel (Refer to Table 1-2 and Table A-2) between the two devices.
3. Power on the DUT and ensure that the device is initialized and all needed drivers are loaded.
4. Power on the test link partner and verify that it is initialized and all needed drivers are loaded.
5. Check local management information to verify that the link is established at the proper speed and that link auto-negotiation, if supported, negotiated the optimal common values for the two devices.
6. Send the DUT a series of packets and observe whether the packets are accepted or not.

Case 2: The DUT receives signal from the link partner during initialization.

1. Power off the DUT and the link partner.
2. Connect a compliant high attenuation media channel (Refer to Table 1-2 and Table A-2) between the two devices.

3. Power on the link partner and ensure that the device is initialized and all needed drivers are loaded.
4. Power on the DUT and verify that it is initialized and all needed drivers are loaded. Check local management information to verify that the link is established at the proper speed and that link auto-negotiation, if supported, negotiated the optimal common values for the two devices.
5. Send the DUT a series of packets and observe whether the packets are accepted or not.

Case 3: The DUT establishes link with a fully powered and operational link partner. (Note: this case is only applicable to PSEs and PDs receiving power from a Midspan device)
1. Power off the DUT and the link partner.
2. Power both devices back on at the same time and allow them to initialize.
3. Connect a compliant high attenuation media channel (Refer to Table 1-2 and Table A-2) between the devices.
4. Verify that a proper link is established as in Cases 1 and 2.
5. Remove and hold the cable for a few seconds, then reinsert. Repeat five times. Check local management information to verify that the link came up at the proper speed and that link auto-negotiation, if supported, negotiated the optimal common values for the two devices.
6. Send the DUT a series of packets and observe whether the packets are accepted or not.

Part B (Note: this case is only applicable to PSEs and PDs receiving power from a Midspan device)
1. Establish a valid Highest Common Denominator (HCD) link between the DUT and link partner via a compliant high attenuation media channel (Refer to Table 1-2 and Table A-2). Verify that a valid HCD link is established.
2. Break the link and connect the DUT to a testing station configured to send link signaling at a speed other than the HCD.
3. Reconnect the DUT to the link partner. Verify that a valid HCD link is re-established.
4. Repeat steps 1-3 for all speeds supported by the link partner.

Observable Results:
a. The DUT and the link partner should establish an HCD link in all cases. Both the DUT and link partner must be examined for indicators of proper link speed and type. This is typically an LED that indicates when a link is established. Many devices provide some indication of link speed as well. Local management may provide information about configuration such as link duplex status as well as link speed.
b. The DUT should establish an HCD link as described in part a.

Possible Problems: If management access is not provided, it may be difficult to determine if the DUT resolves a link at the proper speed. If a Midspan device is employed to power a PD it should be noted that 100BASE-TX full duplex should be the HCD as 1000BASE-T signaling may be interrupted by Midspan equipment.

Test #1.1.2: Packet Error Ratio Estimation

Purpose: To determine if the DUT can exchange packets with a link partner such that the exchange of packets must produce a packet error ratio that is low enough to meet a desired bit error ratio.

References:
- [1] ISO/IEC 9314-3:1990, Section 8
- [2] ANSI/TIA/EIA-568-B-2001
- [3] IEEE p802.3af D4.0
  - (a) 10BASE-T: - Clause 14
  - (b) 100BASE-TX: - subclause 24.1.4.3, Clause 25
  - (c) 100BASE-FX: - 24.1.4.3, Clause 25
  - (d) 1000BASE-X: - subclauses 36.1.4.3, Clause 38
  - (e) 1000BASE-T: - Clause 40
- [4] IOL FEC 100BASE-TX PMD Test Suite Appendix 25D

Resource Requirements:
- A set of reference stations that can be used as link partners.
- Two test stations, one that can be used to source packets, and one that can be used to respond or echo the sourced packet. These stations must be able to provide detailed counts of packets transmitted, received, as well as information on errors associated with link level operation.
- Local management indicators on the DUT that provide information on link level errors such as CRC errors, and frame counts. (Optional)
- Cable channels with well known compliant properties applicable to the appropriate technology referenced in Appendix A.

Last Modification: January 10, 2003

Discussion: This test is designed to verify the ability of a DUT to exchange packets with another station over the appropriate cable model. The exchange of packets must produce a packet error ratio that is low enough to meet a desired bit error ratio. The IOL uses a packet error ratio specification outlined in Appendix A Table A-1; this will insure the bit error ratio with 95% accuracy. The packets sourced by the testing station are then sent back to the DUT or an echo responder. If more than 14 packets are lost during the exchange, the bit error ratio criterion has not been met and the test fails. In addition to packets lost, local management information may make it possible to isolate the packet loss to either the transmit side or the receive side of the test channel relative to the DUT. If more than seven packets are lost in either side of the channel, then the DUT has failed the bit error ratio and the DUT has failed the test.

The observable results in this testing process are one or more packet counters. A single packet contains many bits; therefore the measurement technique does not actually measure the bit error ratio. The pass/fail criterion assumes that no more than one bit is in error in a lost packet. Thus, a device may, in theory, pass a test with a bit error ratio in excess of those specified in Table A-1. However, given that any one bit in error will corrupt the packet, multiple errors within a packet

do not, in practice, make a difference in the number of packets that must be retransmitted on real links. Thus, a short-term clock deviation that causes a bit error ratio of 5 bits in a stream of 10^8 bits will, under most conditions, cause as many packet errors as a device with a bit error ratio of 1 in 10^8.

For the purposes of this test the exchange of packets is performed using packets of length 64-bytes and of length 1518-bytes. The former, being the minimum specified frame size for a device implementing the CSMA/CD MAC sublayer, yields the least amount of time to process a single packet header and provides the smallest probability of multiple errors occurring in a single packet. The latter, specified as the maximum untagged frame size, provides the longest single packet transmission time and the highest probability of an error to be present.

The underlying issues, which cause bit errors in the transmission of packets in this testing process, have the tendency to vary due to the statistical nature of such events. In past testing, the IOL has observed a significant variation in the number of packets in error for a given set up. **The results obtained from this testing process should therefore not be seen as a true measure of the bit error ratio, but as information that may suggest the need for further analysis.**

Test Setup: The DUT is tested against a link partner while power is being supplied over the channel (except for legacy device interoperability testing). The link partner is the device at the other end of the channel being used for interoperability testing. There are four possible setups depending on the type of device being tested and the type of link partner. Both the DUT and the link partner may be either an end station or an internetworking device. For our purposes an internetworking device is any device that receives packets on one port and forwards them out another port. End stations are those devices that generate and respond to ICMP packets.

The following four figures show the respective setups for end stations and internetworking devices. In Figure 1-1 the DUT is an end station such as a Personal Computer (PC) Network Interface Card (NIC) and it is being tested against another device that is an end station, such as another PC NIC. In Figure 1-2 the DUT is still an end station but the link partner is an internetworking device. In this case the link partner connects a third station into the network, which either sources or sinks the packets. This device is called the echo source/responder or simply, the testing station. The channel between the link partner and the testing station must be compliant with the appropriate standard. Figure 1-3 covers the case where the DUT being an internetworking device as well as the link partner being an internetworking device. Figure 1-4 covers the final case where the DUT is either a Midspan device or is a PD receiving power from a Midspan while passing traffic to a testing station.

For simplicity of presentation, the DUT and its link partner will be categorized as either Data Terminal Equipment (DTE) or Data Connecting Equipment (DCE). For the purposes of this explanation, the term DTE will be used to indicate a network interface card, print server, or a router. The term DCE will be used to indicate a repeater, a buffered distributor, or an unmanaged switch.

Case 1: DTE to DTE

Connect the DUT to its link partner through the reference environment as shown in Figure 1-1.
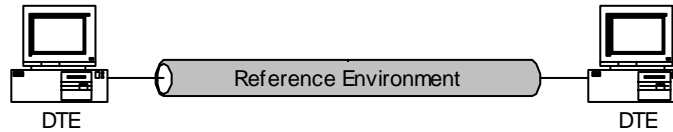
Figure 1-1 Both the DUT and link partner are DTEs

Case 2: DTE to DCE

Connect the DUT to its link partner through the reference environment as shown in Figure 1-2. The testing station will exchange packets with the DTE. The link between the testing station and the DCE must be error free.

Figure 1-2 The DUT is a DTE and the link partner is a DCE, or vice versa

Case 3: DCE to DCE

Connect the DUT to its link partner through the reference environment as shown in Figure 1-3. The testing stations will exchange packets. The links between the testing stations and the DCEs must be error free.
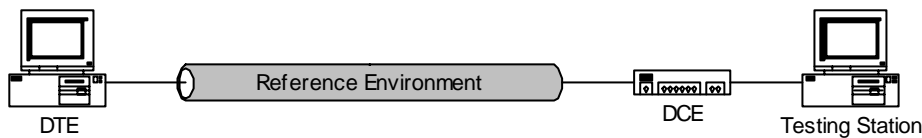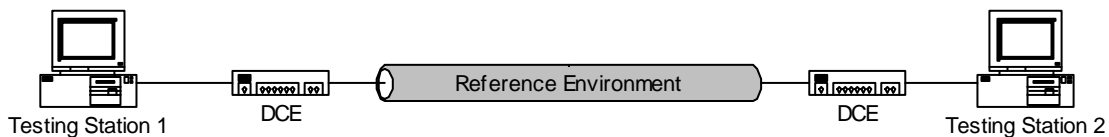

Figure 1-3 Both the DUT and link partner are DCEs
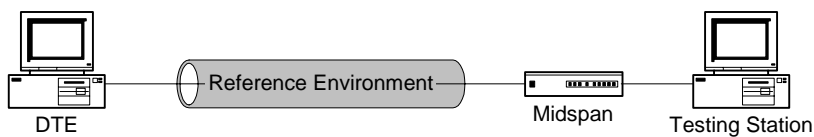
Case 4: DTE (Midspan Powered) to Testing Station

Figure 1-4 Midspan powered equipment

Test Setup: Connect the DUT to its link partner with an appropriate media channel as outlined in Appendix A.

Procedure:
1. Connect the high attenuation channel between the DUT and the link partner.
2. Reset all counters that will be used to measure or monitor the exchange of packets between the DUT and the link partner. Configure software as needed.
3. Via Auto-Negotiation or manual configuration, place the DUT and its link partner into compatible modes of operation.
4. Using the echo source, transmit (n) 64-byte ICMP echo request packets to the IP address of the echo responder. Where (n) is the 64-byte value determined from Table A-1.
5. Using the echo source, transmit (m) 1518-byte ICMP echo request packets to the IP address of the echo responder. Where (m) is the 1518-byte value determined from Table A-1.
6. Repeat steps 2-4, replacing the current media channel with a low-attenuation channel.

Observable Results:
a. Using the counters on the echo source station, identify the number of ICMP echo reply packets received. The difference between the number of ICMP echo request packets sent and the number received is the number of lost packets. An ARP request and response may have occurred during the testing, adjust as needed. This value should be examined with other information gathered during the testing process to ensure that the failure is due to bit errors and not resource errors on the DUT or testing stations. In the ideal case all lost packets are identified on one of the testing stations or the DUT as either an FCS error, or some other type of receiver error. If the local information gathered from the DUT is reliable it is often possible to isolate the failure to either the transmitter channel or the receiver channel. No more than seven packets may be lost on either side of the channel (transmit or receive). If it is not possible to determine which side of the channel the packets were lost on, no more than fourteen packets may be lost.

Possible Problems:
- Bit errors that occur outside the range of FCS coverage will not be detected.
- Some of the adapter cards will generate DMA underrun conditions causing the testing station or DUT to generate truncated packets.
- A number of devices may transmit packets during the testing process that are not associated with the testing. These frames are often multicast frames but not always.

Test #1.1.3: Endurance Stress Test

Purpose: To verify that no obvious buffer management problems occur when directing a large volume of traffic at the DUT.

References:
- [1] ISO/IEC 9314-3, 1990
  - (a) 100BASE-FX: - Clause 8
- [2] IEEE Std 802.3af D4.0
  - (a) 10BASE-T: - Clause 14
  - (b) 100BASE-TX: - subclause 24.1.4.3, Clause 25
  - (c) 100BASE-FX: - 24.1.4.3, Clause 25
  - (d) 1000BASE-LX: - subclauses 36.1.4.3, Clause 38
  - (e) 1000BASE-SX: - subclauses 36.1.4.3, Clause 38
  - (f) 1000BASE-T: - Clause 40

Resource Requirements:
- Two test stations, one that can be used to source packets at minimum inter-packet gap (IPG), and one that can be used to respond or echo the sourced packet. These stations must be able to provide detailed counts of packets transmitted, received, as well as information on errors associated with link level operation.

Last Modification: January 10, 2003

Discussion: This test is informative only and is designed to verify that the DUT has no obvious buffer management problems. In the first section of this test, the DUT is attached to a sourcing station (Refer to **Error! Reference source not found.**) that is capable of sending an appropriate number of 64-byte ICMP echo requests as outlined in Table 1- with a minimum IPG of 96BT. The DUT does not have to respond to all of the requests but the test should not cause any system failures.

The observable results in this testing process are one or more packet counters. In past testing the IOL has observed a significant variation in the number of packets in error for a given set up. **The results obtained from this testing process should therefore not be seen as a true measure of the performance of the device but as information that may suggest the need for further analysis.**

Test Setup: A link is established between the DUT and the testing station while power is being supplied over the channel (except for legacy device interoperability testing). There are three possible setups depending on the type of device being tested. The DUT may be either an end station or an internetworking device. For our purposes an internetworking device is any device that receives packets on one port and forwards them out another port. End stations are those devices that respond to an ICMP echo request packet. When the DUT can play both the role of an end station and an internetworking device it is treated as an internetworking device.

The following two figures show the respective setups for end stations and internetworking devices. In Figure 1- the DUT is an end station such as a PC NIC. It is connected to the testing station, which works as an end station, such as another PC NIC. In Figure 1- the DUT is an internetworking device connected to two testing stations, one to source and the other to respond or echo the sourced packets.

For simplicity of presentation, the DUT and its link partner will be categorized as either a DTE or a DCE. For the purposes of this explanation, the term DTE will be used to indicate a network interface card, a managed switch, a router, or the testing station. The term DCE will be used to indicate a repeater, a buffered distributor, or an unmanaged switch.

Table 1-3 Packet Error Ratio Verification

Technology	BER	# of Packets
10BASE-T	10^{-8}	468,000
100BASE-TX	10^{-9}	4,680,000
1000BASE-T	10^{-10}	46,800,000

Case 1: DTE to Testing Station

Connect the DUT to the testing station as shown in Figure 1-.

DTE   Reference Environment   DTE
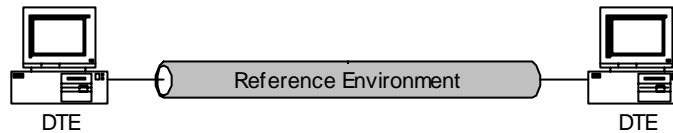
Figure 1-5 Both the DUT and testing station are DTEs

Case 2: DCE to Testing Stations

Connect the DUT to its link partner through the reference environment as shown in Figure 1-. The testing station will exchange packets with the DTE. The link between the testing station and the DCE must be error free.

Testing Station Reference Environment DCE Testing Station
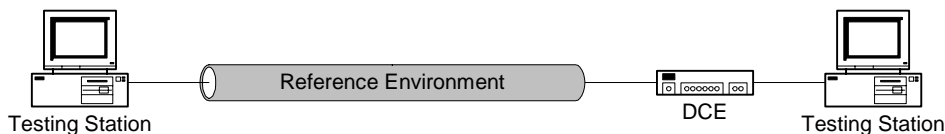
Figure 1-6 The DUT is a DCE and the testing stations are DTEs

Case 3: DTE (Midspan Powered) to Testing Station
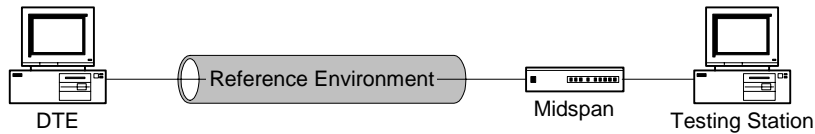
Figure 1-7 Midspan powered equipment

Procedure:

1. Connect the appropriate high attenuation channel between the DUT and the test station(s) determined from Appendix A.
2. Reset all counters that will be used to measure or monitor the exchange of packets between the DUT and the testing station. Configure software as needed.
3. Using the echo source, transmit (n) 64-byte ICMP echo request packets with an IPG of 96BT to the IP address of the echo responder, where (n) is the 64-byte value determined from Table 1-.

Observable Results:

a. Using the counters on the echo source station, identify the number of ICMP echo reply packets received. The difference between the number of ICMP echo request packets sent and the number received is the number of lost packets. An ARP request and response may have occurred during the testing, adjust as needed. The DUT does not have to respond to all of the requests, but the test should not cause any system failures.

Possible Problems: None

GROUP 2: Test Suites Related to PSE testing

Scope: The following tests cover parametric tests specific to Power Sourcing Equipments that support 10BASE-T, 100BASE-TX, 100BASE-FX, and 1000BASE-T devices.

Overview: These tests are designed to identify problems that IEEE p802.3af D4.1compliant devices may have in establishing link and exchanging packets with each other.

Test # PSE Detection Circuit

Purpose: To verify the Thevenin equivalent detection circuit of the PSE detection source.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Sections 33.2.5 and Figures 33-8, 33-9

Resource Requirements:
- 45kΩ test load
- Current Source
- Current Meter
- Oscilloscope

Last Modification: March 4, 2003

Discussion: The PSE should detect the PD via the PSE PI. The PSEs detection circuit should have a Thevenin equivalent circuit consistent with Figure 33-8 or 33-9 in all detection states. This is intended to prevent a PSE to PSE connection from detecting a valid PD signature.

Test Setup:

PSE Detection Source (Figure 33-8): Connect the PSE to the PD simulator with a 1m length of Category 5 cable. An oscilloscope is connected across the PI of the PD simulator. A 45kΩ load is attached to the PDs PI.

Alternative PSE Detection Source (Figure 33-9): Connect the PSE to the PD simulator with a 1m length of Category 5 cable. A current meter is connected to the PI of the PD simulator. A current source is connected to the PI of the PD simulator to inject current to the $V_{detect+}$ port.

Procedure:
1. Connect the current source to the PI
2. Measure the current flowing into the $V_{detect+}$ port of the PSE
3. If current was not accepted in step 2, measure the maximum output voltage of the open circuit PI. Otherwise, the test is complete.
4. Disconnect the current source
5. Connect the 45kΩ test load to the PI
6. Measure the maximum output voltage of the loaded PI

Observable Results:
a. If the DUT does not accept current into the Vdetect+ port, the DUT follows Figure 33-9. Otherwise, the DUT should accept current into the Vdetect+ port, the DUT should show a loaded PI voltage of less than half of the open circuit PI voltage, according to Figure 33-8.

Possible Problems: None

Test # Backdrive Current

Purpose: To verify the detection circuit of the PSE can withstand maximum backdrive current at maximum voltage.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.5, Table 33-5

Resource Requirements:
- Current Source
- PD Simulator

Last Modification: March 4, 2003

Discussion: The PSE must be able to handle a PSE to PSE connection. This is specified as being a backdrive current of 5mA at a voltage corresponding to V_{Port}. In order to test the maximum limits, the maximum value of V_{Port} as specified in table 33-5 should be used. After the maximum backdrive current has been applied, the DUT should still be capable of detecting an attached PD.

Test Setup: Connect the PSE to the PD simulator with a 1m length of Category 5 cable. Connect a current meter to the PI of the PD simulator. Connect a current source to the PI of the PD simulator.

Procedure:
1. Using the 5mA source, inject a current into the PSEs $V_{detect+}$ port for 10 seconds.
2. Disconnect the current source from the PSE and attach a valid PD signature
3. Observe if the PSE correctly detects the PD and supplies power
4. Disconnect the valid PD
5. Re-connect the current source and inject current into the PSEs $V_{detect-}$.
6. Disconnect the current source
7. Re-connect the PSE to a valid PD
8. Observe if the PSE correctly detects the PD and supplies power

Observable Results:
- In step 3, the DUT should properly detect a PD signature.
- In step 5, the DUT should not be affected by the backdrive current.
- In step 8, the DUT should properly detect a PD signature.

Possible Problems: None.

Test # 33.2.5-3 Detector Circuit Output Current

Purpose: To verify that the short circuit output current of the PSE during PD detection conforms to the specifications defined in Table 33-2.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.5, Table 33-2

Resource Requirements:
- PD Simulator
- Oscilloscope
- Current meter

Last Modification: March 4, 2003

Discussion: The PSE should limit its output current during detection such that in the event of a short circuit condition the PSE will not be damaged. The output current for the PSE detection circuit should conform to the values in Table 33-2. This value assures the PSE and any attached media will not be damaged.

Test Setup: Connect the DUT to the PD simulator configured as a short circuit.

Procedure:
1. Using the current probe, measure the short circuit current at the PI.
2. Repeat step 1 for all probe voltages sourced by the DUT.

Observable Results:
- In step 1, the short current should not exceed 5 mA.

Possible Problems: None

Test # 33.2.5-3 Detector Circuit Output Voltage

Purpose: To verify the voltage output of the PSE detection circuit conforms to the specifications defined in Table 33-2.

- **References:** IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.5, Table 33-2

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: March 4, 2003

Discussion: The PSE should detect the PD by probing via the PSE PI. When a valid PD signature is connected, the detection voltage Vdetect should be within the Vvalid voltage range at the PSE PI as specified in Table 33-2. The loaded circuit values are measured with a valid PD signature attached to the PSE. The PSE should make at least 2 measurements with Vdetect values that create at least a ΔVtest difference as specified in Table 33-2. The PSE should measure the voltage or current after Vdetect has settled to within 1% of its steady state condition. These values assure the PSE will not overload an attached device.

Test Setup: Connect the DUT to a high impedance probe to measure the open circuit voltages sourced by the PSEs detection circuit. Connect the PSE to the PD simulator to test the probe voltages when a load is attached.

Procedure:
1. Using the oscilloscope, measure the open circuit voltage at the PI.
2. Attach the PD simulator to the PI.
3. Using the oscilloscope, measure the probe voltage at the PI.
4. Using the oscilloscope, measure the slew rate of the probe voltages.
5. Repeat steps 3 & 4 for each probing voltage supplied by the DUT.

Observable Results:
- In step 1, the open circuit voltage seen at the PI should be less than or equal to 30 volts.
- In step 3, the loaded PI output detection voltages should be between 2.8 and 10 volts.
- In step 4, the slew rate of the probe voltages should be less than or equal to 0.1 V/μs
- In step 5, the voltage difference between consecutive detection probe voltages should be at least 1 volt.

Possible Problems: None

Test # PD Signature Detection Limits

Purpose: To verify that the DUT will properly detect a PD's Signature Impedance.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.6; Figures 33-8, 33-9

Resource Requirements:
- PD Simulator
- Voltmeter

Last Modification: March 4, 2003

Discussion: The PSE should be able to detect the signature impedance of an attached PD. This detection is accomplished by probing the PD via the PI. From this signature, the PSE should determine whether or not to supply power to the attached PD. The PSE should only provide power if the PD presents a signature which is compliant with Table 33-2; otherwise, the PSE should not supply power onto the PI.

Test Setup: Connect the PSE to the PD Simulator with a 1m length of Category 5 cable.

Procedure:

Part a: Input Resistance Minimums
1. Adjust the PD simulator to have a valid input signature capacitance (2nF)
2. Increase the signature resistance from $R_{bad}min$ until the DUT supplies power to the PD
3. Record the value at which the PSE accepts the PD signature resistance.
4. Decrease the signature resistance below $R_{good}min$ until the DUT does not supply power to the PD
5. Record the value at which the PSE rejects the PD signature resistance.

Part b: Input Resistance Maximums
6. Increase the signature resistance above $R_{good}max$ until the DUT does not supply power to the PD
7. Record the value at which the PSE rejects the PD signature resistance.
8. Decrease the signature resistance from $R_{bad}max$ until the DUT supplies power to the PD
9. Record the value at which the PSE accepts the PD signature resistance.

Part c: Input Capacitance "Must Accept"
10. Set the PD signature model to have a resistance between $R_{good}min$ and $R_{good}max$ (22kΩ)
11. Set the PD signature model to have a capacitance of $C_{sig}max$ (119nF)
12. Connect the PD signature model to the PI of the PSE and observe the voltage at the PI

Part d: Input Capacitance "Must Reject"
13. Set the PD signature model to have a capacitance of greater than $C_{bad}min$ (10.5μF)

14. Connect the PD signature model to the PI of the PSE and observe the voltage at the PI

Observable Results:

    a. In step 3 and 5, the resistance should be between 15kΩ and 19kΩ
    b. In step 7 and 9, the resistance should be between 26.5kΩ and 33kΩ
    c. In step 12, the DUT should accept the PD signature and provide power
    d. In step 14, the DUT should reject the PD signature and not provide power

Test # PSE Classification

Purpose: To verify a PSE supporting classification properly performs PD class detection.

Reference:
 [1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.7.1,33.2.7.2, Table 33-4,
    Table 33-3, Table 33-6, Figure 33C.19, Annex 33C.4.

Resource Requirements:
 - PD simulator
 - Oscilloscope

Last Modification: March 4, 2003

Discussion: The PSE may attempt to classify the PD, and the PD may provide information, to allow features such as load management to be implemented. The PSE should probe the PD with a voltage between 15 and 20 volts limited to 100 mA The PSE should measure I_{Class} and classify the PD based on the observed current as per Table 33-4.

Test Setup: Connect the PSE to the PD simulator with a 1m length of Category 5 cable.

Procedure:
 1. Set the load resistance to the minimum.
 2. Measure V_{Class} using an oscilloscope before T_{pdc}.
 3. Measure the current I_{Class}.
 4. Vary the resistance stepwise to draw the different levels of current.
 5. After the classification time (T_{pdc}), measure the voltage (V_{Port}) across the PD model.
 6. Compute the power at the output of the PSE.

Observable Results:
 a. In step 2 the PSE should supply voltage between 15-20 Volts.
 b. In step 3 if the I_{Class} is greater than or equal to 47mA the PSE should not power the PD.
 c. In step 3 the PSE should accurately classify the PD.
 d. In step 4 the PSE should supply current not higher than 100 mA.
 e. In step 6 the PSE should supply appropriate power after classification of the PD as per Table 33-3.

Possible Problems: If the PSE does not perform classification, then the PSE should assign the PD to Class 0.

Test # PSE Classification timing

Purpose: To verify that a PSE capable of classifying a PD should complete the classification within Tpdc after successfully completing the detection of a PD.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.8, Table 33-5

Resource Requirements:
- Oscilloscope
- PD Simulator

Last Modification: March 4, 2003

Discussion: After successful detection of a PD, and if the PSE supports classification, then it must complete classification within the time frame of T_{pdc}. The classification should occur anytime within the time frame of T_{pon}. If the PSE fails to power the PD within T_{pon}, it must reinitiate the detection and optional classification sequence.

Test Setup: Connect the PSE to the PD simulator with a 1m length of Category 5 cable.

Procedure:
1. Measure the delay from the time that the DUT initiates classification to the time that it has completed one classification cycle by measuring the width of the classification pulse.

Observable Results:
a.   In step 1 the time delay should be less than T_{pdc}.

Possible Problems: **None.**

Test # PD MPS Dropout Time Limits

Purpose: To verify that the PSE correctly monitors the PD Maintain Power Signature.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.8.6 and Table 33-5

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: March 4, 2003

Discussion: The PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD is disconnected. There are two methods specified for determining this: Option "a" ensures detection of a disconnect by monitoring current drawn; Option "b" ensures detection of a disconnect by monitoring the AC impedance. If the PSE implements Option "a", the DUT should remove power from the PI if the current drawn by the PD drops below 5mA for more than T_{MPDO}. This test is only applicable for devices which implement Option "a".

Test Setup: Connect the PSE to the PD Simulator with a 1m length of Category 5 cable.

Procedure:
1. Set the PD Simulator to draw 20mA of current from the PSE
2. Decrease the current draw of the simulated PD to below 9mA for 500ms or more.
3. Observe the output voltage of the DUT.
4. If the PSE has not disconnected power, reduce the current to below 4mA for 500ms or more.
5. Observe the output voltage of the DUT.

Observable Results:
- a. In Step 3, the DUT may disconnect power from the PI.
- b. In Step 5, the DUT must disconnect power from the PI.

Possible Problems: If the DUT does not implement Option "a", the DUT may never remove power.

Test # PD MPS Dropout Time Limits

Purpose: To verify that the PSE correctly monitors the PD Maintain Power Signature.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.8, 33.2.10 and Table 33-5

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: March 4, 2003

Discussion: The PSE must monitor the link segment for the PD's Maintain Power Signature, and remove power if it detects that the PD is disconnected. There are two methods specified for determining this: Option "a" ensures detection of a disconnect by monitoring current drawn; Option "b" ensures detection of a disconnect by monitoring the AC impedance. If the PSE implements Option "a", the DUT should remove power from the PI if the current drawn by the PD drops below 5mA for more than T_{MPDO}. This test is only applicable for devices which implement Option "a".

Test Setup: Connect the PSE to the PD Simulator with a 1m length of Category 5 cable.

Procedure:
1. Adjust the PD Simulator to have a current draw of 15mA.
2. Reduce the current drawn by the PD to 2mA for $t < T_{MPDO}$.
3. Observe the voltage output of the PSE at the PI.
4. Repeat Steps 2 and 3, using a reduced t, to find the minimum time which the PSE will continue sourcing power to the PD.

Observable Results:
- The PSE should maintain power for times greater than 400ms
- The PSE should disconnect power for times less than 300ms
- The PSE may disconnect power for times between 300 and 400ms

Possible Problems: If the DUT does not implement Option "a", this test cannot be performed.

Test # 33.2.9 Power Feed Ripple and Noise

Purpose: To verify the power feeding ripple and noise are below the specified amount.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.10 and Table 33-5

Resource Requirements:
- Oscilloscope
- PD Simulator
- Voltmeter
- Current Meter

Last Modification: March 4, 2003

Discussion: The PSE should source power at all rated levels with noise and ripple which are below the levels specified in Table 33-5. Excessive noise may cause attached PDs to behave abnormally.

Test Setup: Connect the PSE to the PD simulator with a 1m length of Category 5 cable.

Procedure:
1. Adjust the PD to sink .44 watts.
2. Measure the amount of pair-to-pair ripple and noise voltage at the PD.
3. Measure the amount of common-mode ripple and noise voltage at the PD.
4. Adjust the PD to sink 15.4 watts.
5. Repeat steps 3 and 4.

Observable Results:
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 0-500Hz will be less than .5 volts
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 500Hz-150kHz will be less than .2 volts
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 150kHz-500kHz will be less than .15 volts
- The ripple and noise peak-to-peak voltages, pair-to-pair and common-mode, in the band 500kHz-1MHz will be less than .1 volts

Possible Problems: None.

Test # Load Regulation

Purpose: To verify that the PSE performs load regulation while supplying power to the PI.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.8, Table 33-5

Resource Requirements:
- PD Simulator
- Oscilloscope

Last Modification: March 4, 2003

Discussion: The PSE should perform voltage regulation while supplying power to a PD over the PI. This requires that if the load changes at a maximum rate of 35mA/µs, the output voltage of the PSE should stay between 44 and 57 volts. The PSE must also not produce any transients greater than 3.5V/µs. These requirements prevent the voltage supply from exceeding the operating range of a PD.

Test Setup: Connect the PSE to the PD Simulator with a 1m length of Category 5 cable.

Procedure:
2. Connect the PSE to the PD simulator with a valid signature and the load set to draw 10mA.
3. Connect the Oscilloscope to the PI of the PD.
4. Adjust the current draw of the PD from 10mA to 350mA in less than 9.7µs. .
5. Observe the voltage transients and output voltage of the PSE at the PI.

Observable Results:
7. The voltage transients seen should not exceed 3.5V/µs.
8. The PSE output voltage at the PI should be within the range of 44 to 57 volts.

Test # Power turn on timing

Purpose: To verify that the PSE starts applying power within T_{pon} after it has successfully detected the PD.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.2.8.15, Table 33-5

Resource Requirements:
- Oscilloscope
- PD Simulator

Last Modification: March 4, 2003

Discussion: The PSE must power on the PD after detection and optional classification within T_{pon}. If the PSE supports classification then it must successfully complete classification within the time frame of T_{pdc}. If the PSE fails to power the PD within T_{pon}, it must reinitiate the detection and optional classification sequence.

Test Setup: Connect the PSE to the PD simulator with a 1m length of Category 5 cable.

Procedure:
1. Confirm that the detection of the PD has been successfully completed.
2. Measure the time delay between the end of detection and when the PSE starts applying power.

Observable results:
a. In step 2 the time delay should be less than T_{pon}.

Possible Problems: None.

GROUP 3: Test Suites Related to PD testing

Scope: The following tests cover parametric tests specific to Powered Devices that support 10BASE-T, 100BASE-TX, and 1000BASE-T devices.

Overview: These tests are designed to identify problems that IEEE Draft P802.3af/ D4.1compliant devices may have in establishing link and exchanging packets with each other.

PD source power

Purpose: To verify that PD does not source power

Reference:
[1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.3.1, Table 33-7, Figure 33-5.

Resource Requirements:
- Voltmeter

Last Modification: March 6, 2003

Discussion: The PD should not source power on its PI at any time.

Test Setup: Connect the DUT to a voltmeter.

Procedure:
1. Measure the V_{Port} at the PI of the DUT using a voltmeter.
2. Verify that there is no power at the PI

Observable Results:
a. In step 1 the DUT should not source any power on its PI.

Possible Problem: None

Test # PD Pinout

Purpose: Verify that the PD operates in PD Mode-B and per at least one of the PD Mode-As.

Reference:
 [1]   IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Sections 33.3.1, Figure 33-5, Table 33-7

Resource Requirements:
- Voltage Source
- PSE Simulator

Last Modification: March 6, 2003

Discussion: After detection and optional classification, a PSE could supply power on either set of the four wire pairs, hence the PD must be able to support both Mode A and Mode B. In addition, a PD should not accept power simultaneously on both wire pairs. The PD must be able to operate in at least one of the PD Mode A columns, and in the PD Mode B column in Table 33-7. A PD that implements Auto-MDI-X should be polarity insensitive.

Test Setup: The PD is connected to a voltage source.

Procedure:
1. Set the PSE simulator to supply power in accordance to Mode A MDI.
2. Check if the DUT is powered up.
3. Repeat steps 1 and 2 for Mode A MDI-X and Mode B.

Observable Results:
a. The DUT must accept power in Mode B and in at least one of the setups for Mode A.

Possible Problems: None

Test # Valid PD detection signature characteristics

Purpose: Verify valid PD detection signature characteristics measured at PD input connector.

References:
 [1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Section 33.3.3, Annex 33C.4, Figure 33C.19, 33C.20, 33C.21, Table 33-8

Resource Requirements:
- PSE Simulator
- Oscilloscope
- Current meter
- Inductance meter

Last Modification: March 6, 2003

Discussion:
If a PD will accept power via the PI, but is not powered via the PI, then it shall present a valid detection signature at the PI between the positive and negative V_{Port} pins for both Mode A and Mode B as defined in 33.3.1.

Test Setup:
Connect the PSE to the PD Simulator with a 1m length of Category 5 cable. Confirm that the PD under test is currently not powered via the PI but will accept power via the PI.

Procedure:
For Setup # 1:
1.   Refer to the figure 33C.19. Close only switch S1 to measure the current for the V-I slope.
2.   Limit the current of V_N between 4 to 5 mA.
3.   Vary V_N from 2.7V to 10.1V in steps of 1V and measure I_N for each V_N.
4.   Calculate $Rsig_N =(V_{N+1} -V_N)/(I_{N+1} - I_N)$.
5.   Calculate the voltage offset by calculating the intersection of the line between the (V_N, I_N) and $(V_{N+1,} I_{N+1})$ data points and V/I axis. (Refer to Figure 33C.20)
6.   Calculate the current offset by calculating the intersection of the line between the (V_N, I_N) and $(V_{N+1,} I_{N+1})$ data points and V/I axis. (Refer to Figure 33C.20)
For Setup #2:
1. Refer to the figure 33C.19. Open S1 and close S2 to measure the Input capacitance of the PD. Connect the inductance meter in series with the current source.
2. Activate the constant current source of 100μA by closing S2.Calculate the capacitance by ramping up the capacitance voltage with a constant current source. Use I*t=V*C to calculate the capacitance. This method is useful when series diodes are present.
3. Calculate the port capacitance (Cpd) by measuring the port resistance (Rpd) and using it in a typical differential equation solution.
4. Measure the inductance using the inductance meter.

Observable Results:

For Setup #1

    a. In step 3 verify that 23.5 KΩ<= Rsig$_N$<=26.25KΩ

    b. In step 4 verify that voltage offset is less than 1.9V.

    c. In step 5 verify that current offset is less than 10µA.

For Setup #2

    a. In step 2 calculate Cpd and verify that 50nF<=Cpd<=130nF.

    b. In step 3 the input inductance should be less than 100µA.

Possible Problems: None

Test # Non- valid PD detection signature characteristics

Purpose: Verify non-valid PD detection signature characteristics measured at PD input connector.

Reference:
 [1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.3.3, Annex 33C.4, Figure 33C.19, 33C.20, 33C.21, Table 33-9

Resource Requirements:
- PSE Simulator
- Current meter

Last Modification: March 4, 2003

Discussion:
There are two cases when a PD should present a non-valid detection signature when attached to the PSE via the PI. The first case is while a PD is in a state where it will not accept power via the PI. The second case is when a PD becomes powered via the PI, and it must present a non-valid detection signature on the set of pairs from which is it not drawing power.

Test Setup:
Connect the PSE to the PD Simulator with a 1m length of Category 5 cable. Confirm that the PD under test is either powered via the PI or is in a state where it will not accept power via PI. Refer to the figure 33C.19.

Procedure:
V-I Slope
1.   Close only switch S1 to measure the current for the V-I slope.
2.   Limit the current of V_N between 4 to 5 mA.
3.   Vary V_N from 2.70V to 10.1V in steps of 1V and measure I_N for each V_N.
4.   Calculate $Rsig_N = (V_{N+1} - V_N)/(I_{N+1} - I_N)$.
5.   Vary V_N from 0.00V to 2.7V in steps of 0.20V and measure I_N for each V_N.
6.   Repeat step 3.

Input Capacitance
7.   Open S1 and close S2 to measure the Input capacitance of the PD.
8.   Activate the constant current source of 100μA by closing S2. Ignore any data points above 10.1V.
9.   Calculate the capacitance by ramping up the capacitance voltage with a constant current source. Use I*t=V*C to calculate the capacitance. This method is useful when series diodes are present.
10.   Calculate the port capacitance (Cpd) by measuring the port resistance (Rpd) and using it in a typical differential equation solution.

Observable Results:

a.   In step 4 verify that 12 KΩ> Rsig$_N$ or Rsig$_N$>45KΩ.

b.   In step 9 calculate Cpd and verify that 10μF<Cpd.

Possible Problems: None

Test # PD Classification signature characteristics

Purpose: Verify PD classification signature characteristics, measured at PD input connector.

Reference:
 [1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Sections 33.3.4, Table 33-10, Table 33-11, and, Annex 33C.4, Figure 33C.19

Resource Requirements:
*   PSE Simulator
*   Current meter
*   Oscilloscope

Last Modification: March 4, 2003

Discussion:
The purpose of PD classification is to provide the PSE information about the maximum power that the PD will draw across all input voltages and operational modes. A PD should present one and only classification signature during classification. A PD that does not support classification will be classified as Class 0 by default. The PD that provides a valid classification signature characteristic will be classified as Class 1-3.

Test Setup: Refer to the setup illustrated in Figure 33C.19.

Procedure:
1.   Set switch S1 ON and S2 OFF.
2.   Vary the Voltage V_N from 15V to 20V.
3.   Measure the corresponding I_N.
4.   Confirm that the PD provided the required classification signature within $T_{Class.}$
5.   Apply voltage in the range V_{Port} higher than $V_{ON.}$
6.   Measure the current drawn by the PD.

Observable Results:

a. If the PD does not support classification, then it must not draw more power than that specified in Table 33-10.
b. For step 3 the characteristics of the PD should abide by those specified in Table 33-11.
c. For Step 6 the power drawn by the PD should abide by those specified in Table 33-10.

Possible Problems: None

GROUP 4: Test Suites Related to Management Functions

Scope: The following tests cover parametric tests specific to Manaagement functions that a PSE or PD might support.

Overview: These tests are designed to identify problems that IEEE Draft P802.3af/ D4.1compliant devices may have in establishing link and exchanging packets with each other.

Test #XX: Detection Status

Purpose: To verify that the DUT properly sets the value of bits 12.3:1 to reflect the current state of the PD Detection function.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: subclause 33.6.1.2.9, Table 33-16

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: The PSE indicates to management the current state of the PD Detection function by writing to bits 12.3:1

Bit(s)	Name	Description	Type

Test Setup: Connect the DUT to the PD simulator and the Line Monitor

Procedure:
1. Disable the PSE function (write a zero to bit 11.0) and read the value of bits 12.3:1.
2. Enable the PSE function (write a one to bit 11.0) and read the value of bits 12.3:1.
3. Enable PD Detection test mode by writing a value of one to bit 11.4.
4. Present the DUT with a valid detection signature at the PI and allow it to detect, optionally classify, and supply power to the PD.
5. Monitor the link segment.
6. Read the value of bits 12.3:1.
7. Enable normal PD Detection by writing a zero to bit 11.4.
8. Present the DUT with a valid detection signature at the PI and allow it to detect the PD.
9. Before power is applied to the PI, read the value of bits 12.3:1.
10. Once power has been applied onto the PI, read the value of bits 11.3:1.
11. Read the value of bits 12.3:1.
12. If the DUT supports the indication of a fault condition, then cause the DUT to indicate a fault condition by any means, else this test cannot be performed.
13. Read the value of bits12.3:1
14. Attempt to write a value to bits 12.3:1.

Observable Results:

- When PSE functionality has been disabled, in step 1 the value of bits 11.3:2 should reflect '000b'.
- When PSE functionality has been enabled and the PSE is searching for a PD, in step 2 the value of bits 12.3:2 should reflect '001b'.
- In step 6, once the PSE has successfully detected, classified, and is supplying power to a PD, bits 12.3:2 should read as '010b'.
- When the detection function is normal and the DUT has detected a PD, but the PSE is not supplying power, in step 8 bits 12.3:2 should correspond to '010b'.
- Upon successful detection and application of power onto the PI, the value of bits 12.3:2 should reflect '011b' in step 9.
- In step 13, the value of bits 12.3:2 should read '011b' once PD detection has detected a fault.
- In step 14, the DUT should ignore any attempt to write to bits 12.3:2.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #XX: Detection Test Control

Purpose: To verify that bit 11.4 controls the mode of operation of the PD Detection function

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: subclause 33.6.1.2.5, Table 33-18

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: When management has disabled the PSE Function it has the ability to control the current mode of operation of the PD Detection function through the PSE Control Register (Register 12) by writing to bit 11.4. A value of '0' allows the PD Detection function to operate normally. A value of '1' places the PD in a test mode that allows the PD Detection function to operate normally with the exception that power should not be supplied to a detected PD, and power should be removed from a PD that has already been detected.

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:
15.   Via management access, read the default value of MII/GMII Register 11 bit 4.
16.   If necessary, write a value of zero to bit 11.4 to force the PD detection function to operate normally.
17.   Present the DUT with a valid detection signature at the PI and allow the DUT to detect, optionally classify, and apply power to the link.
18.   Monitor the link segment.
19.   Write a value of one to bit 11.4 to place the PD Detection function in test mode.
20.   Monitor the link segment.
21.   Restart PD Detection and present the DUT with a valid detection signature at the PI.
22.   Monitor the link segment.

Observable Results:
- In step 4, the DUT may supply power once a valid PD has been detected.
- If the DUT applied power onto the PI in step 4, power should be removed before the expiration of the PD Maintain Power Signature dropout time limit once a value of one has been written to bit 11.4.
- Once bit 11.4 has been set and PD detection has been restarted, the DUT should properly detect and classify the PD (optional), however, power should not be applied onto the PI.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #XX: Force Power Test Control

Purpose: To verify that bit 11.1 controls the enabling/disabling of power being applied onto the PI without detection.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.6.1.1.4, Table 33-17

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: Management has the ability to enable a test mode to force power onto the PI without regard to detection of a PD by setting bit 11.0 to zero and setting bit 11.1 to one in the PSE Control register (Register 11). Likewise, setting bit 11.0 to zero puts the PSE into normal operation where detection mode controls the sourcing of power.

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:
Part a
1. Via management access, read the default value of MII/GMII Register 11 bit 1.

Part b
1. Disable PSE functions by writing a value of zero to bit 11.0.
2. Write a value of one to bit 11.1 and monitor the link segment.

Part c
1. Repeat step 2, changing the value written to zero.

Part d
1. Enable PSE functions by writing a value of one to bit 11.0.
2. Write a value of one to bit 11.1 and monitor the link segment.

Observable Results:
- The default value of bit 11.1 should be zero.
- When PSE functions have been disabled and bit 11.1 is set, power should be applied onto the PI.
- When PSE functions have been disabled and bit 11.1 is not set, power should be removed from the PI.

- When PSE functions are enabled, management should ignore the value of bit 11.1 and only apply power onto the PI after a PD is detected.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #XX: MPSabsent

Purpose: To verify that the DUT sets bit 12.7 upon reception of an MPS absent condition.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.6.1.2.3, Table 33-18

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: Management is made aware that an MPS absent condition has occurred by reading bit 12.7 of the PSE/PD Status register (Register 12). Upon receiving such a condition, the DUT must set this bit. A value of '1' means that an MPSabsent condition has been detected, while a value of '0' indicates that an MPSabsent condition has not been detected. An MPSabsent condition is detected when either or both elements of the Maintain Power Signature are absent for a duration greater than the PD Maintain Power Signature dropout time limit. The MPSabsent bit should reset upon a read to the PSE/PD Status register.

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:
DC Current
1. Present the DUT with a valid detection signature at the PI and allow the DUT to detect, optionally classify, and apply power to the link.
2. Adjust the load being powered by the PSE to draw current ≤ 5 mA for a duration >400 ms such that an MPSabsent condition occurs.
3. Read the PSE/PD Status register (Register 12).
4. Remove the MPSabsent condition and read the PSE/PD Status register again.

AC Impedance
5. Repeat step 1.
6. Adjust the AC impedance of the load >1980 kΩ for a duration >400 ms.
7. Read the PSE/PD Status register (Register 12).
8. Remove the MPSabsent condition and read the PSE/PD Status register again.
9. Attempt to write a value to bit 12.7.

Observable Results:
- Bit 12.7 should be set to one the first time the PSE/PD Status register is read, and set to zero the second time the register is read.
- The DUT should reject any attempt to write to bit 12.7.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #XX: Overcurrent

Purpose: To verify that the DUT sets bit 12.8 upon reception of an overcurrent condition.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.6.1.2.2, Table 33-18

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: Management is made aware that an overcurrent condition has occurred by reading bit 12.8 of the PSE/PD Status register (Register 12). Upon receiving such a condition, the DUT must set this bit. A value of '1' means that an overcurrent condition has been detected, while a value of '0' indicates that an overccurent condition has not been detected. An overcurrent condition occurs when the current drawn from the PSE at the PI is greater than the overload current limit for duration greater than the overload time limit. The Overcurrent bit should reset upon a read to the PSE/PD Status register.

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:

10. Present the DUT with a valid detection signature at the PI and allow the DUT to detect, optionally classify, and apply power to the link.
11. Adjust the load being powered by the PSE to draw current ≥400 mA for a duration >500 ms such that an overcurrent condition occurs.
12. Read the PSE/PD Status register (Register 12).
13. Remove the overcurrent condition and read the PSE/PD Status register again.
14. Attempt to write a value to bit 12.8.

Observable Results:
- Bit 12.8 should be set to one the first time the PSE/PD Status register is read, and set to zero the second time the register is read.
- The DUT should reject any attempt to write to bit 12.8.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #33.1.1: Pair Control

Purpose: To verify that the DUT sets bits 11.3:2 to properly reflect the supported PSE Pinout Alternative.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.6.1.1.3, Table 33-17

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: After a valid detection and optional classification of a PD, a PSE that has chosen to apply power to the link must do so using either Alternative A, or Alternative B, or both, and must report the supported pinout to management via bits 11.3:2 of the PSE Control register (Register 11). Additionally, implemented pinout alternatives are constrained by the location of the PSE with respect to the link segment. An Endpoint PSE may support either Alternative A or B, or both; Midspan PSEs must use only Alternative B. Optionally, if the PSE indicates support for Pair Control Ability through bit 12.0, the PSE Pinout Alternative may be controlled through these bits.

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:
Part a:
    23.   Via management access, read the default value of MII/GMII Register 11 bits 3-2.

Part b:
    24.   Present the DUT with a valid detection signature at the PI and allow the DUT to detect, optionally classify, and apply power to the link.
    25.   Monitor the link segment.
    26.   Via management, access and read the value of bits 11.3:2.

Part c:
    27.   If Pair Control Ability is set (bit 12.0 set to one), write a value of '10b' to bits 11.3:2.
    28.   Repeat steps 2 through 4.
    29.   Repeat steps 5 & 6 changing the value written to '01b'.
    30.   Repeat steps 5 & 6 changing the value written to '00b'.
    31.   Repeat steps 5 & 6 changing the value written to '11b'.

Part d:

32.　　　　If Pair Control Ability is not set (bit 12.0 set to zero), attempt to write a value of '11b' to bits 11.3:2.

33.　　　　Repeat step 10, changing the value written to '00b'.

Observable Results:

a. The default value of bits 11.3:2 should be either '01b' or '10b'.

b. The value contained in bits 11.3:2 should reflect the Pinout Alternative supported by the DUT and correspond to the pair the DUT applied power to in step 4.

c. If pair Control Ability is supported by the DUT, the pair that power is applied to should correspond to the values written in bits 11.3:2. The DUT should not accept a write to a reserved pair combination.

d. When bit 12.0 is set to zero, the DUT should ignore any write to bits 11.3:2 and should report the supported Pinout Alternative.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #XX: Pair Control Ability

Purpose: To verify that the DUT sets bit 12.0 if it is capable of controlling which PSE Pinout Alternative is used for PD detection and power.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: A PSE that supports controlling the supported PSE Pinout Alternative must indicate this capability to management by setting bit 12.0 in the PSE/PD Status register (Register 12). A value of '1' means that the PSE supports the option to control which PSE Pinout Alternative is used during the detection and power of a PD through the Pair Control bits. A value of '0' indicates the PSE does not support control of the PSE Pinout Alternative used for PD detection and power through the Pair Control bits. When pair control is not available, the PSE should report the supported PSE Pinout Alternative statically through the Pair Control bits.

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:
34.	Via management access, read the value of MII/GMII Register 12 bit 0.
35.	Write a value of '01b' to bits 11.3:2.
36.	Present the DUT with a valid detection signature at the PI and allow the DUT to detect, optionally classify, and apply power to the link.
37.	Monitor the link segment.
38.	Attempt to write any value to bit 12.0.

Observable Results:
- If the value of bit 12.0 in step 1 was one then the pairs powered in step 4 should correspond to value written to bits 11.3:2. Otherwise, if bit 12.0 in step 1 was zero then writing to bits 11.3:2 should have been ignored and not affected the pairs that power was applied to in step 4.
- The DUT should reject any attempt to write to bit 12.0.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #XX: PD Class

Purpose: To verify that the DUT sets bits 12.6:4 according to Table 33-18 based upon the PD Class of a detected PD.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.6.1.2.4, Table 33-18

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: A PSE that supports classification of PDs must accurately detect and classify the PD in Class 1, 2, 3, or 4 before applying power to the link segment. The detected PD Class is then related to management via bits 12.6:4 of the PSE/PD Status register (Register 12).

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:
Part a
Measurent Current Method
1. Present the DUT with a valid detection signature at the PI.
2. Provide a classification signature with current characteristics of a Class 0 load.
3. Read the value of bits 12.6:4.
4. Disconnect the load for a duration greater than 975 ms.
5. Repeat steps 1 through 4 changing the classification signature to that of a Class 1 load.
6. Repeat steps 1 through 4 changing the classification signature to that of a Class 2 load.
7. Repeat steps 1 through 4 changing the classification signature to that of a Class 3 load.
8. Repeat steps 1 through 4 changing the classification signature to that of a Class 4 load.

Measured Voltage Method
1. Present the DUT with a valid detection signature at the PI.
2. Provide a classification signature with voltage characteristics of a Class 0 load.
3. Read the value of bits 12.6:4.
4. Disconnect the load for a duration greater than 975 ms.
5. Repeat steps 9 through 12 changing the classification signature to that of a Class 1 load.
6. Repeat steps 9 through 12 changing the classification signature to that of a Class 2 load.
7. Repeat steps 9 through 12 changing the classification signature to that of a Class 3 load.
8. Repeat steps 9 through 12 changing the classification signature to that of a Class 4 load.

Part b
1. Attempt to write a value to bits 12.6:4

Observable Results:
- Bits 12.6:4 should correspond to the PD Class of the detected PD.
- The DUT should reject any attempt to write to bits 12.6:4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #XX: PSE Enable

Purpose: To verify that bit 11.0 controls the enabling/disabling of the PSE function.

References:
- IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.6.1.1.5, Table 33-17

Resource Requirements:
- PD simulator – A system capable of generating a valid detection signature at the PI when probed by a PSE during PD Detection, and providing a valid Maintain Power Signature once power has been applied onto the PI.
- Line Monitor – A system capable of monitoring the link segment at the PI during the detection, classification, and powering of a PD.

Last Modification: March 4, 2003

Discussion: Management has the ability to enable the PSE function through the PSE Control register (Register 11) by setting bit 11.0 to one and to disable the PSE function by setting bit 11.0 to zero. If management has set bit 11.0 to zero, then the DUT should function as if no PSE function was present, and power may be applied using bit 11.1 (Force Power Test Control). When bit 11.0 is set to one, the DUT may provide power onto the PI only if a valid PD is detected.

Test Setup: Connect the DUT to the PD simulator and the Line Monitor.

Procedure:
Part a
1. Via management access, read the default value of MII/GMII Register 11 bit 0.

Part b
1. If necessary, enable the PSE function by writing a value of one to bit 11.0.
2. Present the DUT with a valid detection signature at the PI and allow the DUT to detect, optionally classify, and apply power to the link.
3. Monitor the link segment.

Part c
1. Disable the PSE function by writing a value of zero to bit 11.0, and ensure the DUT is functioning in normal operation by setting bit 11.1 to zero.
2. Monitor the link segment.

Part d
1. With bit 11.0 still set to zero, repeat steps 3 & 4.

Observable Results:
- The default value of bit 11.0 should be one.
- When the DUT has detected a valid PD it may or may not apply power onto the PI.

- When bit 11.0 is set to zero and the DUT is in normal operation, power should not be applied onto the PI.
- When bit 11.0 is set to zero, the DUT should function as if it had no PSE function.

Possible Problems: If management access is not provided, then this test cannot be performed.

APPENDIX A: PACKET ERROR RATIO SPECIFICATIONS

Table A-1 Constrained Packet Error Ratio Verification

Technology	BER	# of Transmitted Packets[a]	
		64-byte	1518-byte
10BASE-T	$10E^{-8}$	468,000	19,700
100BASE-TX	$10E^{-8}$	468,000	19,700
1000BASE-T	$10E^{-9}$	4,680,000	197,000

[a]The number of transmitted packets outlined in Table A-1 will insure the listed bit error ratio with 95% accuracy. Due to time constraints of the testing period the IOL has chosen to limit the number of packets transmitted in a given test, and therefore, may not be verifying the true bit error ratio for a given technology. The results obtained from this testing process should therefore not be seen as a true measure of the bit error ratio, but as information that may suggest the need for further analysis.

Category-5 Cable Test Environment

Since equalizers often tend to be optimized for particular cable conditions the test procedure uses both high attenuation and a low attenuation environment. The high attenuation testing is done over a Category-5 compliant channel attenuated to simulate a worst-case environment equivalent of 60 degrees (Refer to Table A-2). The low attenuation testing is done over a Category-5 compliant channel specified in Table A-2. Each of these channels must be tested to ensure that they meet the expected characteristics as defined by their associated standards.

Table A-2 UTP Channel Definitions

Technology	Media Type	Insertion Loss – Low (+/- 1 dB)[a]			Insertion Loss – High (+/- 1 dB)[a]		
		16 MHz	32 Mhz	100 Mhz	16 MHz	32 MHz	100 MHz
100BASE-TX	Category-5 UTP	9.9	14.2	25.7	0.6	1.0	1.2
1000BASE-T	Category-5 UTP	9.9	14.2	25.7	0.6	1.0	1.2

[a]Insertion loss is the sum of channel attenuation and connector losses.

Optical Test Environment

For optical devices, the high attenuation testing is performed over a compliant optical channel where the signal is attenuated using an optical fiber attenuator to the minimum TX Link Up value for the DUT. The low attenuation testing is done over a compliant optical channel and the signal is not attenuated. A summary of the optical channel definitions is provided in **Error! Reference source not found.**.