Power Over Ethernet

Clause 33 PD
Parametric Test Suite
Version 1.5

Technical Document

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MODIFICATION RECORD

- October 8, 2004 – Version 1.5
  Sean LaPierre: Added test 33.1.9 *Ripple and Noise Operation*
- July 19, 2004 – Version 1.4
  Jeremy Kent: Extracted part b from test 33.1.5 *Classification Signature Characteristics* and created tests 33.1.6 *Input Average Power*, and test 33.1.7 *Backfeed Voltage*; subsequent tests were renumbered appropriately.
- December 22, 2003 - Version 1.3
  Jeremy Kent: Removed Test 33.1.2 Part B; Modified test procedures where necessary to reflect current implementation(s).
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  Veena Venugopal
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  Veena Venugopal
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INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functionality of their IEEE Std. 802.3af based products. The tests do not determine if a product conforms to the IEEE Std. 802.3af standard, nor are they purely interoperability tests. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other Power over Ethernet capable devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in many Power over Ethernet environments.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross-references to the IEEE Std. 802.3af standard and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup
The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure
The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results
The observable results section lists specific items that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable result, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable result.

Possible Problems
This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

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GROUP 1: PARAMETRIC TESTING

Scope: The following tests cover parametric tests specific to Powered Devices (PDs) that support 10BASE-T, 100BASE-TX, and 1000BASE-T devices.

Overview: The following group of tests pertains to the determination of various parametric values as defined in IEEE Std. 802.3af/D4.3. Note, successfully passing these tests, or failing these tests does not necessarily indicate that the DUT will, or will not, be interoperable. Devices that pass these tests are more inclined to be interoperable with, not only existing products, but also all future standard compliant devices.

Test #33.1.1: Source Power

Purpose: To verify that DUT does not source power on its power interface (PI).

Reference:
[1] IEEE Std 802.3af, 2003 Edition: Subclause 33.3.1, Table 33-7, Figure 33-5.

Resource Requirements:
- Voltmeter

Last Modification: June 5, 2003

Discussion: A device that is either drawing power or requesting power from PSE should not be capable of sourcing power on either of the two sets of PI conductors at any time.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the voltmeter, and the negative V_{port} pins to the negative terminal of the volt meter.

Procedure:
1. Measure V_{Port} at the PI of the DUT using a voltmeter.
2. Verify that there is no power present at the PI.

Observable Results:
a. The DUT should not source power onto the PI at any time.

Possible Problem: None

Test #33.1.2: PD Pinout

Purpose: To verify that the DUT is insensitive to the polarity of the power supply and is able to operate in either Mode A or Mode B.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: subclause 33.3.1, Figure 33-5, Table 33-7

Resource Requirements

- Power Supply

Last Modification: December 22, 2003

Discussion: After detection and optional classification, a PSE may supply power on either set of the four wire pairs, hence the PD must support drawing its power from both Mode A and Mode B regardless of the polarity of the power supply.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:

1. Apply power over the range of 0.44 to 12.95 W onto the PI using Alternative A MDI.
2. Observe the operational status of the DUT
3. Repeat steps 1 and 2, however, applying power on Mode A MDI-X, Mode B MDI, and Mode B MDI-X.

Observable Results:

a. In all cases the DUT should accept the applied power and become operational once the requested power has been supplied.

Test #33.1.3: Valid Detection Signature Characteristics

Purpose: To verify that the DUT presents a valid detection signature while it is requesting power on the power interface (PI).

References:

[1] IEEE Std 802.3af, 2003 Edition: Section 33.3.3, Annex 33C.4, 33C.20, Figure 33C.19, Table 33-8

Resource Requirements:

- Power Supply
- Voltage meter
- Current meter

Last Modification: May 3, 2004

Discussion: If a PD will accept power, but is not powered, via the PI then it should present a valid detection signature at the PI between the positive and negative V_{Port} pins for both pinout Modes such that the attached PSE will properly detect the PD's request for power. The standard defines the signature to be comprised of five characteristics: a valid resistance, capacitance, and inductance; and either a voltage offset or a current offset. The voltage offset limit was specified to allow for the inherent voltage offset for two series diode drops. Similarly, the current limit allows for internal FET leakage. Given the minimum and maximum limits on the defined resistive slope, there are no minimum bounds for the offset components as a maximum current implies a minimum voltage, and vice versa. Figure 33C.20 of Annex C in Clause 33, reproduced below, illustrate the signature resistance and voltage offsets.

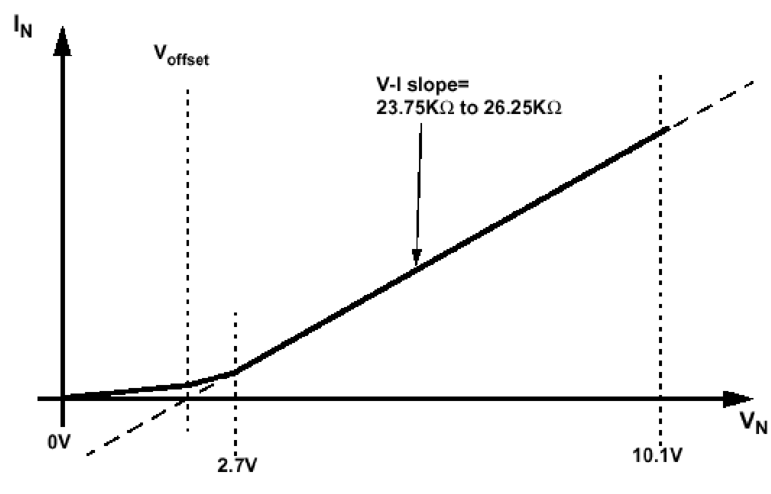

Figure 33C.20—Signature voltage offset

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:

1. Limit the power supply current between 4 to 5 mA.
2. Applying voltage using Alternative A, vary the power supply voltage, V_N, from 0.0 V to 3.0 V in steps of 50 mV and measure the corresponding current, I_N, drawn by the DUT.
3. Vary the power supply voltage, V_N, from 3.2 V to 10.2 V in steps of 200 mV and measure the corresponding current, I_N, drawn by the DUT.
4. Calculate R_{sigN} using a 1 V chord between measurement points.
5. Determine either the voltage offset or the current offset by calculating the intersection of the line between the ($V_{N,}$ I_N) and ($V_{N+1,}$ I_{N+1}) data points and V/I axis.
6. Repeat steps 1-5, however, connect the DUT to accept power on Mode B

Observable Results:

a. In step 4 the observed signature resistance should be between 23.75 KΩ and 26.25KΩ (inclusive)
b. In step 5 the DUT should have either a voltage offset less than or equal to 1.9 V, or a current offset less than 10 μA.

Possible Problems: None

Test #33.1.4: Non- valid Detection Signature Characteristics

Purpose: To verify that the DUT presents a non-valid detection signature while it is not requesting power, or once powered, at the power interface (PI) of the non-powered pairs.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: Subclause 33.3.3, Annex 33C.4, 33C.20, Figure 33C.19, Table 33-9

Resource Requirements:

- Power Supply
- Voltage meter
- Current meter

Last Modification: May 3, 2004

Discussion: There are two cases when a PD should present a non-valid detection signature when attached to the PSE via the PI. The first case is while a PD is in a state where it will not accept power via the PI. The second case occurs once a PD becomes powered via the PI, and it must present a non-valid detection signature on the set of pairs from which is it not drawing power.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:

Part a: Resistance

1. Limit the power supply current between 4 to 5 mA.
2. Apply power onto the PI using Alternative A, and confirm the DUT is drawing power via the PI.
3. Applying voltage to the non-powered pairs, vary the power supply voltage, V_N, from 0.0 V to 3.0 V in steps of 50 mV and measure the corresponding current, I_N, drawn by the DUT.
4. Vary the power supply voltage, V_N, from 3.2 V to 10.2 V in steps of 200 mV and measure the corresponding current, I_N, drawn by the DUT.
5. Calculate R_{sigN} using a 1 V chord between measurement points.
6. Repeat steps 1-5; however, connect the DUT to accept power on Mode B.

Observable Results:

a. In step 5 verify that $Rsig_N < 12$ KΩ or $Rsig_N > 45$ KΩ.

Possible Problems: None

Test #33.1.5: Classification Signature Characteristics

Purpose: To verify that the DUT provides proper information about its maximum power requirements, and that those requirements fall within the acceptable range.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: subclause 33.3.4, and Table 33-11

Resource Requirements:

- Power Supply
- Voltage meter
- Current meter

Last Modification: May 7, 2004

Discussion: The purpose of PD classification is to provide the PSE information about the maximum power that the PD will draw across all input voltages and operational modes. A PD should present one and only one classification signature during classification. By default, a PD is Class 0; however, to improve power management for the PSE, a PD may provide a signature for Class 1 to 3, which are outlined in table 33-11.

Table 33-11 - Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5 V to 20.5 V	0	4	mA
Current for Class 1	14.5 V to 20.5 V	9	12	mA
Current for Class 2	14.5 V to 20.5 V	17	20	mA
Current for Class 3	14.5 V to 20.5 V	26	30	mA
Current for Class 4	14.5 V to 20.5 V	36	44	mA

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply.

Procedure:

1. Apply power onto the PI using Alternative A, varying the power supply voltage from 12.5V to 22.5V.
2. Measure the corresponding current drawn by the DUT.
3. Repeat steps 1-2, however, connect the DUT to accept power on Mode B.

Observable Results:

a. In step 2 the current drawn by the DUT for each supported class should be within the range (inclusive) specified in table 33-11.
b. The DUT should only present one classification signature during classification.

Possible Problems: None

Test #33.1.6: Input Average Power

Purpose: To verify that the DUT will turn on once power has been applied to the power interface (PI), will remain on over the entire port voltage range, and turn off once power is removed.

Reference:
[1] IEEE Std 802.3af, 2003 Edition: subclause 33.5.1, 33.5.7, Table 33-10.

Resource Requirements:
- Power Supply
- Current meter

Last Modification: May 7, 2003

Discussion: For a PD that supports classification, the maximum power that the PD may draw across all input voltages and operational modes is governed by the limits specified in table 33-10.

Table 33-10 - PD Power classification

Class	Usage	Range of maximum power used by the PD
0	Default	0.44 to 12.95 Watts
1	Optional	0.44 to 3.84 Watts
2	Optional	3.84 to 6.49 Watts
3	Optional	6.49 to 12.95 Watts
4	Not Allowed	Reserved for Future Use

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply through a 20Ω series resistance.

Procedure:
1. If possible, configure the DUT for desired Class operation.
2. Apply a port voltage of 44 V onto the PI using Alternative A.
3. Measure the current drawn by the DUT and calculate the input power averaged over a 1 second period.
4. Repeat steps 1-2, however, apply power using Alternative B and a port voltage of 57 V.
5. Repeat steps 1-3 for all supported classes.

Observable Results:
a. The maximum power drawn by the DUT for each supported class should be within the range (inclusive) specified in table 33-10.

Test #33.1.7: Backfeed Voltage

Purpose: To verify that the backfeed voltage measured across the non-powered power interface (PI) conductors of the DUT falls within the conformance limits.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: subclause 33.3.5.10, Table 33-12.

Resource Requirements:

- Power Supply
- Voltage meter

Last Modification: May 5, 2003

Discussion: When the maximum port voltage is applied across the PI for a given Mode, the voltage measured across the PI, regardless of polarity, for the opposite Mode with a 100 kΩ load resistor connected must be less than 2.8 V, the backfeed voltage (V_{bfd}) limit specified in the PD power supply limits of table 33-12.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply. Connect the Mode B positive V_{port} pins of the DUT to the positive terminal of the voltage meter, and the negative V_{port} pins to the negative terminal of the voltage meter with a 100 kΩ load connected.

Procedure:

1. Apply 57 V across the PI using Alternative A MDI.
2. Measure the voltage across the PI for Mode B.
3. Repeat steps 1-2, however, apply power using Alternative A MDI-X
4. Repeat steps 1-3, however, apply power using Alternative B MDI and measure V_{bfd} across the PI for Mode A.

Observable Results:

a. In all cases, the measured voltage should not exceed 2.8 V.

Test #33.1.8: Power Supply Turn On / Off

Purpose: To verify that the DUT will turn on once power has been applied to the power interface (PI), will remain on over the entire port voltage range, and turn off once power is removed.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: subclause 33.5.1, 33.5.7, Table 33-12.

Resource Requirements:

- Power Supply
- Current meter

Last Modification: May 3, 2003

Discussion: After startup, a PD is required to turn on its power supply before the input voltage (V_{port}) level reaches 42 V. Once turned on, the power supply then must remain on over the entire range of V_{port}, which is specified from 36 V to 57 V, as the attached PSE may vary the applied voltage on the PI over this range at any time. If the minimum value of V_{port} is not maintained by the PSE, the PD must turn off before the input voltage level reaches 30 V.

Test Setup: Connect the Mode A positive V_{port} pins of the DUT to the positive terminal of the power supply, and the negative V_{port} pins to the negative terminal of the power supply through a 20Ω series resistance.

Procedure:

1. Apply 42 V across the PI.
2. Observe the operational status of the DUT
3. Repeat steps 1 and 2, however, increment the applied voltage by 1 V until the DUT has become fully operational.
4. Once operational, increase the applied voltage to 57 V in 1 V increments, and then decrease the voltage to 36 V.
5. Observe the operational status of the DUT.
6. Decrease the applied voltage by 1 V
7. Observe the status of the DUT
8. Repeat steps 6 and 7 until the DUT turns off
9. Repeat steps 1-8, however, connect the DUT to accept power on Mode B.

Observable Results:

a. The DUT should become fully operational at a port voltage less than 42 V.
b. Once the DUT has turned on, it should remain operational for port voltages between 36 V and 57 V.
c. The DUT should turn off at a port voltage greater than 30V and less than 36 V.

Test #33.1.9: Ripple and Noise Operation

Purpose: To verify that DUT operates properly when noise is applied to the PI, for all operating voltages.

Reference:
[1] IEEE Std 802.3af, 2003 Edition: Subclause 33.5.6, Table 33-7, Table 33-12.

Resource Requirements:
- Power Supply
- Arbitrary Waveform Generator
- Noise Injection Circuit

Last Modification: Sept 2, 2003

Discussion: The DUT must maintain proper operation in the presence of noise from the PSE over the entire range of operating voltages. The ripple and noise is specified by table 33-12 item 7:

Table 33-12 – PD Power Supply Limits

Item	Parameter	Symbol	Unit	Min	Max
7	Ripple and noise, < 500Hz		V_{PP}		0.5
	Ripple and noise, 500Hz to 150KHz		V_{PP}		0.2
	Ripple and noise, 150KHz to 500KHz		V_{PP}		0.15
	Ripple and noise, 500KHz to 1MHz		V_{PP}		0.1

Test Setup: Connect the DUT, AWG and power supply to the noise injection circuit.

Procedure:
1. Set the waveform generator to have a sinusoidal waveform with V_{PP} set to 0.50V and a frequency of 10Hz.
2. Observe the operational status of the DUT.
3. Repeat steps 1 and 2, over the range of frequencies from 10Hz to 500Hz.
4. Repeat steps 1 through 3 with V_{PP} set to 0.20V over the frequency range of 501Hz to 150KHz.
5. Repeat steps 1 through 3 with V_{PP} set to 0.15V over the frequency range of 151KHz to 500KHz.
6. Repeat steps 1 through 3 with V_{PP} set to 0.10V over the frequency range of 501KHz to 1MHz.

Observable Results:
a. The DUT should operate correctly under the specified ripple and noise conditions over all operating voltages defined by Table 33-12.

Possible Problem: Current draw of PD might exceed capabilities of the injection circuit.