University of New Hampshire InterOperability Laboratory
Power Over Ethernet Consortium

Superseded

As of October 8, 2004 the Power Over Ethernet Consortium Clause 33 Powered Device Parametric Conformance Test Suite version 1.3 has been superseded by the release of the Clause 33 Powered Device Parametric Conformance Test Suite version 1.5. This document along with earlier versions, are available on the Power Over Ethernet Consortium test suite archive page.

Please refer to the following site for both current and superseded test suites:

http://www.iol.unh.edu/testsuites/ethernet/archive.html

Power Over Ethernet

Clause 33 PD
Parametric Test Suite

Technical Document

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MODIFICATION RECORD

- December 22, 2003 - Draft 1.3
  Jeremy Kent: Removed Test 33.1.2 Part B; Modified test procedures where necessary to reflect current implementation(s).
- April 16, 2003 - Draft 1.2
  Veena Venugopal
- March 3, 2003 - Draft 1.1
  Veena Venugopal
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Jeff Lapak	University of New Hampshire
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INTRODUCTION

Overview
The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functionality of their IEEE Std. 802.3af based products. The tests do not determine if a product conforms to the IEEE Std. 802.3af standard, nor are they purely interoperability tests. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other Power over Ethernet capable devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in many Power over Ethernet environments.

Organization of Tests
The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number
The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose
The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References
The references section lists cross-references to the IEEE Std. 802.3af standard and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements
The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification
This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure

The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

The observable results section lists specific items that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable result, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable result.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

TABLE OF CONTENTS

GROUP 1: PARAMETRIC TESTING

Scope: The following tests cover parametric tests specific to Powered Devices that support 10BASE-T, 100BASE-TX, and 1000BASE-T devices.

Overview: The following group of tests pertains to the determination of various parametric values as defined in IEEE Std. 802.3af/D4.3. Note, successfully passing these tests, or failing these tests does not necessarily indicate that the DUT will, or will not, be interoperable. Devices that pass these tests are more inclined to be interoperable with, not only existing products, but also all future standard compliant devices.

Test #33.1.1: Source Power

Purpose: To verify that DUT does not source power on its PI.

Reference:
[1] IEEE Std 802.3af, 2003 Edition: Subclause 33.3.1, Table 33-7, Figure 33-5.

Resource Requirements:
- Voltmeter

Last Modification: June 5, 2003

Discussion: A device that is either drawing power or requesting power from PSE should not be capable of sourcing power on either of the two sets of PI conductors at any time.

Test Setup: Connect the DUT to a voltmeter.

Procedure:
1. Measure V_{Port} at the PI of the DUT using a voltmeter.
2. Verify that there is no power present at the PI.

Observable Results:
a. The DUT should not source power onto the PI at any time.

Possible Problem: None

Test #33.1.2: PD Pinout

Purpose: To verify that the DUT is insensitive to the polarity of the power supply and is able to operate in either Mode A or Mode B.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: subclause 33.3.1, Figure 33-5, Table 33-7

Resource Requirements

- Voltage source
- PSE Simulator

Last Modification: December 22, 2003

Discussion: After detection and optional classification, a PSE may supply power on either set of the four wire pairs, hence the PD must support drawing its power from both Mode A and Mode B regardless of the polarity of the power supply.

Test Setup: Connect the DUT to the PSE Simulator with a 1m length of Category 5 cable.

Procedure:

1. Set the PSE simulator to supply between 0.44 and 12.95 W of power to Mode A MDI
2. Observe the operational status of the DUT
3. Repeat steps 1 and 2, however, applying power on Mode A MDI-X, Mode B MDI, and Mode B MDI-X.

Observable Results:

a. In all cases the DUT should accept the applied power and become operational once the requested power has been supplied.

Test #33.1.3: Valid PD Detection Signature Characteristics

Purpose: To verify that the DUT presents a valid detection signature while it is requesting power on the PI.

References:

[1] IEEE Std 802.3af, 2003 Edition: Section 33.3.3, Annex 33C.4, Figure 33C.19, 33C.20, 33C.21, Table 33-8

Resource Requirements:

- PSE Simulator
- Oscilloscope
- Current meter
- Inductance meter

Last Modification: December 22, 2003

Discussion: If a PD will accept power, but is not powered, via the PI then it should present a valid detection signature at the PI between the positive and negative V_{Port} pins for both pinout Modes such that the attached PSE will properly detect the PD's request for power. The standard defines the signature to be comprised of five characteristics: a valid resistance, capacitance, and inductance; and either a voltage offset or a current offset. The voltage offset limit was specified to allow for the inherent voltage offset for two series diode drops. Similarly, the current limit allows for internal FET leakage. Given the minimum and maximum limits on the defined resistive slope, there are no minimum bounds for the offset components as a maximum current implies a minimum voltage, and vice versa. Figure 33C.20 and 33C.21 of Annex C in Clause 33, reproduced below, illustrate the signature resistance, capacitance, and voltage offsets.

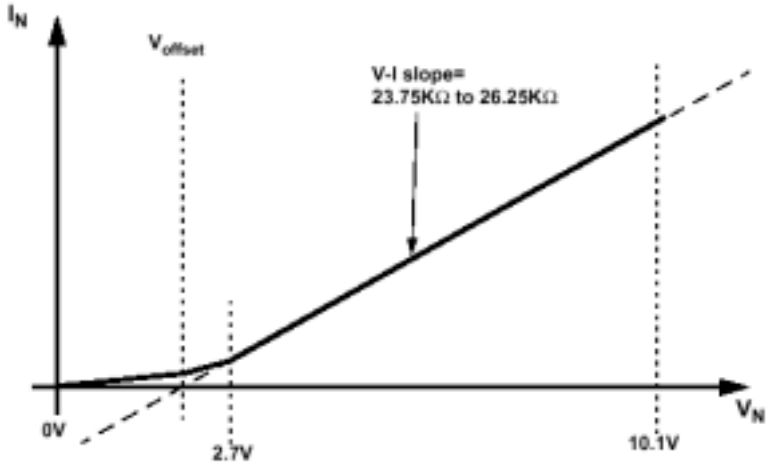

Figure 33C.20—Signature voltage offset

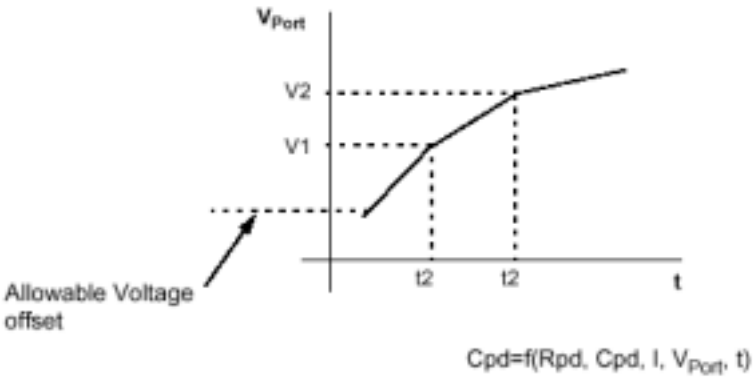

Figure 33C.21—Signature input capacitance

Test Setup: Connect the DUT to the PSE Simulator with a 1m length of Category 5 cable. Confirm that the PD under test is currently not powered, but will accept power via the PI.

Procedure:

Part a: Resistance

1. Limit the power supply current between 4 to 5 mA.
2. Applying voltage using Alternative A, vary the power supply voltage, V_N, from 0.00 V to 2.3 V in steps of 50 mV and measure the corresponding current, I_N, drawn by the DUT.
3. Vary the power supply voltage, V_N, from 3.2 V to 10.2 V in steps of 200 mV and measure the corresponding current, I_N, drawn by the DUT.
4. Calculate R_{sigN} using a 1 V chord between measurement points.
5. Determine either the voltage offset or the current offset by calculating the intersection of the line between the (V_N, I_N) and (V_{N+1}, I_{N+1}) data points and V/I axis.

Part b: Input Capacitance

6. Limit the current output of the power supply to 1A.
7. Supply 2.7 V, V_{port}, to the DUT.
8. Ramp the supply voltage to 3.7 V
9. Remove power from the link and measure the time duration, t, for V_{port} to drop from 57.0 V to 56.0 V.
10. Calculate the port capacitance using the equation $C = \frac{I_{Port} \times t}{V}$

Part c: Inductance

11. Measure the inductance using the inductance meter.
12. Repeat steps 1-12, however, applying voltage using Alternative B MDI

Observable Results:

a. In step 4 the observed signature resistance should be between 23.75 KΩ and 26.25KΩ (inclusive)
b. In step 5 the DUT should have either a voltage offset less than or equal to 1.9 V, or a current offset less than 10 μA.

c. In step 10 the observed signature capacitance of the DUT should be between 0.05 μF and 0.12 μF (inclusive).
d. In step 11 observed signature inductance should be less than or equal to 100 μH.

Possible Problems: None

Test #33.1.4: Non- valid PD Detection Signature Characteristics

Purpose: To verify that the DUT presents a non-valid detection signature while it is not requesting power, or once powered, at the PI of the non-powered pairs.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: Subclause 33.3.3, Annex 33C.4, Figure 33C.19, 33C.20, 33C.21, Table 33-9

Resource Requirements:

- PSE Simulator
- Current meter

Last Modification: December 22, 2003

Discussion:

There are two cases when a PD should present a non-valid detection signature when attached to the PSE via the PI. The first case is while a PD is in a state where it will not accept power via the PI. The second case occurs once a PD becomes powered via the PI, and it must present a non-valid detection signature on the set of pairs from which is it not drawing power.

Test Setup:

Connect the PSE to the PD Simulator with a 1m length of Category 5 cable.

Procedure:

Part a: Resistance

1. Apply power onto the PI using Alternative A, and confirm the DUT is drawing power via the PI.
2. Limit the power supply current between 4 to 5 mA.
3. Applying voltage to the non-powered pairs, vary the power supply voltage, V_N, from 0.00 V to 2.3 V in steps of 50 mV and measure the corresponding current, I_N, drawn by the DUT.
4. Vary the power supply voltage, V_N, from 3.2 V to 10.2 V in steps of 200 mV and measure the corresponding current, I_N, drawn by the DUT.
5. Calculate R_{sigN} using a 1 V chord between measurement points.

Part b: Input Capacitance

6. Limit the current output of the power supply to 1A.
7. Supply 2.7 V, V_{port}, to the DUT.
8. Ramp the supply voltage to 3.7 V
9. Remove power from the link and measure the time duration, t, for V_{port} to drop from 57.0 V to 56.0 V.
10. Calculate the port capacitance using the equation $C = \frac{I_{Port} \times t}{V}$
11. Repeat steps 1-10, however, apply power to Alternative B in step 1.
12. If possible, configure the DUT to not request power from the PI. Repeat steps 2-11.

Observable Results:

a. In step 5 verify that 12 KΩ> $Rsig_N$ or $Rsig_N$>45 KΩ.
b. In step 10 calculate C_{pd} and verify that 10μF<C_{pd}.

Possible Problems: None

Test #33.1.5: PD Classification Signature Characteristics

Purpose: To verify that the DUT provides proper information about its maximum power requirements, and that those requirements fall within the acceptable range.

Reference:

[1] IEEE Std 802.3af, 2003 Edition: subclause 33.3.4, Table 33-10, Table 33-11, and, Annex 33C.4, Figure 33C.19

Resource Requirements:

- PSE Simulator
- Current meter
- Oscilloscope

Last Modification: August 13, 2003

Discussion:

The purpose of PD classification is to provide the PSE information about the maximum power that the PD will draw across all input voltages and operational modes. A PD should present one and only one classification signature during classification. By default, a PD is Class 0; however, to improve power management for the PSE, a PD may provide a signature for Class 1 to 3.

Table 33-10 - PD Power classification

Class	Usage	Range of maximum power used by the PD
0	Default	0.44 to 12.95 Watts
1	Optional	0.44 to 3.84 Watts
2	Optional	3.84 to 6.49 Watts
3	Optional	6.49 to 12.95 Watts
4	Not Allowed	Reserved for Future Use

Table 33-11 - Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5 V to 20.5 V	0	4	mA
Current for Class 1	14.5 V to 20.5 V	9	12	mA
Current for Class 2	14.5 V to 20.5 V	17	20	mA
Current for Class 3	14.5 V to 20.5 V	26	30	mA
Current for Class 4	14.5 V to 20.5 V	36	44	mA

Test Setup: Connect the receive pins of the DUT to the power supply.

Procedure:

1. Vary the power supply voltage from 12.5V to 22.5V.

2. Measure the corresponding current drawn by the DUT.
3. Insert 20 Ω in series between the DUT and the link partner
4. Apply a port voltage of 44 V.
5. Measure the current drawn by the DUT and calculate the input power averaged over a 1 second period.
6. Repeat steps 4 and 5, however, increment the port voltage by 1 V until the port voltage is equal to 57 V.

Observable Results:

a. In step 2 the current drawn by the DUT for each class should be within the range (inclusive) specified in Table 33-11.
b. In Step 6 the power drawn by the DUT for each class should be within the range (inclusive) specified in Table 33-10.

Possible Problems: None

Test #33.1.6: PD Power Supply Turn On / Off

Purpose: To verify that the DUT will turn on once power has been applied to the PI, will remain on over the entire port voltage range, and turn off once power is removed.

Reference:
[1] IEEE Std 802.3af, 2003 Edition: subclause 33.5.1, 33.5.7, Table 33-12.

Resource Requirements:
- PSE Simulator
- Current meter

Last Modification: August 4, 2003

Discussion: To be completed.

Test Setup: Connect the PSE to the PD Simulator through a 20Ω series resistance.
Procedure:
1. Apply 30V across the PI
2. Observe the operational status of the DUT
3. Repeat steps 1 and 2, however, increment the applied voltage by 1 V until the DUT has become fully operational.
4. Once operational, increase the port voltage to 44 V.
5. Vary the applied voltage over the range 44 V to 57 V in 1 V increments.
6. Observe the operational status of the DUT
7. Decrease the applied voltage by 1 V
8. Observe the status of the DUT
9. Repeat steps 7 and 8 until the DUT turns off

Observable Results:
a. The DUT should become fully operational at a port voltage less than 42 V.
b. Once the DUT has turned on, it should remain operational for port voltages between 44 V and 57 V.
c. The DUT should turn off at a port voltage greater than 30V and less than 36 V.