University of New Hampshire InterOperability Laboratory
Power Over Ethernet Consortium

Superseded

As of December 22, 2003 the Power Over Ethernet Consortium Clause 33 Powered Device Parametric Conformance Test Suite version 1.2 has been superseded by the release of the Clause 33 Powered Device Parametric Conformance Test Suite version 1.3. This document along with earlier versions, are available on the Power Over Ethernet Consortium test suite archive page.

Please refer to the following site for both current and superseded test suites:

http://www.iol.unh.edu/testsuites/ethernet/archive.html

Power Over Ethernet

Powered Device
Parametric Test Suite

Technical Document

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Power Over Ethernet Consortium
InterOperability Laboratory
Research Computing Center
University of New Hampshire

121 Technology Drive, Suite 2
Durham, NH 03824
Phone: (603) 862-0166
Fax: (603) 862-4181
http://www.iol.unh.edu/consortiums/poe/

MODIFICATION RECORD

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Gerard Nadeau	University of New Hampshire
Jeremy Kent	University of New Hampshire
Nathan Bourgoine	University of New Hampshire
Jeff Lapak	University of New Hampshire
Veena Venugopal	University of New Hampshire

INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers identify problems that IEEE p802.3af D4.1 devices may have in establishing link and exchanging packets with each other. The tests do not determine if a product conforms to the IEEE p802.3af D4.0 standard. Rather, they provide one method to verify that the two devices can exchange packets within the bit error ratio specifications established by the IEEE p802.3af D4.1 standard when operating over a worst-case compliant channel. The interoperability test suite focuses on two areas of functionality to simulate a real-world environment: the exchange of packets to produce a packet error ratio that is low enough to meet a desired bit error ratio while power is being supplied over the link channel, and the ability to detect and establish a link at the optimal speed between two devices that make up a link segment while power is being supplied over the link channel. A third area covers specific cable testing.

Note: Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other compliant devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in most environments.

Cable Plants

The intent of interoperability testing is to ensure that the DUT will perform as expected in a real world network. Testing in a real world network is often variable. Each technology has a standard, which defines the allowable cable characteristics for that technology. To account for all of the possible cable plant scenarios in the real world, a "worst case cable plant" which is very close to the limit of the TIA/EIA cable standards is used. The cable plants are tuned to be between 1-5% above the margins specified in ANSI-TIA-EIA-568-B-2001 or other applicable specifications. A shorter patch cable is also included in testing to insure that short links between devices are also viable.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose
The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References
The references section lists cross-references to the IEEE p802.3af D4.1 standard and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements
The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification
This specifies the date of the last modification to this test.

Discussion
The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup
The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure
The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results
The observable results section lists specific items that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable result, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable result.

Possible Problems
This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

TABLE OF CONTENTS

Test Suites Related to PD parametric testing

Scope: The following tests cover parametric tests specific to Powered Devices that support 10BASE-T, 100BASE-TX, and 1000BASE-T devices.

Overview: These tests are designed to identify problems that IEEE Draft P802.3af/ D4.1compliant devices may have in establishing link and exchanging packets with each other.

PD 1:PD source power

Purpose: To verify that PD does not source power

Reference:

[1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.3.1, Table 33-7, Figure 33-5.

Resource Requirements:

- Voltmeter

Last Modification: March 6, 2003

Discussion: The PD should not source power on its PI at any time.

Test Setup: Connect the DUT to a voltmeter.

Procedure:

1. Measure the V_{Port} at the PI of the DUT using a voltmeter.
2. Verify that there is no power at the PI

Observable Results:

a. In step 1 the DUT should not source any power on its PI.

Possible Problem: None

PD 2: PD Pinout

Purpose: Verify that the PD operates in PD Mode-B and per at least one of the PD Mode-As.

Reference:
[1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Sections 33.3.1, Figure 33-5, Table 33-7

Resource Requirements:
- Voltage Source
- PSE Simulator

Last Modification: March 6, 2003

Discussion: After detection and optional classification, a PSE could supply power on either set of the four wire pairs, hence the PD must be able to support both Mode A and Mode B. In addition, a PD should not accept power simultaneously on both wire pairs. The PD must be able to operate in at least one of the PD Mode A columns, and in the PD Mode B column in Table 33-7. A PD that implements Auto-MDI-X should be polarity insensitive.

Test Setup: The PD is connected to a voltage source.

Procedure:
1. Set the PSE simulator to supply power in accordance to Mode A MDI.
2. Check if the DUT is powered up.
3. Repeat steps 1 and 2 for Mode A MDI-X and Mode B.

Observable Results:
a. The DUT must accept power in Mode B and in at least one of the setups for Mode A.

Possible Problems: None

PD 3: Valid PD detection signature characteristics

Purpose: Verify valid PD detection signature characteristics measured at PD input connector.

References:

[1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Section 33.3.3, Annex 33C.4, Figure 33C.19, 33C.20, 33C.21, Table 33-8

Resource Requirements:

- PSE Simulator
- Oscilloscope
- Current meter
- Inductance meter

Last Modification: March 6, 2003

Discussion:

If a PD will accept power via the PI, but is not powered via the PI, then it shall present a valid detection signature at the PI between the positive and negative V_{Port} pins for both Mode A and Mode B as defined in 33.3.1.

Test Setup:

Connect the PSE to the PD Simulator with a 1m length of Category 5 cable. Confirm that the PD under test is currently not powered via the PI but will accept power via the PI.

Procedure:

For Setup # 1

1. Refer to the figure 33C.19. Close only switch S1 to measure the current for the V-I slope.
2. Limit the current of V_N between 4 to 5 mA.
3. Vary V_N from 2.7V to 10.1V in steps of 1V and measure I_N for each V_N.
4. Calculate $Rsig_N = (V_{N+1} - V_N)/(I_{N+1} - I_N)$.
5. Calculate the voltage offset by calculating the intersection of the line between the (V_N, I_N) and (V_{N+1}, I_{N+1}) data points and V/I axis. (Refer to Figure 33C.20)
6. Calculate the current offset by calculating the intersection of the line between the (V_N, I_N) and (V_{N+1}, I_{N+1}) data points and V/I axis. (Refer to Figure 33C.20)

For Setup #2

1. Refer to the figure 33C.19. Open S1 and close S2 to measure the Input capacitance of the PD. Connect the inductance meter in series with the current source.
2. Activate the constant current source of 100μA by closing S2.Calculate the capacitance by ramping up the capacitance voltage with a constant current source. Use I*t=V*C to calculate the capacitance. This method is useful when series diodes are present.
3. Calculate the port capacitance (Cpd) by measuring the port resistance (Rpd) and using it in a typical differential equation solution.
4. Measure the inductance using the inductance meter.

Observable Results:

For Setup #1

a. In step 3 verify that 23.5 KΩ<= $Rsig_N$<=26.25KΩ
b. In step 4 verify that voltage offset is less than 1.9V.
c. In step 5 verify that current offset is less than 10μA.

For Setup #2

a. In step 2 calculate Cpd and verify that 50nF<=Cpd<=130nF.
b. In step 3 the input inductance should be less than 100μA.

Possible Problems: None

PD 4: Non- valid PD detection signature characteristics

Purpose: Verify non-valid PD detection signature characteristics measured at PD input connector.

Reference:

[1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Subclause 33.3.3, Annex 33C.4, Figure 33C.19, 33C.20, 33C.21, Table 33-9

Resource Requirements:

- PSE Simulator
- Current meter

Last Modification: March 4, 2003

Discussion:

There are two cases when a PD should present a non-valid detection signature when attached to the PSE via the PI. The first case is while a PD is in a state where it will not accept power via the PI. The second case is when a PD becomes powered via the PI, and it must present a non-valid detection signature on the set of pairs from which is it not drawing power.

Test Setup:

Connect the PSE to the PD Simulator with a 1m length of Category 5 cable. Confirm that the PD under test is either powered via the PI or is in a state where it will not accept power via PI. Refer to the figure 33C.19.

Procedure:

V-I Slope

1. Close only switch S1 to measure the current for the V-I slope.
2. Limit the current of V_N between 4 to 5 mA.
3. Vary V_N from 2.70V to 10.1V in steps of 1V and measure I_N for each V_N.
4. Calculate $Rsig_N = (V_{N+1} - V_N)/(I_{N+1} - I_N)$.
5. Vary V_N from 0.00V to 2.7V in steps of 0.20V and measure I_N for each V_N.
6. Repeat step 3.

Input Capacitance

7. Open S1 and close S2 to measure the Input capacitance of the PD.
8. Activate the constant current source of 100μA by closing S2. Ignore any data points above 10.1V.
9. Calculate the capacitance by ramping up the capacitance voltage with a constant current source. Use I*t=V*C to calculate the capacitance. This method is useful when series diodes are present.
10. Calculate the port capacitance (Cpd) by measuring the port resistance (Rpd) and using it in a typical differential equation solution.

Observable Results:

a. In step 4 verify that 12 KΩ> $Rsig_N$ or $Rsig_N$>45KΩ.

b. In step 9 calculate Cpd and verify that 10μF<Cpd.

Possible Problems: None

PD 5: PD Classification signature characteristics

Purpose: Verify PD classification signature characteristics, measured at PD input connector.

Reference:
[1] IEEE *Draft* Std 802.3af/D4.1, 2003 Edition: Sections 33.3.4, Table 33-10, Table 33-11, and, Annex 33C.4, Figure 33C.19

Resource Requirements:
- PSE Simulator
- Current meter
- Oscilloscope

Last Modification: March 4, 2003

Discussion:
The purpose of PD classification is to provide the PSE information about the maximum power that the PD will draw across all input voltages and operational modes. A PD should present one and only classification signature during classification. A PD that does not support classification will be classified as Class 0 by default. The PD that provides a valid classification signature characteristic will be classified as Class 1-3.

Test Setup: Refer to the setup illustrated in Figure 33C.19.

Procedure:
1. Set switch S1 ON and S2 OFF.
2. Vary the Voltage V_N from 15V to 20V.
3. Measure the corresponding I_N.
4. Confirm that the PD provided the required classification signature within $T_{Class.}$
5. Apply voltage in the range V_{Port} higher than $V_{ON.}$
6. Measure the current drawn by the PD.

Observable Results:

a. If the PD does not support classification, then it must not draw more power than that specified in Table 33-10.
b. For step 3 the characteristics of the PD should abide by those specified in Table 33-11.
c. For Step 6 the power drawn by the PD should abide by those specified in Table 33-10.

Possible Problems: None