FAST ETHERNET CONSORTIUM

Clause 25 100BASE-TX PMD
Energy Efficient Ethernet
Test Suite

Version 1.1

Technical Document

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MODIFICATION RECORD

Revision	Release Date	Author	Comments
0.1		Harrison de Bree	• Initial Preliminary Draft
0.2		Jon Beckwith	• Added lots of tests
0.3		Jon Beckwith	• Made a PMD-specific version and incorporated first round of comments
0.4		Jon Beckwith Pete Scruton Jeff Lapak Mike DeGaetano	• Group Review
0.5		Jon Beckwith	• Fixed test procedure in 25.1.6 • Changed Clock tolerance test
1.0		Jon Beckwith	• Minor Editorial Changes • Initial Public Release
1.1		Mike DeGaetano	• Removed Wake Signal tests

The University of New Hampshire
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Jon Beckwith	UNH InterOperability Laboratory
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Peter Scruton	UNH InterOperability Laboratory
Jeff Lapak	UNH InterOperability Laboratory
Michael DeGaetano	UNH InterOperability Laboratory

INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the functionality of their Energy Efficient Ethernet capable 100BASE-TX Fast Ethernet products.

These tests are designed to determine if a product conforms to specifications defined in Clause 25 and Clause 78 of the IEEE P802.3AZ-D3.1 Standard. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many Fast Ethernet environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

Test Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

GROUP 1: EEE ELECTRICAL REQUIREMENTS

Overview:

This group of tests verifies several of the electrical specifications of the Energy Efficient portion of the 100BASE-TX Physical Medium Dependent sublayer outlined in clause 25 of the IEEE P802.3AZ-D3.1 standard.

Scope:

All of the tests described in this section are undergoing implementation and are currently not active at the University of New Hampshire InterOperability Lab.

Test 25.1.1 – Transmitter Timing Jitter

Purpose: To verify that the total transmit jitter of the device under test (DUT) is below the conformance limit.

References:

[1] IEEE Std P802.3AZ-D3.1, subclause 25.4.6 – Change to 9.1.9, "Jitter"
[2] UNH-IOL Clause 25 TP-PMD Test Suite, v3.4 - Test 25.1.4
[3] UNH-IOL Clause 25 TP-PMD Test Suite, v3.4 - Appendix 25.B

Resource Requirements: See Appendix A

Last Modification: November 12, 2009

Discussion:

Reference [1] specifies the jitter requirements for a 100BASE-TX EEE-capable DUT. References [2] and [3] outline the jitter procedure for non-EEE 100BASE-TX devices. This measurement employs the same technique that has been discussed in references [2] and [3] with three notable exceptions. Here, the measurement shall be done using 100ms to 1000ms of data, excludes the first 5μs worth of edge data during the TX_SLEEP state, and ignores jitter contributions from clock transitions occurring during the TX_QUIET state.

Test Setup: See Appendix A

Test Procedure:

1. Establish a 100BASE-TX EEE link between the DUT and the testing station and wait for the DUT to enter low power idle mode.
2. Use an EEE-capable 100BASE-TX transmitter to force the DUT to enter low power idle.
3. Ensure that the DUT is sending scrambled SLEEP code groups during its' Refresh states.
4. Capture 100ms to 1000ms worth of edge data, ignoring the first 5μs of edge data during the TX_SLEEP state and during TX_QUIET.
5. Measure the peak-to-peak transmit jitter at a BER of 10^{-8} using the method shown in reference [3].

Observable Results:

a. The peak-to-peak transmit jitter shall not exceed 1.4ns at a BER of 10^{-8}.

Possible Problems: None

Test 25.1.2 – Sleep time

Purpose: To verify the DUT transmits the SLEEP signal for the time specified.

References:

[1] IEEE Std P802.3AZ-D3.1, subclause 78.2 – LPI mode timing parameters description
[2] IEEE Std P802.3AZ-D3.1, Subclause 24.2.2.1.1 – Data code-groups
[3] IEEE Std P802.3AZ-D3.1, subclause 24.2.3.4 – Timers

Resource Requirements: See Appendix A

Last Modification: November 12, 2009

Discussion:

Reference [1] specifies the length of time, T_s, the PHY transmits the SLEEP signal before shutting down all transmitters and entering the QUIET state. Reference [2] defines the SLEEP signal, /P/, which is sent as 00000 and when observed after scrambling, matches the output of the scrambler. The value measured in this test is the value the DUT used for its' lpi_tx_ts_timer.

Test Setup: See Appendix A

Test Procedure:

1. Establish a 100BASE-TX EEE link between the DUT and the testing station and wait for the DUT to enter low power idle mode.
2. Use an EEE-capable 100BASE-TX transmitter to force the DUT to enter low power idle.
3. Capture waveform.
4. Decode the waveform prior to the quiet state.
5. Measure T_s.
6. Repeat for multiple captures

Observable Results:

a. T_s should be greater than 200μs and less than 220μs.

Possible Problems: None

Test 25.1.3 – Quiet time

Purpose: To verify that the amount of time the DUT is quiet is within the conformance limits.

References:

[1] IEEE Std P802.3AZ-D3.1, subclause 78.2 – LPI mode timing parameters description
[2] IEEE Std P802.3AZ-D3.1, subclause 24.2.3.4 – Timers

Resource Requirements: See Appendix A

Last Modification: November 12, 2009

Discussion:

Reference [1] specifies the length of time, T_q, the DUT is in the QUIET state. T_q is measured from when the SLEEP time crosses below the Signal_Detect de-assertion threshold to when the Refresh signal crosses above the Signal_Detect assertion threshold. The value measured in this test is the value the DUT uses for its' lpi_tx_tq_timer.

Test Setup: See Appendix A

Test Procedure:

1. Establish a 100BASE-TX EEE link between the DUT and the testing station and wait for the DUT to enter low power idle mode.
2. Capture waveform.
3. Measure T_q.
4. Repeat for multiple captures.

Observable Results:

a. T_q should be greater than 20ms and less than 22ms.
b. INFORMATIVE: Measure the peak transmit voltage during the quiet period. There should be no stray signaling or transitions observed.

Possible Problems: The DUT may prematurely exit the quiet state if there are frames being sent. In these circumstances, the measured quiet time may not reflect the value of T_q and should not be included as part of the measurement.

Test 25.1.4 – Refresh time

Purpose: To verify the DUT transmits the refresh signal for the time specified.

References:

[1] IEEE Std P802.3AZ-D3.1, subclause 78.2 – LPI mode timing parameters description
[2] IEEE Std P802.3AZ-D3.1, subclause 24.2.3.4 – Timers

Resource Requirements: See Appendix A

Last Modification: November 12, 2009

Discussion:

Reference [1] specifies the time, T_r, that the DUT transmits the REFRESH signal before entering the QUIET state. T_r is measured from when the Signal_Detect assertion threshold is detected after a quiet period to when the Signal_Detection de-assertion threshold is detected before a quiet period.

Test Setup: See Appendix A

Test Procedure:

1. Establish a 100BASE-TX EEE link between the DUT and the testing station and wait for the DUT to enter low power idle mode.
2. Capture refresh waveform.
3. Measure T_r using the Signal_Detect threshold as a beginning and ending point.
4. Repeat for multiple captures.

Observable Results:

a. T_r should be greater than 200μs and less than 220μs.

Possible Problems: The DUT may prematurely exit the sleep state if there are frames being sent. In these circumstances, the measured refresh time may not reflect the value of T_r and should not be included as part of the measurement.

Test 25.1.5 – Transmit wake time

Purpose: To verify that the amount of time the DUT transmits the wake signal is within the conformance limits.

References:

[1] IEEE Std P802.3AZ-D3.1, subclause 78.2 – LPI mode timing parameters description
[2] IEEE Std P802.3AZ-D3.1, table 78-4 – Summary of LPI timing parameters
[3] IEEE Std P802.3AZ-D3.1, figure 78-4 – LPI mode timing parameters and their relationship to minimum system wake time

Resource Requirements: See Appendix A

Last Modification: December 16, 2009

Discussion:

Reference [1] specifies the time, T_{phy_wake} that the DUT transmits the WAKE signal before resuming normal data transmission. Here, WAKE is signified by 100BASE-TX IDLE, and can be measured explicitly as the duration of transmitted IDLE between the last QUIET period and the first data frame. Reference [2] defines a minimum transmit wake time, $T_{w\_sys\_tx}$, that the DUT should transmit. Reference [3] defines $T_{w\_sys\_tx}$ (repeated in eq. 25.1.6 below for convenience) from the MII, and incorporates a $T_{phy\_shrink\_tx}$ value. Since this test observes the signal at the MDI, $T_{phy\_shrink\_tx}$ is zero, and hence $T_{w\_sys\_tx}$ should be equal to $T_{w\_sys\_rx}(\min) + T_{phy\_shrink\_rx}(\max)$. For 100BASE-TX, the minimum allowable transmit wake time is 25μs.

$$T_{w\_sys\_tx}(\min) = T_{w\_sys\_rx}(\min) + T_{phy\_shrink\_tx}(\max) + T_{phy\_shrink\_rx}(\max) \quad \text{(eq. 25.1.6)}$$

Test Setup: See Appendix A

Test Procedure:

1. Establish a 100BASE-TX EEE link between the DUT and the testing station and wait for the DUT to enter low power idle mode.
2. Cause the DUT to send a frame
3. Measure the amount of time the DUT transmits IDLE signaling prior to the frame
4. Repeat multiple times, and record the results.

Observable Results:

a. T_{phy_wake}, the amount of time the DUT should transmit IDLE before a frame, should be greater than 25μs.

Possible Problems: None

GROUP 2: EEE RECEIVE TESTS

Overview:

This group of tests verifies the integrity of the Device Under Tests' Active Input Interface. This is done by using various frame reception and physical characterization tests while operating in Energy Efficient Mode.

Scope:

All of the tests described in this section are undergoing implementation and are currently not active at the University of New Hampshire InterOperability Lab.

Test 25.2.1 – Adaptive Equalization with Fast Wakeup

Purpose: To verify that, while operating in Energy Efficient Ethernet mode and under worst-case operating conditions, the device under test (DUT) correctly compensates for the wide range of attenuation and phase distortion introduced by cable and is able to wake up within the minimum required time.

References:

[1] IEEE Std P802.3AZ-D3.1, Clause 25
[2] ANSI X3.263-1995, section 9.2.1
[3] UNH-IOL Clause 25 TP-PMD Test Suite
[4] IEEE Std P802.3AZ-D3.1, subclause 78.2 – LPI mode timing parameters description
[5] IEEE Std P802.3AZ-D3.1, table 78-4 – Summary of the LPI timing parameters for supported PHYs

Resource Requirements: See Appendix A

Last Modification: December 15, 2009

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100BASE-TX devices. Reference [2] defines a set of input signals that must be accepted by the Active Input Interface (AII).

Test 25.2.2 in reference [3] defines an Adaptive Equalization test which performs a sweep from 5% to 100% of the maximum allowable attenuation levels in a 100BASE-TX environment. Based on the analysis in Appendix 25.D in reference [4], no more than 7 packets can be lost throughout the course of the test in order to maintain a BER of less than 10^{-8}.

Devices that are capable of operating in Energy Efficient Ethernet mode are expected to do so without any corruption or loss of data. References [4] and [5] specify parameters associated with Low Power Idle, including a wake time. This parameter is negotiated during Auto-Negotiation. $T_{w\_sys\_rx}$ defines the absolute minimum time required by the system between a request to wake and its' readiness to receive data. For 100BASE-TX, $T_{w\_sys\_rx}$ is 10μs. $T_{phy\_shrink\_tx}$ and $T_{phy\_shrink\_rx}$ are the PHY Tx and Rx shrinkage time, the difference in time from the MDI to the xMIII when a change from Assert LPI to Normal IDLE occurs.

Figure 78-4 in reference [5] summarizes the LPI timing parameters. Equation 25.2.1-1 below shows the minimum transmit system wake time that system designers are recommended to follow. The minimum system transmit wake time is as follows:

$$T_{w\_sys\_tx}(\min) = T_{w\_sys\_rx}(\min) + T_{phy\_shrink\_tx}(\max) + T_{phy\_shrink\_rx}(\max) \qquad \text{(eq. 25.2.1-1)}$$

While using the setup shown in figure 25.A-1, there is no need to add any compensation transmitter readiness, and we can hence set $T_{phy\_shrink\_tx}$ to 0. Table 25.1-1 shows the values used to calculate $T_{w\_sys\_tx}$(min) used in the test procedure.

Table 25.2.1-1: wakeup time constants for 100BASE-TX

PHY Type	$T_{phy\_shrink\_rx}$(max), in μs	$T_{w\_sys\_rx}$(min), in μs
100BASE-TX	15	10

Using eq. 25.2.1-1, and setting $T_{phy\_shrink\_tx}$(max) to zero, $T_{w\_sys\_tx}$ is 25μs. The DUT is expected to maintain normal packet error exchange rates when this minimum system wakeup time is used. This test has 2 cases: one which has 20,000 1518-byte packets, each of which is immediately preceded by a minimum wakeup time and followed by an interpacket gap large enough to allow the device to respond to the frame, and the second which has one minimum wakeup time, immediately followed by 500,000 64-byte packets.

Table 25.2.1-2 summarizes the model parameters used in this test in the context of the link model defined in appendix 25.C in reference [3].

Table 25.2.1-2: Summary of model parameters for test #25.2.1

Parameter	Description	Value	Units
J_{pp}	Peak-peak jitter	1.4	ns
t_r	Response time	3 (5)	ns
%OS	Waveform overshoot	5	%
R_S	Transmitter source impedance	100	Ω
R_L	Receiver load impedance	100	Ω
L_1	Transmitter open circuit inductance	350	μH
L_2	Receiver open circuit inductance	350	μH
R_{WG}	Waveform generator source impedance	100	Ω
R_{DUT}	DUT load impedance	100	Ω
L_{DUT}	DUT open circuit inductance	measured in test #25.1.7	μH
l	Cable length	5 to 100 in increments of 5	m
T	Temperature	60	°C
V_{out}	Differential output voltage	950	mV
C	Number of connectors in the channel	4	—
M	Flat loss margin	0.3	dB
N_B	Reference NEXT loss (at 16MHz)	40.5	dB
N_M	NEXT loss scale	16.6	$^{dB}/_{decade}$

Test Setup: See Appendix A

Test Procedure:

1. Use a 100BASE-TX EEE source to negotiate a 100BASE-TX EEE link.
2. Configure the link simulator to use the model parameters in table 25.2.1-2 with a response time of 3ns and cable length of 5m. Monitor any errors with a link monitor attached to the DUT's Tx pair.
3. The link simulator will repeat the following pattern 20,000 times:
   a. IDLE for a minimum allowable duration
   b. One cycle of quiet/refresh/quiet
   c. IDLE for 25μs to trigger a wakeup from LPI
   d. 1 1518-byte ICMP request packet.
4. Repeat steps 1-3, incrementing the cable length by 20m with each iteration, until the cable length reaches 100m.
5. Repeat steps 1-4 with a low-power idle state prior to 1 group of 500,000 64-byte frames.
6. Repeats steps 1-5 for a response time of 5ns.

Observable Results:

a. There shall be no more than 7 errors for any iteration.

Possible Problems:

The rate at which the device under test can process incoming packets may make the test duration prohibitive. In such cases, fewer packets may be sent resulting in a lower confidence that a bit error rate of 10^{-8} is being met.

Test 25.2.2 – Clock Tolerance

Purpose: To verify that 100BASE-TX EEE-capable devices correctly track a varying source clock.

References:
[1] IEEE Std P802.3AZ-D3.1, subclause 24
[2] UNH-IOL Clause 25 TP-PMD Test Suite, Appendix 25.D

Resource Requirements: See Appendix A

Last Modification: September 1, 2009

Discussion:
While the DUT is operating in low-power idle mode, there are long (20-22ms) periods of "quiet" in which no signaling is being transmitted, immediately followed by short bursts of MLT-3, which allow for clock synchronization to be maintained. During these quiet periods, the receiver will likely choose to leave its' PLL running with the last-known configuration, and use these values when it attempts to lock onto the signal during the refresh periods.

Reference [1] states that a complaint 100BASE-TX transmitter shall have a source clock of 125 MHz +/- 0.01% (+/- 6.25kHz). This test varies the clock frequency of the transmitted signal, stressing the ability of the receiver to maintain clock synchronization. .

Test Setup: See Appendix A

Test Procedure:
1. Use a 100BASE-TX EEE source to negotiate a 100BASE-TX EEE link
2. Configure the link simulator to use a source clock frequency of 125MHz – 6.25kHz.
3. Configure the link simulator for a simulated cable length of 0m. Monitor any errors with a link monitor attached to the DUT's Tx pair.
4. The link simulator will repeat the following pattern 20,000 times:
   a. IDLE for a minimum allowable duration
   b. Ten cycles of quiet/refresh
   c. IDLE for 25μs to trigger a wakeup from LPI
   d. 1 1518-byte ICMP request packet.
5. Repeat steps 1-4 for simulated cable lengths of 75, 100m
6. Repeat steps 1-5 using a source clock frequency of 125MHz + 6.25kHz

Observable Results:
a. There shall be no more than 7 errors for any iteration.

Possible Problems: None

Test 25.2.3 – Long Term Frequency Stability

Purpose: To verify that 100BASE-TX EEE-capable devices are able to maintain a link and appropriate BER after operating in Low Power Idle mode for extended periods of time.

References:

[1] IEEE Std P802.3AZ-D3.1, Clause 78

[2] UNH-IOL Clause 25 TP-PMD Test Suite, Appendix 25.D

Resource Requirements: See Appendix A

Last Modification: September 1, 2009

Discussion:

Over long periods of time, oscillators and other components inside networking equipment have a tendency to have varying characteristics. Oscillators drift in frequency, temperature and humidity of environments changes, all of which affect two devices to maintain synchronization.

While investigations into temperature and humidity are out of scope for this test, observing a DUT's ability to maintain clock synchronization over long periods of time relates directly to the BER. This test is informative in nature and is performed in order to ensure that no obvious buffer management, clock stability, or higher-layer processes interfere with the low power idle state.

Test Setup: See Appendix A

Test Procedure:

1. Use a 100BASE-TX EEE source to negotiate a 100BASE-TX EEE link
2. Configure the link simulator for a simulated cable length of 0m. The link simulator will send IDLE for an arbitrary amount of time, low-power idle signaling (with minimum refresh durations and maximum quiet durations) for 1 hour, IDLE for 25μs to trigger a wakeup from LPI, immediately followed by 500,000 64-byte packets. Monitor any errors with a link monitor attached to the DUT's Tx pair.
3. Repeat steps 1-3 for simulated cable lengths of 75, 100m.

Observable Results:

a. Informative: At least 1 frame after the long LPI state must be responded to.

Possible Problems: None

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Appendix A – Test Setups

Purpose: To outline the test setups, hardware, and software used to perform the tests contained in this test suite.

References:

[1] IEEE Std 802.3az–2010, Clause 78 – Energy Efficient Ethernet

Last Modification: September 11, 2009

Discussion:

The following hardware is necessary to perform the testing outlined in this test suite:

- 100BASE-TX Energy Efficient Ethernet Transmitter, capable of negotiating a 100BASE-TX EEE link. Here, a dual Tektronix AWG2041 setup is used with a BNC-T.
- Oscilloscope
- Line Monitor
- Interconnecting Hardware
- Post-processing software (ex: UNH-IOL custom Matlab-based test tool)

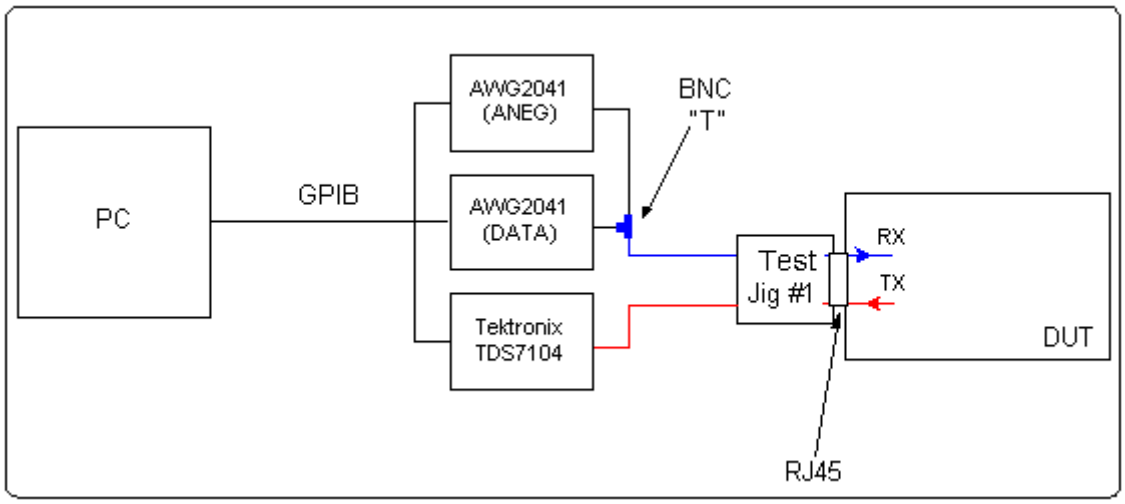

Figure A.1 – Test setup for Transmitter tests

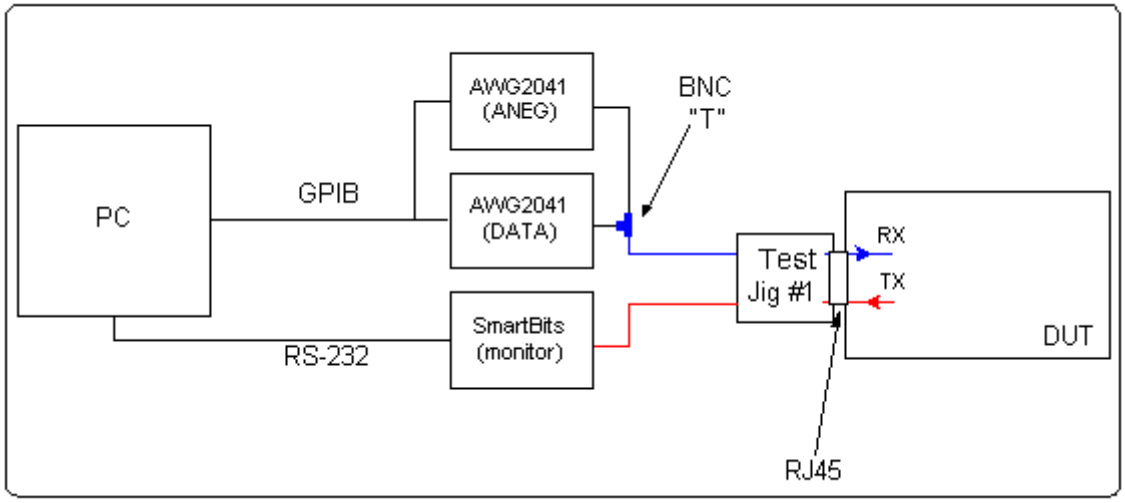

Figure A.2 – Test setup for receiver tests (single-port device)

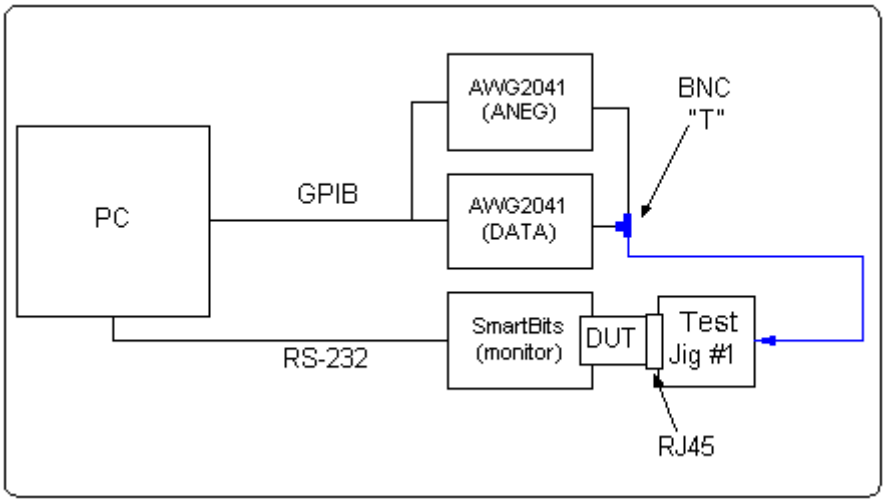

Figure A.3 – Test Setup for receiver tests (MII)

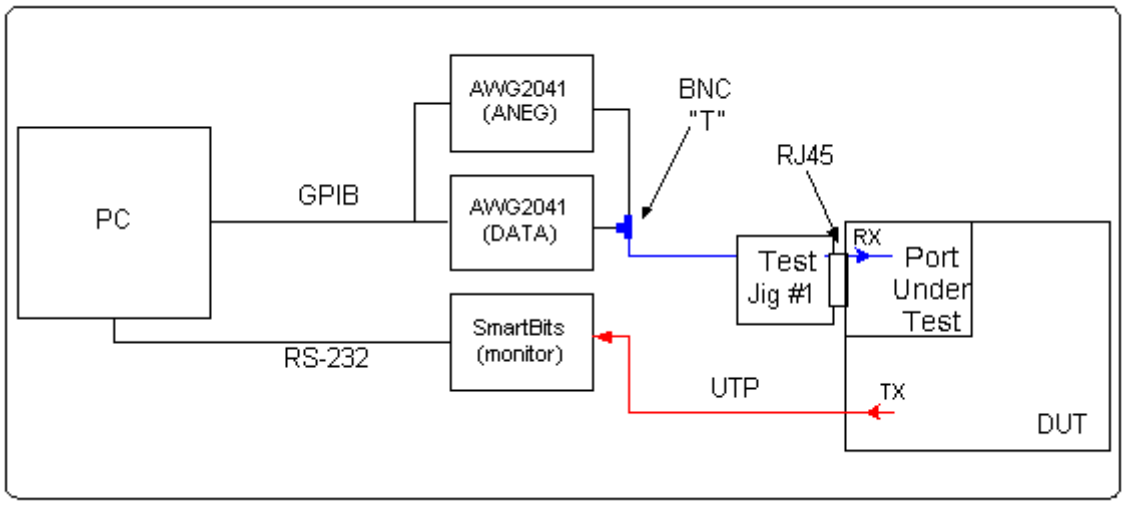

Figure A.4 – Test Setup for receiver tests (multi-port device)