

**2.5, 5, 10G ETHERNET  
TESTING SERVICE**  
**Clause 128A**  
**2.5G Storage Enclosure Interface Test Plan**  
***Version 1.0***

*Technical Document*



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*2.5, 5, 10G Ethernet Testing Service*

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**TABLE OF CONTENTS**

<b>TABLE OF CONTENTS .....</b>	<b>2</b>
<b>MODIFICATION RECORD.....</b>	<b>3</b>
<b>ACKNOWLEDGMENTS .....</b>	<b>4</b>
<b>INTRODUCTION.....</b>	<b>5</b>
<b>GROUP 1: ELECTRICAL SIGNALING REQUIREMENTS .....</b>	<b>7</b>
TEST 128A.1.1 – SIGNALING SPEED.....	8
TEST 128A.1.2 – COMMON MODE OUTPUT VOLTAGE.....	9
TEST 128A.1.3 – DIFFERENTIAL OUTPUT AMPLITUDE.....	10
TEST 128A.1.4 – TRANSITION TIME.....	11
TEST 128A.1.5 – TRANSMIT JITTER .....	12
TEST 128A.1.6 – TRANSMIT OUTPUT NOISE AND DISTORTION .....	13
<b>GROUP 2: IMPEDANCE REQUIREMENTS .....</b>	<b>14</b>
TEST 128A.2.1 – DIFFERENTIAL OUTPUT RETURN LOSS .....	15
TEST 128A.2.2 – DIFFERENTIAL INPUT RETURN LOSS.....	16
<b>GROUP 3: ELECTRICAL RECEIVER REQUIREMENTS .....</b>	<b>17</b>
TEST 128A.3.1 – HOST RECEIVER INTERFERENCE TOLERANCE.....	18
TEST 128A.3.2 – HOST RECEIVER JITTER TOLERANCE .....	19
TEST 128A.3.3 – DRIVE RECEIVER INTERFERENCE TOLERANCE .....	20
TEST 128A.3.4 – DRIVE RECEIVER JITTER TOLERANCE.....	21
<b>APPENDICES.....</b>	<b>22</b>
APPENDIX 128A.A - TEST FIXTURES AND SETUPS .....	23

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**MODIFICATION RECORD**

March 28, 2018 Version 0.9

Hayden Haynes: Initial draft of test plan.

January 8, 2019 Version 1.0

Hayden Haynes: Initial draft of test suite.

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*InterOperability Laboratory*  
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Hayden Haynes  
Mike Klempa

UNH InterOperability Laboratory  
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## **INTRODUCTION**

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This test plan has been developed to help implementers evaluate the functionality of the Storage Enclosure Interface (SEI) sublayer of their 2.5GSEI products.

These tests are designed to determine if a product conforms to specifications defined in Annex 128A of the IEEE 802.3cb Standard. Successful completion of all tests contained in this plan does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 2.5GSEI environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test plan is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

### **Purpose**

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

### **References**

This section specifies source material *external* to the test plan, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test plan document itself.

### **Resource Requirements**

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

### **Last Modification**

This specifies the date of the last modification to this test.

### **Discussion**

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

### **Test Setup**

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

### **Test Procedure**

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

### **Observable Results**

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

### **Possible Problems**

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test plan appendices and/or whitepapers that may provide more detail regarding these issues.

## **GROUP 1: ELECTRICAL SIGNALING REQUIREMENTS**

**Overview:**

The tests defined in this section verify the electrical signaling characteristics of the Storage Enclosure Interface (SEI) layer defined in Annex 128A of IEEE 802.3cb.

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**Test 128A.1.1 – Signaling Speed**

**Purpose:** To verify that the baud rate of the DUT is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.1 – 2.5GSEI host output characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.3 – 2.5GSEI drive output characteristics
- [3] IEEE Std. 802.3cb, subclause 128A.3.1.1 – Signaling rate and range
- [4] IEEE Std. 802.3cb, Figure 128B-1 – Test configuration

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

References [1] and [2] specify the transmitter characteristics for 2.5GSEI devices. These specifications include conformance requirements for the signaling speed, which is specified in [3].

Reference [3] states that the 2.5GSEI signaling speed shall be 3.125 Gbaud +/- 100 ppm. This translates to 3.125 Gbaud +/- 0.3125 Mbaud, with a nominal Unit Interval (UI) of 320 ps.

In this test, the signaling speed is measured while the DUT is setup in the test configuration defined in [4], or its functional equivalent. The signal being transmitted by the DUT may be any valid 2.5GSEI signal.

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Configure the DUT to send a valid test pattern.
2. Connect the DUT's transmitter to the test fixture.
3. Measure the average transmitter signaling speed at TP4<sub>H-D</sub> for host.
4. Measure the average transmitter signaling speed at TP2<sub>D-H</sub> for drive.

**Observable Results:**

- a. The host and drive signaling speeds shall be within 3.125 Gbaud +/- 0.3125 Mbaud.
- b. The host and drive nominal unit interval value shall be 320ps.

**Possible Problems:** None.

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**Test 128A.1.2 – Common Mode Output Voltage**

**Purpose:** To verify that the DC common mode output voltage of the DUT is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.1 – 2.5GSEI host output characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.3 – 2.5GSEI drive output characteristics
- [3] IEEE Std. 802.3cb, subclause 128A.3.1.2 – Signaling levels
- [4] IEEE Std. 802.3cb, Figure 128B-1 – Test configuration
- [5] IEEE Std. 802.3-2018, Annex 48A.1 – High frequency test pattern

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

References [1] and [2] specify the transmitter characteristics for 2.5GSEI devices. These specifications include conformance requirements for the common mode output voltage defined in [3].

In this test, the DC and AC common mode output voltage is measured at the  $V_{com}$  test point while the DUT is connected to the test fixture defined in [4], or its functional equivalent. The signal being transmitted by the DUT shall be the high frequency test pattern defined in [5].

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Configure the DUT to transmit a high frequency test pattern.
2. Connect the DUT's transmitter to the test fixture.
3. Measure the common mode output voltage of SL<p> and SL<n> at the  $V_{com}$  test point.

**Observable Results:**

- a. The host and drive DC common mode output voltage shall not exceed 1.9 V with respect to the signal shield.
- b. The host and drive AC RMS common mode voltage shall not exceed 30 mV with respect to the signal shield.

**Possible Problems:** None.

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**Test 128A.1.3 – Differential Output Amplitude**

**Purpose:** To verify that the differential output amplitude of the DUT transmitter is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.1 – 2.5GSEI host output characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.3 – 2.5GSEI drive output characteristics
- [3] IEEE Std. 802.3cb, subclause 128.7.1.4 – Output amplitude
- [4] IEEE Std. 802.3cb, Figure 128B-1 – Test configuration
- [5] IEEE Std. 802.3-2018, Annex 48A.2 – Low frequency test pattern

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

References [1] and [2] specify the transmitter characteristics for 2.5GSEI devices. These specifications include conformance requirements for the differential output amplitude defined in [3].

In this test, the maximum and minimum differential peak-to-peak output voltage are measured while the DUT is connected to the test fixture defined in [4], or its functional equivalent. The signal being transmitted by the DUT shall be the square wave test pattern defined in [5] consisting of a run of at least eight consecutive ones and eight consecutive zeros.

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Connect the DUT's transmitter to the test fixture.
2. Configure the DUT to send the low frequency test pattern defined in [5].
3. Measure the maximum peak-to-peak differential output voltage.
4. Measure the minimum peak-to-peak differential output voltage.
5. Disable the transmitter and measure the peak-to-peak output voltage.

**Observable Results:**

- a. The host minimum and maximum differential peak-to-peak output voltages shall be no less than 580 mV and no greater than 1,200 mV respectively.
- b. The drive minimum and maximum differential peak-to-peak output voltages shall be no less than 800 mV and no greater than 1,200 mV respectively.
- c. The host and drive transmitter output voltage shall not exceed 35 mV peak-to-peak when disabled.

**Possible Problems:** None.

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**Test 128A.1.4 – Transition Time**

**Purpose:** To verify that the rising and falling edge transition times are within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.1 – 2.5GSEI host output characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.3 – 2.5GSEI drive output characteristics
- [3] IEEE Std. 802.3cb, subclause 128.7.1.7 – Transition time
- [4] IEEE Std. 802.3cb, Figure 128B-1 – Test configuration
- [5] IEEE Std. 802.3-2018, Annex 48A.1 – High frequency test pattern

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

References [1] and [2] specify the transmitter characteristics for 2.5GSEI devices. This specification includes conformance requirements for the rising and falling edge transition times defined in [3].

In this test, the transition time is measured while the DUT is connected to the test fixture defined in [4] or its functional equivalent. The transition times are to be measured at the 20% and 80% levels as defined in [1] and [2] using the high frequency test pattern defined in [5].

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Configure the DUT to send the high frequency test pattern defined in [5].
2. Connect the DUT's transmitter to the test fixture.
3. Measure the rising and falling edge transition times at the 20% and 80% levels.

**Observable Results:**

- a. The host maximum transition time shall be no greater than 460 ps.
- b. The drive maximum transition time shall be no greater than 229 ps.

**Possible Problems:** None.

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**Test 128A.1.5 – Transmit Jitter**

**Purpose:** To verify that the peak-to-peak transmit jitter of the DUT is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.1 – 2.5GSEI host output characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.3 – 2.5GSEI drive output characteristics
- [3] IEEE Std. 802.3cb, subclause 128A.3.1.4 – Transmit jitter test requirements
- [4] IEEE Std. 802.3cb, subclause 128A.3.1.5 – Transmit jitter
- [5] IEEE Std. 802.3cb, Figure 128B-1 – Test configuration
- [6] IEEE Std. 802.3-2018, Annex 48A.2 – Low frequency test pattern

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

References [1] and [2] specify the transmitter characteristics for 2.5GSEI devices. These specifications include conformance requirements for the peak-to-peak transmit jitter defined in [3] and [4].

In this test, the peak-to-peak transmit jitter is measured while the DUT is connected to the test fixture defined in [5] or its functional equivalent. Reference [6] specifies that the DUT must transmit the low frequency test pattern defined in reference [6]. For this test, Duty Cycle Distortion is considered part of Deterministic Jitter.

Jitter is defined at a BER of  $10^{-12}$ .

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Configure the DUT to send the low frequency test pattern defined in [6].
2. Connect the DUT's transmitter to the test fixture.
3. Measure the Random Jitter, Deterministic Jitter, Duty Cycle Distortion and Total Jitter.

**Observable Results:**

- a. The Random Jitter value shall not exceed 0.2 UI.
- b. The Deterministic Jitter value shall not exceed 0.12 UI.
- c. The Duty Cycle Distortion value shall not exceed 0.035 UI.
- d. The Total Jitter value shall not exceed 0.32 UI.

**Possible Problems:** None.

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**Test 128A.1.6 – Transmit Output Noise and Distortion**

**Purpose:** To verify that the SNDR of the DUT is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.1 – 2.5GSEI host output characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.3 – 2.5GSEI drive output characteristics
- [3] IEEE Std. 802.3cb, subclause 128A.3.1.6 – Transmitter output noise and distortion
- [4] IEEE Std. 802.3cb, Figure 128B-1 – Test configuration
- [5] IEEE Std. 802.3-2015, subclause 93A.1.4.3 – Receiver equalizer
- [6] IEEE Std. 802.3cb, Table 128A-2 – 2.5G host receiver equalizer parameters
- [7] IEEE Std. 802.3-2015, subclause 85.8.3.3.5 – Linear fit to the waveform measurement at TP2

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** March 23, 2018

**Discussion:**

References [1] and [2] specify the transmitter characteristics for 2.5GSEI devices. These specifications include conformance requirements for the signal to noise and distortion ratio (SNDR) limit defined in [3].

In this test, a complete cycle of PRBS9 is captured while the device is connected to the test fixture defined in [4] or its functional equivalent. The reference equalizer defined in [5] is applied to the captured waveform. Linear fit pulse response  $p(k)$  and linear fit error waveform  $e(k)$  are calculated from the resulting waveform. RMS deviation of the mean voltage is measured from the flattest portion of the waveform. These results are used to calculate the SNDR from Equation 128A-3 in reference [3].

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Capture a complete cycle of PRBS9.
2. Apply the reference equalizer in [5] using the values in [6].
3. Compute the linear fit pulse response  $p(k)$  and error  $e(k)$  as described in [7].
4. Measure the RMS deviation from the mean voltage at the flattest portion of the waveform.
5. Calculate the SNDR by using the results from steps 3 and 4 into Equation 128A-3 defined in [3].

**Observable Results:**

- a. The host and drive SNDR value shall be no less than 25 dB.

**Possible Problems:** None.

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**GROUP 2: IMPEDANCE REQUIREMENTS**

**Overview:**

The tests defined in this section verify the impedance characteristics of the Storage Enclosure Interface (SEI) layer defined in Annex 128A of IEEE 802.3cb.

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**Test 128A.2.1 – Differential Output Return Loss**

**Purpose:** To verify that the differential output return loss of the DUT is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.1 – 2.5GSEI host output characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.3 – 2.5GSEI drive output characteristics
- [3] IEEE Std. 802.3cb, subclause 128A.3.1.3 – Output return loss

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** March 23, 2018

**Discussion:**

References [1] and [2] specify the transmitter characteristics for 2.5GSEI devices. This specification includes conformance requirements for the differential output return loss, which is specified in [3].

For the purpose of this test, the differential output return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 50 MHz to 2343.75 MHz, the differential return loss of the driver shall abide by Equation 128A-2. The reference impedance for differential return loss measurements is 100  $\Omega$ .

$$Returnloss \geq \left\{ \begin{array}{ll} 12 & 50 \leq f < 275 \\ 12 - 6.75 \log_{10} \left( \frac{f}{275} \right) & 275 \leq f < 2343.75 \end{array} \right\} (dB) \quad (EQ. 128A - 2)$$

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing normal IDLE signaling.
3. Connect the DUT's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 50 MHz to 2343.75 MHz.
5. Compute the return loss from the reflection coefficient values.

**Observable Results:**

- a. The differential output return loss shall abide by the limits described in Equation 128A-2.

**Possible Problems:** None.

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**Test 128A.2.2 – Differential Input Return Loss**

**Purpose:** To verify that the differential input return loss of the DUT is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.2 – 2.5GSEI host input characteristics
- [2] IEEE Std. 802.3cb, subclause 128A.3.4 – 2.5GSEI drive input characteristics
- [3] IEEE Std. 802.3cb, subclause 128A.3.2.1 – Input differential return loss
- [4] IEEE Std. 802.3cb, subclause 128A.3.4.1 – Input differential return loss

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** March 23, 2018

**Discussion:**

References [1] and [2] specify the receiver characteristics for 2.5GSEI devices. These specifications include conformance requirements for the differential input return loss defined in [3] and [4].

For the purpose of this test, the differential input return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 50 MHz to 2343.75 MHz, the differential input return loss of the driver shall abide by the margins defined in Equation 128A-2. For input return loss measurements, hosts are measured at TP1<sub>D-H</sub>, drives are measured at TP3<sub>H-D</sub>. The reference impedance for differential input return loss measurements is 100 Ω.

$$Returnloss \geq \left\{ \begin{array}{ll} 12 & 50 \leq f < 275 \\ 12 - 6.75 \log_{10} \left( \frac{f}{275} \right) & 275 \leq f < 2343.75 \end{array} \right\} (dB) \quad (EQ. 128A - 2)$$

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing normal IDLE signaling.
3. Connect the DUT's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 50 MHz to 2343.75 MHz.
5. Compute the return loss from the reflection coefficient values.

**Observable Results:**

- a. The differential input return loss shall abide by the limits described in Equation 128A-2.

**Possible Problems:** None.

## **GROUP 3: ELECTRICAL RECEIVER REQUIREMENTS**

**Overview:**

The tests defined in this section verify the electrical signaling receiver characteristics of the Storage Enclosure Interface (SEI) layer defined in Annex 128A of IEEE 802.3cb.

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**Test 128A.3.1 – Host Receiver Interference Tolerance**

**Purpose:** To verify that the bit error ratio (BER) of the DUT receiver is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.2 – 2.5GSEI host input characteristics
- [2] IEEE Std. 802.3cb, subclause 128A3.2.2 – Receiver interference tolerance
- [3] IEEE Std. 802.3cb, Figure 128A-8 – Host interference calibration and test setup
- [4] UNH-IOL 100Base-Tx TP-PMD Test Suite, Appendix 25.D

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

In this test, the host receiver is tested to ensure it can extract data from a lossy channel while simultaneously being affected by interference. Reference [1] specifies the receiver characteristics for 2.5GSEI devices. This specification includes conformance requirements for the interference tolerance defined in reference [2].

Reference [2] outlines a procedure to inject interference into the test setup. An informative description of the test channel is provided in [3]. Reference [2] states that the target BER of a 2.5GSEI device is  $10^{-12}$ . Based on the analysis in reference [4], if more than 7 errors are observed out of  $3 \times 10^{12}$  bits, it can be concluded that the bit error rate of the device is greater than  $10^{-12}$  with less than a 5% chance of error.

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Create a lossy channel from ISI board, HCB and DCB with 5 dB of loss at 1.5625 GHz.
2. Measure signal through ISI channel at TP2<sub>D-H</sub> and adjust to meet max transition time of 460 ps.
3. Adjust amplitude to meet min and max output amplitude values of 580 mV and 1200 mV, respectively.
4. Adjust noise to meet SNDR value of 25 dB.
5. Adjust pattern generator RJ to meet value of 0.2 UI.
6. Send  $3 \times 10^{12}$  bits to the DUT receiver and calculate BER.

**Observable Results:**

- a. The measured target BER shall be no greater than  $10^{-12}$ .

**Possible Problems:** None.

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**Test 128A.3.2 – Host Receiver Jitter Tolerance**

**Purpose:** To verify that the bit error ratio (BER) of the DUT receiver is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.2 – 2.5GSEI host input characteristics
- [2] IEEE Std. 802.3cb, subclause 128A3.2.3 – Receiver jitter tolerance
- [3] IEEE Std. 802.3cb, Figure 128A-9 – Host jitter tolerance calibration and test setup
- [4] IEEE Std. 802.3cb, Table 128A-5 – Applied peak to peak sinusoidal jitter
- [5] UNH-IOL 100Base-Tx TP-PMD Test Suite, Appendix 25.D

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

In this test, the host receiver is tested to ensure it can extract data from a lossy channel while simultaneously being affected by interference. Reference [1] specifies the receiver characteristics for 2.5GSEI devices. This specification includes conformance requirements for the jitter tolerance defined in reference [2].

Reference [2] outlines a procedure to inject interference into the test setup. An informative description of the test channel is provided in [3]. Reference [2] states that the target BER of a 2.5GSEI device is  $10^{-12}$ . Based on the analysis in reference [4], if more than 7 errors are observed out of  $3 \times 10^{12}$  bits, it can be concluded that the bit error rate of the device is greater than  $10^{-12}$  with less than a 5% chance of error.

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Create a lossy channel from ISI board, HCB and DCB with 5 dB of loss at 1.5625 GHz.
2. Measure signal through ISI channel at TP2<sub>D-H</sub> and adjust to meet max transition time of 460 ps.
3. Adjust amplitude to meet min and max output amplitude values of 580 mV and 1200 mV, respectively.
4. Adjust pattern generator RJ to meet value of 0.2 UI.
5. Adjust sinusoidal jitter to meet value specified in [4].
6. Send  $3 \times 10^{12}$  bits to the receiver under test.
7. Repeat steps 5 and 6 with the remaining SJ test cases.

**Observable Results:**

- a. There shall be no more than 7 errors observed for any iteration.

**Possible Problems:** None.

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**Test 128A.3.3 – Drive Receiver Interference Tolerance**

**Purpose:** To verify that the bit error ratio (BER) of the DUT receiver is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.4 – 2.5GSEI drive input characteristics
- [2] IEEE Std. 802.3cb, subclause 128A3.4.2 – Receiver interference tolerance
- [3] IEEE Std. 802.3cb, Figure 128A-10 – Drive interference calibration and test setup
- [4] UNH-IOL 100Base-Tx TP-PMD Test Suite, Appendix 25.D

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

In this test, the drive receiver is tested to ensure it can extract data from a lossy channel while simultaneously being affected by interference. Reference [1] specifies the receiver characteristics for 2.5GSEI devices. This specification includes conformance requirements for the interference tolerance defined in reference [2].

Reference [2] outlines a procedure to inject interference into the test setup. An informative description of the test channel is provided in [3]. Reference [2] states that the target BER of a 2.5GSEI device is  $10^{-12}$ . Based on the analysis in reference [4], if more than 7 errors are observed out of  $3 \times 10^{12}$  bits, it can be concluded that the bit error rate of the device is greater than  $10^{-12}$  with less than a 5% chance of error.

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Create a lossy channel from ISI board, HCB and DCB with 13.5 dB of loss at 1.5625 GHz.
2. Measure signal through ISI channel at TP<sub>2H-D</sub> and adjust to meet max transition time of 229 ps.
3. Adjust amplitude to meet min and max output amplitude values of 800 mV and 1200 mV, respectively.
4. Adjust noise to meet SNDR value of 25 dB.
5. Adjust pattern generator RJ to meet value of 0.2 UI.
6. Send  $3 \times 10^{12}$  bits to the receiver under test.

**Observable Results:**

- a. There shall be no more than 7 errors observed.

**Possible Problems:** None.

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**Test 128A.3.4 – Drive Receiver Jitter Tolerance**

**Purpose:** To verify that the bit error ratio (BER) of the DUT receiver is within the conformance limits.

**References:**

- [1] IEEE Std. 802.3cb, subclause 128A.3.4 – 2.5GSEI drive input characteristics
- [2] IEEE Std. 802.3cb, subclause 128A3.4.3 – Receiver jitter tolerance
- [3] IEEE Std. 802.3cb, Figure 128A-11 – Drive receiver jitter tolerance test setup
- [4] IEEE Std. 802.3cb, Table 128A-9 – Applied peak to peak sinusoidal jitter
- [5] UNH-IOL 100Base-Tx TP-PMD Test Suite, Appendix 25.D

**Resource Requirements:** See Appendix 128A.A.

**Last Modification:** January 8, 2019

**Discussion:**

In this test, the drive receiver is tested to ensure it can extract data from a lossy channel while simultaneously being affected by interference. Reference [1] specifies the receiver characteristics for 2.5GSEI devices. This specification includes conformance requirements for the jitter tolerance defined in reference [2].

Reference [2] outlines a procedure to inject interference into the test setup. An informative description of the test channel is provided in [3]. Reference [2] states that the target BER of a 2.5GSEI device is  $10^{-12}$ . Based on the analysis in reference [4], if more than 7 errors are observed out of  $3 \times 10^{12}$  bits, it can be concluded that the bit error rate of the device is greater than  $10^{-12}$  with less than a 5% chance of error.

**Test Setup:** See Appendix 128A.A.

**Test Procedure:**

1. Create a lossy channel from ISI board, HCB and DCB with 13.5 dB of loss at 1.5625 GHz.
2. Measure signal through ISI channel at TP4<sub>H-D</sub> and adjust to meet max transition time of 229 ps.
3. Adjust amplitude to meet min and max output amplitude values of 800 mV and 1200 mV, respectively.
4. Adjust pattern generator RJ to meet value of 0.2 UI.
5. Adjust sinusoidal jitter to meet value specified in [4].
6. Send  $3 \times 10^{12}$  bits to the receiver under test.
7. Repeat steps 5 and 6 with the remaining SJ test cases.

**Observable Results:**

- a. There shall be no more than 7 errors observed for any iteration.

**Possible Problems:** None.

## **APPENDICES**

**Overview:**

Test plan appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test plan. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test plan. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test plan), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

**Scope:**

Test plan appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test plan.

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**Appendix 128A.A - Test Fixtures and Setups**

**Purpose:** To specify the measurement hardware, test fixtures, and setups used in this test plan.

**References:**

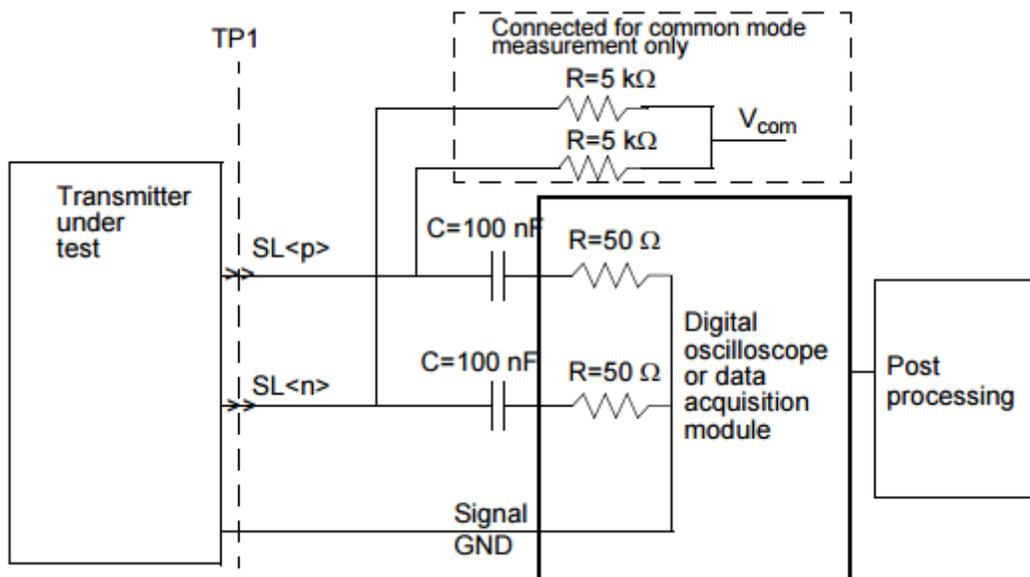
- [1] IEEE Std. 802.3cb, Annex 128B – Test Fixtures for 2.5G and 5G SEI

**Last Modification:** March 27, 2018

**Discussion:**

The tester will need the following in order to perform tests in Group 1.

1. Digital Storage Oscilloscope, 20 GHz bandwidth (minimum).
2. Transmitter Test Fixture.
3. Post Processing.
4. Digital Multi-meter.
5. SMA cables.



**128A.A-1: example test setup for tests 128A.1.1 through 128A.1.6**

**Explanation of 128A.A-1:**

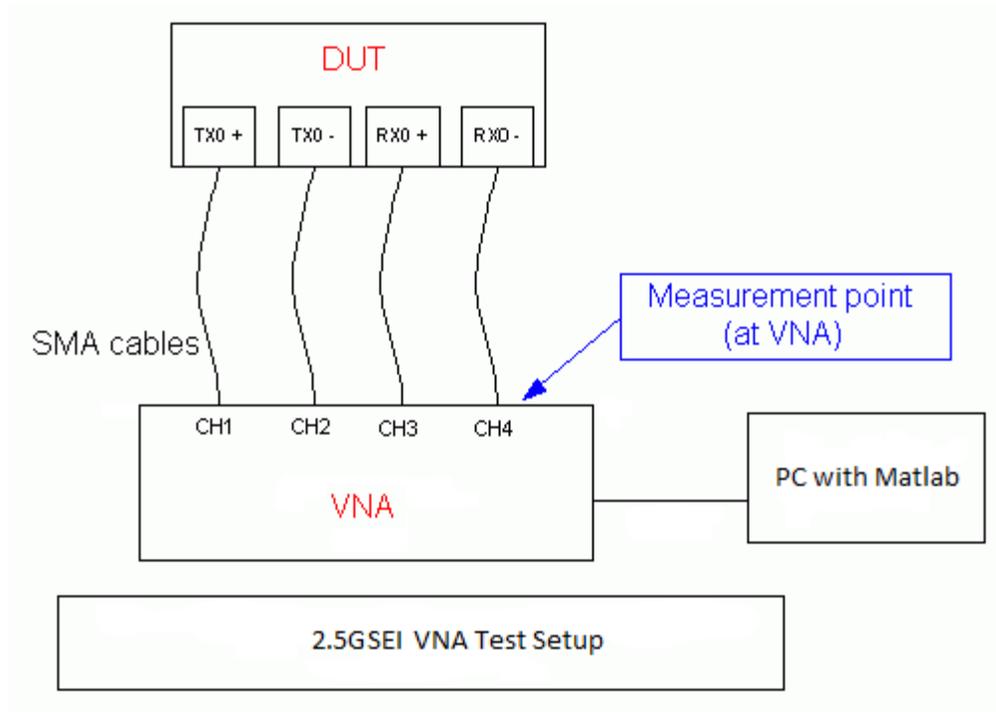
For test, 128A.1.2(Common Mode Output Voltage), the DSO is not used to perform the test. For 128A.1.2 the portion of the diagram above outlined with dotted lines will be used. Vcom in this diagram will be a DMM, set to measure voltage.

For the other six tests (128A.1.1-128A.1.6, excluding 128A.1.2), the DSO will be used. The DUT should be connected to the DSO as depicted in the above diagram through the channel slots on the DSO with SMA cables. The DSO is connected to a computer for post processing.

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The tester will need the following to perform tests in Group 2.

1. Vector Network Analyzer.
2. SMA cables.
3. Post Processing.



**128A.A-2: example test setup for tests 128A.2.1 and 128A.2.2**

**Explanation of 128A.A-2:**

For tests, 128A.2.1 and 128A.2.2, connect the DUT to the VNA with SMA cables according to the 128A.A-2 setup diagram. For post processing, connect the VNA to the PC.