Power over Data Line

IEEE Clause 104
Power Sourcing Equipment
Conformance Test Plan
Version 2.4

Last Updated: November, 2023

University of New Hampshire
InterOperability Laboratory
Power over Ethernet Consortium

21 Madbury Rd., Suite 100
Durham, NH 03824
Phone: (603) 862-0090
Fax: (603) 862-4181

http://www.iol.unh.edu/consortiums/poe

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MODIFICATION RECORD

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Wyman Smith: Preliminary release. First draft

June, 2022 Version 2.0
Marc Tausanovitch: Updated per IEEE 802.3cg and 802.3dd changes and latest UNH-IOL testing methodologies

March, 2023 Version 2.1
Marc Tausanovitch: Updated per internal review

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Marc Tausanovitch: Updated per external review and 802.3-2022 changes

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Marc Tausanovitch: Updated per hardware revision and internal review. Modifications to group 3 tests from 802.3dd changes.

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Craig Chabot	UNH InterOperability Laboratory
Wyman Smith	UNH InterOperability Laboratory
Marc Tausanovitch	UNH InterOperability Laboratory
Demetrios Galatis	UNH InterOperability Laboratory
Devin Eaton	UNH InterOperability Laboratory

INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functionality of the Power over Data Line (PoDL) or Single Pair Power over Ethernet (SPoE) Power Sourcing Equipments (PSE).

These tests are designed to determine if a product conforms to specifications defined in Clause 104 of the IEEE Std. 802.3bu. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many Power over Data Line/Single Pair Power over Ethernet environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

Test Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

TEST SETUP

Figure 1 is the general test setup used by the InterOperability Lab to perform the tests described in this test plan.

The DUT is connected to the UNH-IOL Powered Device Simulator which contains its own circuitry to perform detection, classification, and power on. A DC Load is supplemented in the setup to allow for static or dynamic current draws from the DUT. The UNH-IOL Powered Device Simulator provides the tester on-board breakouts for various measurement instruments. This allows data to be observed from the DUT during the tests included inside this test plan.

Each block is connected to the test station. This is either through an Ethernet Link via a Switch and Router or a USB connection. The DUT can also be connected to the test station if an interface is provided by the vendor. This connection is necessary if the vendor would like both SCCP and detection to be tested. The ability to enable or disable SCCP through this connection must also be available to the tester if both SCCP and detection is needed to be tested.

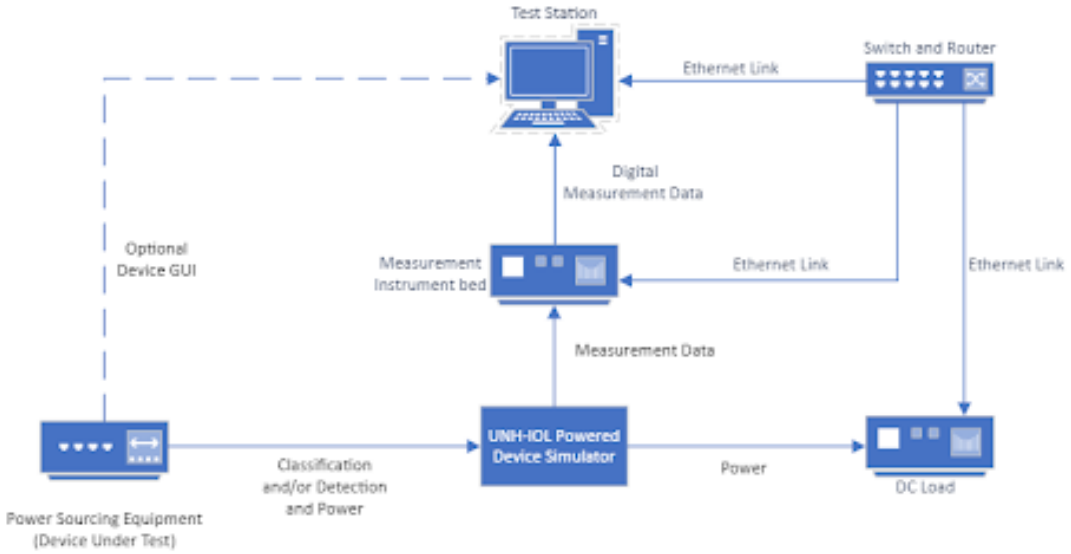

Figure 1: General Test Setup

Test PSE1.5 – PSE Invalid Detection Signature requires a different setup than the General Test Setup. This setup requires the DUT to be connected to a power supply through a coupling network on the Powered Device simulator. This setup yields information as to whether the DUT would attempt to power another PSE. *Figure 2* shows the setup for PSE1.5.

Figure 2: PSE 1.5 Setup

GROUP 1: PSE Detection Characteristics

Overview:

The tests defined in this section verify the detection characteristics of a Power over Data Line (PoDL)/Single-Pair Power over Ethernet (SPoE) Power Sourcing Equipment (PSE), as defined in Clause 104 of the IEEE Std. 802.3-2022. Some of the tests in this group only apply to PSEs not performing classification via SCCP.

Test PSE1.1– PSE Pinout

Purpose: To verify that the PSE has an appropriate connector pin assignment

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.2
[2] IEEE Std. 802.3-2022, Table 104-3
[3] IEEE Std. 802.3bu, PICS PSE1

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- Digital Multimeter

Last Modification: July, 2023

Discussion: A PSE shall implement the PSE pinout in Table 104–3.

Table 104–3—PSE pinout

Contact	PI
1	PI+
2	PI–

Test Setup: Figure 1

Test Procedure:

1. Observe the PoDL connector from the DUT
2. Power the DUT with the applicable auxiliary power
3. Enable the PD simulator and make a voltage measurement using the DMM

Observable Results:

Step	Status	Description
1, 3	PASS	A. The DUT uses a single two-wire connection as illustrated in Table 104-3 for its PI **and** B. The polarity is consistent with Table 104-3
1, 3	FAIL	A. The DUT does not use a single two-wire connection as illustrated in Table 104-3 for its PI

		or B. The polarity is inconsistent with Table 104-3

Possible Problems:

Test PSE1.2 – Detection Probe Requirements

Purpose: To verify that the output current and voltage of the PSE while in the DETECTION state are within the valid range.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.5.1
[2] IEEE Std. 802.3-2022, Tables 104-6, 104-9
[3] IEEE Std. 802.3-2022, PICS PSE6, PSE7

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- Digital Oscilloscope
- Differential Voltage Probe
- Digital Multimeter

Last Modification: April, 2023

Discussion: All detection currents at the PI shall be within the I_{valid} current range, as specified in Table 104–6, when connected to a valid PD detection signature as specified in Table 104–9. The detection probe shall conform to V_{OC}, I_{SC}, I_{slew}, and C_{out} as specified in Table 104–6.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Continuously monitor the current and voltage sourced by the DUT and define these measurements as I_{PSE} and V_{PSE}, respectively
3. Enable the PD Simulator to present a valid detection signature to the DUT and wait at least 500 ms ($T_{Restart}$)
4. Enable the PD Simulator to present a short circuit detection signature to the DUT and wait at least 500 ms ($T_{Restart}$)
   Note - In this step, the short circuit current must be measured 1 ms after the short occurs, in order to allow the current transient to settle
5. Enable the PD Simulator to present an open circuit detection signature to the DUT and wait at least 500 ms ($T_{Restart}$)

Observable Results:

Step	Status	Description
3, 4, 5	**PASS**	A. During detection in step 3, I_{PSE} is in the range of 9 - 16 mA (I_{Valid}) **and** B. During detection in step 4, I_{PSE} does not exceed 24 mA (I_{SC}) **and** C. During detection in step 5, V_{PSE} is in the range of 4.75 - 5.50 V (V_{OC}) **and** D. Outside of detection in steps 3 and 5, V_{PSE} is in the range of 3.15 - 3.575V (V_{Sleep}) **and** E. During detection in steps 3, 4, and 5, the current transient is less than or equal to 1 A/ms (I_{slew})
3, 4, 5	**FAIL**	A. During detection in step 3, I_{PSE} is not in the range of 9 - 16 mA (I_{Valid}) **or** B. During detection in step 4, I_{PSE} exceeds 24 mA (I_{SC}) **or** C. During detection in step 5, V_{PSE} is not in the range of 4.75 - 5.50 V (V_{OC}) **or** D. Outside of detection in steps 3, 4, and 5, V_{PSE} is not in the range of 3.15 - 3.575V (V_{Sleep}) **or** E. During detection in steps 3, 4, and 5, the current transient greater than 1 A/ms (I_{slew})

Possible Problems:

Test PSE1.3 – Detection Timing

Purpose: To verify that a PSE conforms to the timing requirements while in the DETECTION state. This test is applicable to PSEs that do not perform classification via SCCP.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.5
[2] IEEE Std. 802.3-2022, Table 104-6
[3] IEEE Std. 802.3-2022, PICS PSE4

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Digital Oscilloscope
- DC Power Supply
- Differential Voltage Probe
- Digital Multimeter

Last Modification: November, 2023

Discussion: When in the DETECTION state, the PSE shall complete detection of a valid PD signature within T_{det} as specified in Table 104–6. If a valid signature is not detected and classification is not performed, the PSE shall wait at least $T_{Restart}$ before reattempting detection.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Continuously monitor the current sourced by the DUT and the voltage at the DUT PI. Define these measurements as I_{PSE} and V_{PSE}, respectively
3. Enable the PD Simulator to present an invalid detection signature of 3.6 V to the DUT and wait at least 1000 ms
4. Enable the PD Simulator to present a valid detection signature to the DUT and wait at least 1000 ms

Observable Results:

Step	Status	Description
3, 4	**PASS**	A. At all points during the test, the DUT performs detection for no longer than 3.11 ms continuously (T_{det}) **and** B. At all points during the test, the DUT waits for at least 500 ms ($T_{Restart}$) continuously (V_{PSE} in the range of V_{Sleep}) between consecutive detections
3, 4	**FAIL**	A. At any point during the test, , the DUT performs detection for longer than 3.11 ms continuously (T_{det}) **or** B. At any point during the test, the DUT waits for less than 500 ms ($T_{Restart}$) continuously (V_{PSE} in the range of V_{Sleep}) between consecutive detections

Possible Problems:

- This test is only applicable to PSEs that do not perform classification via SCCP
- If a PSE is connected to an invalid signature, it is possible for its detection current to be outside the I_{valid} range. This does not automatically constitute a failure in this test, as the tested PICS only references detection timings. However, this may make observing the occurrence of detection more difficult.

Test PSE1.4– Accept Valid PD Signature

Purpose: To determine the range of detection signatures that a PSE accepts and rejects for a PoDL PD. This test is applicable to PSEs that do not perform classification via SCCP.

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.4.5.2, 104.4.5.3
[2] IEEE Std. 802.3-2022, Table 104-6
[3] IEEE Std. 802.3-2022, PICS PSE8, PSE9

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Digital Oscilloscope
- DC Power Supply
- Digital Multimeter

Last Modification: September, 2023

Discussion: A PSE shall accept as a valid PD signature a link segment with a voltage in the range of 4.05 - 4.7 V (V_{good_PSE}) for at least 1 ms (T_{sig_hold}) in response to a probing current in the range 9 - 16 mA (I_{valid}) as specified in Table 104–6.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Continuously monitor the current sourced by the DUT and the voltage at the DUT PI. Define these measurements as I_{PSE} and V_{PSE}, respectively
3. Enable the PD Simulator to present an invalid detection signature of 3.6 V to the DUT and wait at least 500 ms ($T_{Restart}$)
4. Increase the detection signature by 0.05 V and wait at least 500 ms ($T_{Restart}$) or until the DUT transitions to the POWER_UP state
5. Reset the DUT
6. Enable the PD Simulator to present an invalid detection signature of 5.65 V to the DUT and wait at least 500 ms ($T_{Restart}$)
7. Decrease the detection signature by 0.05 V and wait at least 500 ms ($T_{Restart}$) until the DUT transitions to the POWER_UP state
8. Reset the DUT
9. Enable the PD Simulator to present a valid detection signature to the DUT. Mark the start of detection as t = 0
10. At t = 0.9 ms, remove the valid detection signature and wait at least 500 ms ($T_{Restart}$)
11. Enable the PD Simulator to present a valid detection signature to the DUT. Mark the start of detection as t = 0
12. At t = 1.1 ms, remove the valid detection signature and wait at least 500 ms

Observable Results:

Step	Status	Description
4, 7, 10, 12	**PASS**	A. The DUT rejects voltage signatures below 3.7 V ($V_{bad\_lo\_PSE}$) or above 5.45 V ($V_{bad\_hi\_PSE}$) **and** B. The DUT accepts voltage signatures in the range of 4.05 V - 4.7 V (V_{good_PSE}) **Note –** The DUT may accept voltage signatures in the ranges between V_{bad} and V_{good} **and** C. The DUT rejects voltage signatures that are present for less than 1 ms (T_{sig_hold}) **and** D. The DUT accepts voltage signatures that are present for more than 1 ms (T_{sig_hold})
4, 7, 10, 12	**FAIL**	A. The DUT accepts a voltage signature below 3.7 V ($V_{bad\_lo\_PSE}$) or above 5.45 V ($V_{bad\_hi\_PSE}$) **or** B. The DUT rejects a voltage signature in the range of 4.05 V - 4.7 V (V_{good_PSE}) **or** C. The DUT accepts voltage signatures that are present for less than 1 ms (T_{sig_hold}) **or** D. The DUT rejects voltage signatures that are present for more than 1 ms (T_{sig_hold})

Possible Problems:

- A PSE may successfully detect a PD but then opt not to power the detected PD. It also may be difficult to determine the start of detection and when to remove the detection signature in Steps 10 and 12.
- This test is only applicable to PSEs that do not perform classification via SCCP

Test PSE1.5– PSE Invalid Detection Signature

Purpose: To ensure that a PSE presents an invalid PD detection signature when connected to another PSE

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.7
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3bu, PICS PSE13

Resource Requirements:

- DC Power Supply
- Digital Multimeter

Last Modification: June, 2022

Discussion: To prevent a PSE from applying power to another PSE, each PSE must present an invalid detection signature. For a probe current in the range of 7 mA to 17 mA, the PSE must present a signature voltage greater than 5.15 V or less than 3.7 V.

Test Setup: **Figure 2**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Continuously monitor the current sourced to/from the DUT and the voltage at the DUT PI. Define these measurements as I_{PI} and V_{PI}, respectively
3. Enable the second DC power supply so that it presents 6 V to the DUT PI with a current limit of 7 mA
4. Increase the current limit of the DC power supply by 1 mA
5. Repeat step 4 until the current limit reaches 17 mA

Observable Results:

Step	Status	Description
3, 4, 5	**PASS**	A. The DUT presents a voltage signature below 3.7 V ($V_{bad\_lo\_PSE}$) or above 5.45 V ($V_{bad\_hi\_PSE}$) when driven with a test current in the range of 7 - 17 mA
3, 4, 5	**FAIL**	A. The DUT does not present a voltage signature below 3.7 V ($V_{bad\_lo\_PSE}$) or above 5.45 V ($V_{bad\_hi\_PSE}$) when driven with a test current in the range of 7 - 17 mA

Possible Problems:

- If the DUT fails, this test may cause permanent damage and should therefore be performed last
- It may not be possible to source sufficient current to the DUT when applying 6 V. In this case, the DUT passes the test

GROUP 2: PSE Power Characteristics

Overview:

The tests defined in this section verify that a Power over Data Line (PoDL) or Single Pair Power over Ethernet (SPoE) Power Sourcing Equipment (PSE) conforms to the output requirements defined in Subclause 104 of the IEEE Std. 802.3-2022.

Test PSE2.1 – Output Voltage and Current in POWER_ON State

Purpose: To verify the output voltage, current, and power characteristics of the PSE while in the POWER_ON state

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.3, 104.4.3, 104.4.7.7
[2] IEEE Std. 802.3-2022, Tables 104-1, 104-2
[3] IEEE Std. 802.3-2022, PICS PSE12, PSE14, PSE31, PSE32, PSE33

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- Digital Multimeter
- DC Programmable Load

Last Modification: January, 2024

Discussion: A PSE operating under nominal conditions in the POWER_ON state should apply a voltage in the range of $V_{PSE(ON)}$, which is between $V_{PSE(min)}$ and $V_{PSE(max)}$

Table 104–1—Class power requirements matrix for PSE, PI, and PD

	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	0	1	2	3	4	5	6	7	8	9
$V_{PSE(max)}$ (V)[a]	18	18	18	18	36	36	36	36	60	60
$V_{PSE\_OC(min)}$ (V)[b]	6	6	14.4	14.4	12	12	26	26	48	48
$V_{PSE(min)}$ (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48
$I_{PI(max)}$ (mA)[c]	101	227	249	471	97	339	215	461	735	1 360
$P_{Class(min)}$ (W)[d]	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3
$V_{PD(min)}$ (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7
$P_{PD(max)}$ (W)[e]	0.5	1	3	5	1	3	5	10	30	50

Table 104–2—Class power requirements matrix for PSE, PI, and PD for classes 10 through 15

Class	10	11	12	13	14	15
$V_{PSE(max)}$ (V)	30	30	30	58	58	58
$V_{PSE\_OC(min)}$ (V)	20	20	20	50	50	50
$V_{PSE(min)}$ (V)	20	20	20	50	50	50
$I_{PI(max)}$ (mA)	92	240	632	231	600	1579
$P_{class(min)}$ (W)	1.85	4.8	12.63	11.54	30	79
$V_{PD(min)}$ (V)	14	14	14	35	35	35
$P_{PD(max)}$ (W)	1.23	3.2	8.4	7.7	20	52

Test Setup: Figure 1

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Enable the PD Simulator to present a valid power up sequence to the DUT
3. When the DUT enters the POWER_UP state, configure the programmable load to draw 11 mA (I_{hold_PD})
4. Continuously measure the voltage at the DUT PI and define it as V_{PSE}
5. Increase the current draw of the programmable load by 1 mA and wait at least 75 ms (T_{LIM_MAX})
6. Repeat step 5 until power is removed
7. Disable the DUT
8. Power the DUT with the applicable auxiliary power
9. Enable the PD Simulator to present a valid power up sequence to the DUT
10. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}$/ V_{PSE}
11. Measure the average power sourced by the DUT for 3 seconds and record the measurement as P_{PSE}

Note - The average power is calculated using a sliding window with a width of 1 second, according to the equation below

$$P_{PSE} = \int_{T_0}^{T_0 + 1\,s} V_{PSE}(t) * I_{PSE}(t)\, dt$$

Observable Results:

Step	Status	Description
6, 11	**PASS**	A. All measurements of V_{PSE} are within the range of $V_{PSE(min)}$ and $V_{PSE(max)}$ for the DUT power class **and** B. The DUT does not source more than $I_{PI(max)}$ for the DUT power class **and** C. The measurement of P_{PSE} is greater than or equal to $P_{Class(min)}$ for the DUT power class
6, 11	**FAIL**	A. At least one measurement of V_{PSE} is outside the range of $V_{PSE(min)}$ and $V_{PSE(max)}$ for the DUT power class **or** B. The DUT sources more than $I_{PI(max)}$ for the DUT power class **or** C. The measurement of P_{PSE} is not greater than or equal to P_{Class} for the DUT power class

Possible Problems:

Test PSE2.2 – Open Circuit Voltage in POWER_ON State

Purpose: To verify that the voltage at the PSE PI is greater than $V_{PSE\_OC(min)}$ when presented with an open circuit in the POWER_ON state

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.3, 104.4.3
[2] IEEE Std. 802.3-2022, Tables 104-1, 104-2
[3] IEEE Std. 802.3-2022, PICS PSE2

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- Digital Multimeter
- DC Programmable Load

Last Modification: June, 2022

Discussion: $V_{PSE\_OC(min)}$ is the minimum allowed open circuit voltage measured at the PSE PI in the POWER_ON state

Table 104–1—Class power requirements matrix for PSE, PI, and PD

	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	0	1	2	3	4	5	6	7	8	9
$V_{PSE(max)}$ (V)[a]	18	18	18	18	36	36	36	36	60	60
$V_{PSE\_OC(min)}$ (V)[b]	6	6	14.4	14.4	12	12	26	26	48	48
$V_{PSE(min)}$ (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48
$I_{PI(max)}$ (mA)[c]	101	227	249	471	97	339	215	461	735	1 360
$P_{Class(min)}$ (W)[d]	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3
$V_{PD(min)}$ (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7
$P_{PD(max)}$ (W)[e]	0.5	1	3	5	1	3	5	10	30	50

Table 104–2—Class power requirements matrix for PSE, PI, and PD for classes 10 through 15

Class	10	11	12	13	14	15
$V_{PSE(max)}$ (V)	30	30	30	58	58	58
$V_{PSE\_OC(min)}$ (V)	20	20	20	50	50	50
$V_{PSE(min)}$ (V)	20	20	20	50	50	50
$I_{PI(max)}$ (mA)	92	240	632	231	600	1579
$P_{class(min)}$ (W)	1.85	4.8	12.63	11.54	30	79
$V_{PD(min)}$ (V)	14	14	14	35	35	35
$P_{PD(max)}$ (W)	1.23	3.2	8.4	7.7	20	52

Test Setup: Figure 1

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Enable the PD Simulator to present a valid power up sequence to the DUT When the DUT enters the POWER_UP state, configure the programmable load to draw 11 mA (I_{hold_PD}) and wait at least 6 ms (T_{MFVS})
3. Continuously measure the voltage at the DUT PI and define it as V_{PSE}
4. Configure the programmable load to draw 0 mA and wait for no more than 300 ms ($T_{MFVDO(min)}$)

Observable Results:

Step	Status	Description
5	**PASS**	A. All measurements of V_{PSE} are greater than or equal $V_{PSE\_OC(min)}$ for the DUT power class
5	**FAIL**	A. At least one measurement of V_{PSE} is less than $V_{PSE\_OC(min)}$ for the DUT power class

Possible Problems:

Test PSE2.3 – Output Voltage and Current at Overload Condition

Purpose: To verify the output voltage and current are limited when the PSE transitions from the POWER_ON state to the OVERLOAD, OVERLOAD_DELAY, or DISABLED state

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.4.7.1, 104.4.7.2.1
[2] IEEE Std. 802.3-2022, Tables 104-6, 104-7
[3] IEEE Std. 802.3-2022, PICS PSE15, PSE20, PSE21, PSE23

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- DC Programmable Load
- Digital Multimeter

Last Modification: June, 2022

Discussion: A PSE shall apply a voltage at the PI in the range of $V_{Disable}$ when in the OVERLOAD, OVERLOAD_DELAY, or DISABLED state. During operation in the POWER_UP and POWER_ON states, the PSE shall limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI as specified in Table 104–7.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Enable the PoDL PD Simulator to present a valid power up sequence to the DUT
3. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}/ V_{PSE}$ for the DUT power class and wait at least 500 ms
4. Increase the programmable load current by 1 mA and wait at least 75 ms
5. Repeat step 4 until power is removed (V_{PSE} is less than or equal to 1 V ($V_{Disable}$))
6. Repeat the test (steps 1 - 3)
7. Configure the programmable load to draw $1.41*I_{PI(max)}$ for the DUT power class
8. Repeat the test (steps 1 - 3)
9. Configure the programmable load to present a short circuit to the DUT
   Note - In this step the current must be measured 1 ms after the short is applied to allow the transient to settle

Observable Results:

Step	Status	Description
5, 7, 9	**PASS**	A. The maximum current sourced by the DUT is less than or equal to $1.41*I_{PI(max)}$ for the DUT power class **and** B. When the DUT enters the OVERLOAD state, it maintains the load for at least 10 ms but no longer than 75 ms (T_{LIM}) for power classes 0 - 9 and for at least 50 ms but no longer than 75 ms for power classes 10 - 15 **and** C. When the DUT is disabled due to an overload, its output voltage is less than or equal to 1 V ($V_{disable}$)
5, 7, 9	**FAIL**	A. The maximum current sourced by the DUT is greater than $1.41*I_{PI(max)}$ for the DUT power class **or** B. When the DUT enters the OVERLOAD state, it disables before 10 ms or after 75 ms (T_{LIM}) for power classes 0 - 9 or before 50 ms or after 75 ms for power classes 10 - 15 **or** D. When the DUT is disabled due to an overload, its output voltage is greater than 1 V ($V_{disable}$)

Possible Problems:

Test PSE2.4 – Enter Sleep State

Purpose: To ensure the PSE enters the SLEEP state properly and exhibits the correct current and voltage characteristics while in this state.

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.4.7.1, 104.4.7.2
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE17, PSE18, PSE19, PSE23

Resource Requirements:

- UNH-IOL PSE Test Board
- DC Power Supply
- DC Programmable Load
- Digital Oscilloscope
- Digital Multimeter

Last Modification: June, 2022

Discussion: A PSE enters the SLEEP state when the PD does not present a valid Maintain Full Voltage Signature (MFVS). A PSE entering the SLEEP state must discharge the PI to the range of 3.15 V to 3.575 V (V_{Sleep}) within 500 ms (T_{OFF}), and the discharge current should be limited to between 1.2 mA and 24 mA ($I_{dishcharge}$)

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Enable the PSE Test Board to present a valid power up sequence to the DUT
3. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}$/ V_{PSE} for the DUT power class and wait at least 500 ms
4. Disable the detection signature
5. Measure the voltage and current at the DUT PI continuously and define these measurements as V_{PI} and I_{PI}, respectively
6. Configure the PD Simulator to draw 0.1 mA (I_{Sleep_PD})
7. Disable the programmable load

Observable Results:

Step	Status	Description
7	**PASS**	A. V_{PI} reaches 3.575 V ($V_{Sleep(max)}$) within 500 ms (T_{OFF}) of V_{PI} dropping 1 V below the steady-state full operating voltage value **or** B. V_{PI} does not reach 3.575 V ($V_{Sleep(max)}$) within 500 ms (T_{OFF}) of V_{PI} dropping 1 V below the steady-state full operating voltage value and instead current limits and disables the PI **and** C. I_{PI} is in the range of 1.2 mA - 24 mA ($I_{discharge}$) while V_{PI} is decreasing and still above 3.575 V **and** D. Once discharged, V_{PI} remains in the range of 3.15 V to 3.575 V (V_{Sleep})

7	**FAIL**	A. V_{PI} does not reach 3.575 V ($V_{Sleep(max)}$) within 500 ms (T_{OFF}) of V_{PI} dropping 1 V below the steady-state full operating voltage value **and** B. V_{PI} does not disable the PI when 3.575 V ($V_{Sleep(Max)}$) **or** C. I_{PI} is outside the range of 1.2 mA - 24 mA ($I_{discharge}$) while V_{PI} is decreasing and still above 3.575 V **or** D. Once discharged, V_{PI} does not remain in the range of 3.15 V to 3.575 V (V_{Sleep})

Possible Problems:

Test PSE2.5 – PSE Wakeup

Purpose: To verify that a PSE responds properly to wakeup requests from the SLEEP state and successfully transitions to DETECTION.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.7.2.2
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE25, PSE26

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- DC Programmable Load
- Digital Oscilloscope
- Digital Multimeter

Last Modification: November, 2023

Discussion: A PSE shall transition from the SLEEP state to the DETECTION state when I_{PSE} is in the range of 1.25 mA to 1.85 mA (I_{Wakeup}) for at least 0.1 ms (T_{Wakeup}). A PSE shall remain in the SLEEP state when I_{PSE} is greater than 2.5 mA ($I_{Wakeup\_bad\_hi}$) and less than 0.5 mA ($I_{Wakeup\_bad\_lo}$). A PSE may consider a PD wakeup request valid or invalid if I_{PSE} is in the band between $I_{Wakeup\_bad\_hi}$ and I_{Wakeup} max or the band between I_{Wakeup} min and $I_{Wakeup\_bad\_lo}$.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power and disable the PHY
2. Enable the PD Simulator to present a valid power up sequence to the DUT
3. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}/ V_{PSE}$ for at least 500 ms ($T_{Restart}$)
4. Set the wakeup current on the PD Simulator current sink to 0.3 mA
5. Disable the programmable load and wait at least 900 ms ($T_{MFVDO(max)} + T_{OFF}$)
6. Increase the current draw of the PD Simulator current sink by 20 uA and wait at least 0.1 ms (T_{Wakeup})
7. Repeat step 6 until the DUT enters the DETECTION state
8. Disable the DUT
9. Power the DUT with the applicable auxiliary power and disable the PHY
10. Enable the PD Simulator to present a valid power up sequence to the DUT
11. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}/ V_{PSE}$ for at least 500 ms ($T_{Restart}$)
12. Set the detection current on the PD Simulator current sink to 3 mA
13. Disable the programmable load and wait at least 900 ms ($T_{MFVDO(max)} + T_{OFF}$)
14. Decrease the current draw of the PD Simulator current sink by 20 uA wait at least 0.1 ms (T_{Wakeup})
15. Repeat step 14 until the DUT enters the DETECTION state

Observable Results:

Step	Status	Description
7, 15	**PASS**	A. The DUT reattempts detection when I_{PI} is greater than or equal to 1.25 mA ($I_{Wakeup(min)}$) and less than or equal to 1.85 mA ($I_{Wakeup(max)}$) **and** B. The DUT does not reattempt detection when I_{PI} is less than 0.5 mA ($I_{Wakeup\_bad\_loi}$) or greater than or equal to 2.5 mA ($I_{Wakeup\_bad\_hi}$) **Note –** The DUT may reattempt detection when I_{PI} is in between the range of I_{Wakeup} and I_{Wakeup_bad} **and** C. When the DUT reattempts detection, the wakeup signature has been present for at least 0.1 ms (T_{Wakeup})
7, 15	**FAIL**	A. The DUT reattempts detection when I_{PI} is less than 0.5 mA ($I_{Wakeup\_bad\_lo}$) or greater than 2.5mA ($I_{Wakeup\_bad\_hi}$) **or** B. The DUT does not reattempt detection when I_{PI} is in the range of 1.25 mA - 1.85 mA (I_{Wakeup}) **or** C. When the DUT reattempts detection, the wakeup signature has been present for less than 0.1 ms (T_{Wakeup})

Possible Problems:

Test PSE2.6 – Idle State

Purpose: To ensure the PSE is conformant when transitioning through the IDLE state.

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.4.7.2.1, 104.4.7.2.3
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE23, PSE27, PSE28

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- DC Programmable Load
- Digital Oscilloscope
- Digital Multimeter

Last Modification: November, 2023

Discussion: A PSE enters the IDLE state at least 750 ms (T_{od}) after an overload and before restarting detection. While in the IDLE state, a PSE must apply a voltage to the PI that is in the range of 3.15 V to 3.575 V (V_{Sleep}) . A PSE should transition out of IDLE when I_{PSE} is less than 1.85 mA ($I_{Wakeup(max)}$) for at least 0.1 ms (T_{Wakeup}), and it should remain in IDLE for I_{PSE} greater than 2.5 mA ($I_{Wakeup\_bad\_hi}$).

Test Setup: **Figure 1**
lim
Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Enable the PD Simulator to present a valid power up sequence to the DUT
3. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}$/ V_{PSE} for 500 ms ($T_{Restart}$)
4. Configure the programmable load to present a short circuit
5. Measure the time when the DUT limits the current on the PI and mark this as T_0
6. Measure the time when the DUT disables the PI ($V_{Disable}$) and mark this as T_1
7. Disable the short circuit
8. Configure the PD Simulator current sink to draw 3 mA
9. Measure the time when the DUT begins to source more than 1.85mA and mark this as T_2
10. Decrease the load current by 20 µA and wait at least 1.5 s ($2*T_{od}$)
11. Repeat step 10 until the DUT enters the DETECTION state

Observable Results:

Step	Status	Description
5, 6, 9, 11	**PASS**	A. The DUT enters the IDLE state at least 750 ms (T_{od}) after entering the OVERLOAD state (T_2 - T_1) **and** B. The DUT disables the PI within 75ms (T_{LIM}) after limiting the current (T_1 - T_0) **and** C. The DUT reenters the IDLE state when I_{PI} is less than or equal to 2.5 mA ($I_{Wakeup\_bad\_hi}$) for at least 0.1 ms (T_{Wakeup}) **and** D. V_{PSE} is in the range of V_{Sleep} (3.15-3.575V) at the end of step 8

5, 6, 9, 11	**FAIL**	A. The DUT enters the IDLE state less than 750 ms (T_{od}) after entering the OVERLOAD state (T_2 - T_1) **or** B. The DUT does not disable the PI within 75ms (T_{LIM}) after limiting the current (T_1 - T_0) **or** C. The DUT reenters the DETECTION state when I_{PI} is greater than 2.5 mA ($I_{Wakeup\_bad\_hi}$) or when I_{PI} is less than 2.5 mA for less than 0.1 ms (T_{Wakeup}) **or** D. V_{PSE} is not in the range of V_{Sleep} (3.15-3.575V) at the end of step 8

Possible Problems:

Test PSE2.7 – Power Feeding Ripple and Transients

Purpose: To ensure data integrity is maintained by verifying the PSE meets the appropriate ripple and transient limits.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.7.3
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, Figure 104-7
[4] IEEE Std. 802.3-2022, Equations 104-1, 104-2, 104-3

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- DC Programmable Load
- Digital Oscilloscope

Last Modification: April, 2023

Discussion: A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI of the PSE device under test (DUT) as shown in Figure 104–7. The input impedance, Zin(f), and transfer function, H1(f), of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PSE as specified by Table 104–7 item (4a), f1 = 31.8 kHz ± 1%. When measuring the ripple voltage for a Type B or Type F PSE as specified in Table 104–7 item (4a), f1 = 318 kHz ± 1%. When measuring the ripple voltage for a Type E PSE as specified in Table 104–7 item (4a), f1 = 3.18 kHz ± 1%.

When measuring the ripple voltages for a Type A or Type C PSE as specified by Table 104–7 item (4b), the voltage observed at the MDI/PI with the differential probe where f1 = 31.8 kHz ± 1% is post-processed with transfer function H2(f) specified in Equation (104–3) where f2 = 1 MHz ± 1%. When measuring the ripple voltages for a Type B or Type F PSE as specified by Table 104–7 item (4b), the voltage observed at the MDI/PI with the differential probe where f1 = 318 kHz ± 1% is post-processed with transfer function H2(f) specified in Equation (104–3) where f2 = 10 MHz ± 1%. When measuring the ripple voltages for a Type E PSE as specified by Table 104–7 item (4b), the voltage observed at the MDI/PI with the differential probe where f1 = 3.18 kHz ± 1% is post-processed with transfer function H2(f) specified in Equation (104–3) where f2 = 0.1 MHz ± 1%.

$$Z_{in}(f) = 100\Omega \pm 0.1\% \times \frac{\sqrt{f^2 + f_1^2}}{f} \quad (104\text{–}1)$$

$$H_1(f) = \frac{f}{\sqrt{f^2 + f_1^2}} \quad (104\text{–}2)$$

$$H_2(f) = \frac{f}{\sqrt{f^2 + f_2^2}} \quad (104\text{–}3)$$

Test Setup: Figure 1

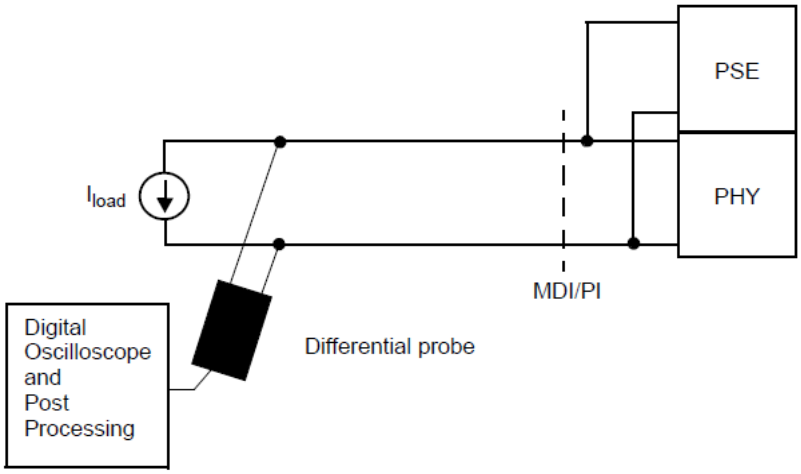

Figure 104–7—PSE ripple voltage test fixture

Test Procedure:

1. Power the DUT with the applicable auxiliary power and disable the PHY
2. Enable the PD Simulator to present a valid power up sequence to the DUT
3. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}/ V_{PSE}$ for 500 ms ($T_{Restart}$)
4. Select the appropriate transfer function H1(f) for the DUT type and apply it to the probe
   Note - The transfer function represents a passive first order high-pass filter network at the probe input. Assuming a 100 Ω differential probe impedance, this corresponds to a balanced configuration of 2x 1 µF for type E devices, 2x 100 nF for type A and C devices, and 2x 10 nF for type B or type F devices
5. Measure the peak to peak voltage noise at the DUT PI
6. Apply the appropriate transfer function $H_2(f)$ for the DUT type in post-processing
   Note – For type A and type C devices, $f_2 = 1$ MHz. For type B or type F devices, $f_2 = 10$ MHz. For type E devices, $f_2 = 0.1$ MHz
7. Repeat the test (steps 1 - 6) with step 3 modified so that the programmable load is configured to draw 11 mA (I_{hold})

Observable Results:

Step	Status	Description
5, 6	**PASS**	A. All measurements in step 5 are less than or equal to 0.1 V_{PP} **and** B. All measurements in step 6 are less than or equal to 0.01 V_{PP}
5, 6	**FAIL**	A. At least one measurement in step 5 is greater than 0.1 V_{PP} **or** B. At least one measurement in step 6 is greater than 0.01 V_{PP}

Possible Problems:

Test PSE2.8 – Output Voltage Slew Rate

Purpose: To ensure the PSE limits its output voltage slew rate under varying load conditions

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.7
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE12

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- DC Programmable Load
- Digital Oscilloscope

Last Modification: March, 2023

Discussion: A PSE must limit its output voltage slew rate when in the POWER_ON state in order to prevent disturbance of the link during load transients. For Type A and C devices, the maximum allowed slew rate is 22 V/ms. For Type B and F devices, the maximum allowed slew rate is 200 V/ms. For Type E devices, the maximum allowed slew rate is 2 V/ms. Additionally, Type A, C, and E devices have a maximum allowed slew rate of 40 V/ms when performing inrush in the POWER_UP state.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Enable the PD Simulator to present a valid power up sequence to the DUT
3. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}/ V_{PSE}$ for at least 500 ms ($T_{Restart}$)
4. Continuously measure the output voltage at the DUT PI and define this measurement as V_{PI}
5. Configure the programmable load to present triangular current waveform varying from 11 mA (I_{Hold}) to $P_{Class(min)}/ V_{PSE}$ with the maximum possible current slew rate
6. Record the maximum observed voltage slew rate from the time derivative of V_{PI}
7. If the DUT is a Type A, C, or E device, proceed to step 8. Otherwise, the test is concluded
8. Remove power from the DUT and wait at least 6 seconds
9. Power the DUT with the applicable auxiliary power
10. Enable the PD Simulator to present a valid power up sequence to the DUT
11. When the DUT enters the POWER_UP state, configure the programmable load to draw $1.41*I_{PI(max)}$ ($I_{(LIM)}$)

Observable Results:

Step	Status	Description
6, 11	**PASS**	A. The DUT is a type A or C device and has a maximum voltage slew rate in the POWER_ON state less than or equal to 22 V/ms **or** B. The DUT is a type B device and has a maximum voltage slew rate less in the POWER_ON state less than or equal to 200 V/ms **or** C. The DUT is a type E device and has a maximum voltage slew rate less in the POWER_ON state less than or equal to 2 V/ms **and** D. The DUT is a type A, C, or E device and has a maximum voltage slew rate in the POWER_UP state less than or equal to 40 V/ms (only applicable to type A, C, and E DUTs)
6, 11	**FAIL**	A. The DUT is a type A or C device and has a maximum voltage slew rate in the POWER_ON state greater than 22 V/ms **or** B. The DUT is a type B device and has a maximum voltage slew rate less in the POWER_ON state greater than 200 V/ms **or** C. The DUT is a type E device and has a maximum voltage slew rate less in the POWER_ON state greater than to 2 V/ms **or** D. The DUT is a type A, C, or E device and has a maximum voltage slew rate in the POWER_UP state greater 40 V/ms

Possible Problems:

Test PSE2.9 – Inrush Time

Purpose: To ensure the PSE properly transitions through the POWER_UP state

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.7.4
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE29, PSE30

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Digital Oscilloscope
- DC Power Supply
- DC Programmable Load

Last Modification: September, 2023

Discussion: After completion of detection and optional classification, the PSE attempts to power the PD. If the PSE is able to apply full operating voltage to the PI within $T_{Inrush(min)}$, it must enter the POWER_ON state. If the PSE takes longer than $T_{Inrush(max)}$ to apply the full operating voltage, the PSE must begin a new detection cycle after a delay of 500 ms ($T_{Restart}$) before attempting to reapply power. If full operating voltage is applied within the range of T_{Inrush}, the PSE may enter the POWER_ON state or begin a new detection cycle after a delay of $T_{Restart}$.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Continuously measure voltage at the DUT PI
3. Enable the PD Simulator to present a valid power up sequence to the DUT
4. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}$/ V_{PSE}
5. Measure the time between the DUT entering POWER_UP and the application of full operating voltage
6. Repeat the test (steps 1 - 5) with step 4 modified so that the programmable load is configured to draw 1.41*$I_{PI(max)}$ (I_{LIM})
7. Repeat the test (steps 1 - 5) with step 4 modified so that the programmable load is configured to present a short circuit to the DUT. Replace the short with a load of $P_{Class(min)}$/ V_{PSE} after $T_{Inrush(max)}$ + 0.2 ms

Observable Results:

Step	Status	Description
5, 6, 7	**PASS**	A. The DUT applies operating voltage ($V_{PSE(PON)}$) within $T_{Inrush(min)}$ (3.17 ms for class 0 - 9 devices or 50 ms for class 10 to 15 devices) of entering the POWER_UP state and it proceeds to the POWER_ON state **or** B. The DUT does not apply operating voltage (in the range of $V_{PSE(PON)}$) within $T_{Inrush(max)}$ (3.87 ms for class 0 - 9 devices or 75 ms for class 10 to 15 devices) of entering the POWER_UP state and it proceeds to the RESTART state
5, 6, 7	**FAIL**	A. The DUT applies operating voltage (in the range of $V_{PSE(PON)}$) within $T_{Inrush(min)}$ (3.17 ms for class 0 - 9 devices or 50 ms for class 10 to 15 devices) of entering the POWER_UP state and does not proceed to the POWER_ON state **or**

		B. The DUT does not apply operating voltage (in the range of $V_{PSE(PON)}$) within $T_{Inrush(max)}$ (3.87 ms for class 0 - 9 devices or 75 ms for class 10 to 15 devices) of entering the POWER_UP state and it proceeds to the POWER_ON state

Possible Problems:

Test PSE2.10 – Disable Time

Purpose: To ensure the PSE removes power within the allotted time after PoDL has been disabled.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.7.5
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE31

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Digital Multimeter
- DC Power Supply
- DC Programmable Load

Last Modification: June, 2022

Discussion: When PoDL is disabled, the discharge time of the PI from V_{PSE} to 1V with a test resistor of 320kΩ attached to the PI shall be less than $T_{Disable}$, or 500ms. $T_{Disable}$ starts when the voltage drops 1V below the steady-state operating voltage at the PI. $T_{Disable}$ ends when V_{PSE} is less than V_{Sleep} max.

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Continuously measure voltage at the DUT PI and define the measurement as V_{PI}
3. Enable the PD Simulator to present a valid power up sequence to the DUT
4. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}$/ V_{PSE}
5. Insert a 320 kΩ test resistor across the DUT PI
6. Disable the DUT PoDL capabilities and disable the programmable load
7. Mark as t0 the moment when V_{PI} drops 1 V below the steady-state value in the POWER_ON state
8. Mark as t1 the moment when V_{PI} is less than or equal to 1 V ($V_{Disable}$)
9. Calculate the disable time as t1 - t0

Observable Results:

Step	Status	Description
9	**PASS**	A. The DUT disables within 500 ms ($T_{Disable}$)
9	**FAIL**	A. The DUT disables after 500 ms ($T_{Disable}$)

Possible Problems:

- It may not be possible to manually disable or reset PoDL on the PSE

Test PSE2.11 – Maintain Full Voltage Signature (MFVS)

Purpose: To verify that the PSE sources and removes power according to the PD MFVS.

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.4.8, 104.4.8.1
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE34, PSE35, PSE36, PSE37

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- DC Power Supply
- DC Programmable Load
- Digital Multimeter

Last Modification: June, 2022

Discussion: A PD's MFVS is considered present by the PSE when I_{PSE} is greater than or equal to 10 mA ($I_{Hold(max)}$) for a minimum of 6 ms (T_{MFVS}) followed by an optional dropout period of 300 ms or less ($T_{MFVDO(min)}$). MFVS is considered absent if I_{PSE} is less than 2.5 mA ($I_{Hold(min)}$) or if the dropout period is longer than 400 ms ($T_{MFVDO(max)}$). The PSE-PI Voltage shall be reduced to the range of V_{Sleep} when MFVS has been absent for a duration greater than $T_{MFVDO.}$

Test Setup: **Figure 1**

Test Procedure:

1. Power the DUT with the applicable auxiliary power
2. Continuously measure voltage at the DUT PI and define the measurement as V_{PI}
3. Enable the PD Simulator to present a valid power up sequence to the DUT
4. When the DUT enters the POWER_UP state, configure the programmable load to draw $P_{Class(min)}$/ V_{PSE} and wait at least 500 ms (T_{Reset})
5. Configure the programmable load so that it draws 11 mA for 6.5 ms followed by no load for 298 ms. Allow this pattern to repeat for 10 cycles
6. Configure the programmable load so that it draws 11 mA for 6.5 ms followed by no load for 402 ms. Allow this pattern to repeat for 10 cycles
   Note - The DUT is expected to enter the SLEEP state during this step. If this is true, the DUT must be restarted per steps 1 - 4 before advancing to the next step
7. Configure the programmable load so that it draws 11 mA for 6.5 ms followed by no load for 298 ms. Allow this pattern to repeat indefinitely
8. Reduce the 11 mA portion of the load cycle by 0.5 mA and wait at least 850 ms
9. Repeat step 8 until the DUT enters the SLEEP state

Observable Results:

Step	Status	Description
5, 6, 9	**PASS**	A. In step 5, the DUT remains in the POWER_ON state **and** B. In step 6, the DUT transitions to the SLEEP state (V_{PI} in the range of V_{Sleep}) **and** C. In step 9, the DUT transitions to the SLEEP state when the MFV signature is between 2.5 mA - 10 mA (I_{Hold})
5, 6, 9	**FAIL**	A. In step 5, the DUT does not remain in the POWER_ON state **or** B. In step 6, the DUT does not transition to the SLEEP state (V_{PI} in the range of V_{Sleep}) **or** C. In step 9, the DUT does not transition to the SLEEP state when the MFV signature is between 2.5 mA - 10 mA (I_{Hold})

Possible Problems:

GROUP 3: PSE SCCP Characteristics

Overview:

The tests defined in this section verify the Serial Communication Classification Protocol (SCCP) implementation of a Power over Data Line (PoDL)/Single-Pair Power over Ethernet (SPoE) Power Sourcing Equipment (PSE), as defined in Clause 104 of the IEEE Std. 802.3-2022 and IEEE Std. 802.3dd. SCCP is a current-sinking, open-drain protocol that relies on a PSE master device to initiate transactions and to provide the necessary pull-up current. SCCP includes functions that allow a connected PD to communicate its class data and perform optional cable resistance measurements for advanced power negotiation.

The following tests apply to all PoDL/SPoE PSEs implementing classification via SCCP.

Editor's Note: The set of test requirements in group 3 are only valid for Type E PSEs. Conformance requirements for types A, B, C, D, and F may be added at a later date.

Test PSE3.1 – SCCP Initialization

Purpose: To verify that a PSE properly issues an SCCP reset pulse before beginning transactions with a connected PD

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.1.1
[2] IEEE Std. 802.3-2022, Figure 104-10
[3] IEEE Std. 802.3dd, Table 104-12
[4] IEEE Std. 802.3-2022, PICS SCCP2, SCCP3, SCCP22

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Power Supply
- Oscilloscope

Last Modification: January, 2024

Discussion: All SCCP communication with a PD shall begin with an initialization sequence that consists of a reset pulse from the PSE followed by a presence pulse from the PD. During the initialization sequence the PSE shall transmit the reset pulse by first driving V_{PSE} low and then releasing to the pull up at t_{RSTL}. The PSE shall then go into receive mode (RX). When the PD detects the rising edge at the PD PI, it shall wait t_{PDH} and then transmit a presence pulse by pulling V_{PD} low for t_{PDL}. Presence data from the PD shall be valid for the entire time window defined by t_{MSP} following the rising edge that terminated the reset pulse. Therefore, the PSE should sample the subsequent voltage within t_{MSP} from the completion of the preceding rising edge at its PI.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid wakeup current and detection signature to the DUT
2. Wait until the DUT output voltage is between 4.7 V and 5.5 V (SCCP idle voltage, V_{PUP})
3. Mark the moment V_{PSE} drops to 2 V (V_{TL}) as t = 0
4. Mark the moment V_{PSE} rises to 3 V (V_{TH}) after t = 0 as t_1
5. At t = t_1 + 1 ms (t_{PDH}), use the PoDL PD Simulator to pull the SCCP line low
6. At t = t_1 + 26 ms (t_{PDL}), use the PoDL PD Simulator to release the SCCP line
7. Repeat the test (steps 1 – 6) with step 5 modified so that the SCCP line is pulled low at t = t_1 + 1.78 ms ($t_{MSP(min)}$ – 0.02 ms)
8. Repeat the test (steps 1 – 6) with step 5 modified so that the SCCP line is pulled low at t = t_1 + 2.42 ms ($t_{MSP(max)}$ + 0.02 ms)

Observable Results:

Step	Status	Description
4, 6	**PASS**	a. T_1 is in the range of 8 – 10.5 ms (t_{RSTL}) **and** b. After step 6 (first and second iterations), the DUT issues a broadcast address command **and** c. After step 6 (final iteration), the DUT does not issue a broadcast address command

4, 6	**FAIL**	a. T_1 is not in the range of 8 – 10.5 ms (t_{RSTL}) **or** b. After step 6 (first and second iterations), the DUT does not issue a broadcast address command **or** c. After step 6 (final iteration), the DUT issues a broadcast address command

Possible Problems:

Test PSE3.2 – Classification Time

Purpose: To verify that a PSE completes classification within the specified timing

References:

[1] IEEE Std. 802.3-2022, Subclause 104.4.6
[2] IEEE Std. 802.3-2022, Table 104-7
[3] IEEE Std. 802.3-2022, PICS PSE10, PSE11

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Power Supply
- Oscilloscope

Last Modification: January, 2024

Discussion: A PSE with SCCP enabled shall complete classification after detection and prior to application of full operating voltage at the PI in a time less than T_{Class} as specified in Table 104–7. If classification is not completed before the T_{Class} timer expires, a new detection cycle shall be completed before any subsequent application of full operating voltage, the PSE shall transition to the RESTART state.

Test Setup: Figure 1

Test Procedure:

1. Present a valid wakeup current and detection signature to the DUT
2. Wait until the DUT issues a SCCP reset pulse and respond with a valid PD presence pulse. Mark the moment the PSE initiates the first reset pulse as $t = t_0$
3. Capture and decode the next 16 write timeslots issued by the DUT.
4. Use the PoDL PD simulator to respond to the next 24 timeslots with the appropriate function format **Note –** Each timeslot begins when V_{PSE} falls below 2V (V_{TL}) and ends when the subsequent timeslot begins
5. Repeat the test with step 4 modified so that the PoDL PD simulator does not respond to the DUT SCCP request

Observable Results:

Step	Status	Description
4, 5	**PASS**	a. The PSE completes classification after detection and prior to application of full operating voltage at the PI in a time less than T_{Class} (366 ms for class 0 – 9 devices, 1300 ms for class 10 – 15 devices) **and** b. The PSE does not complete classification within T_{Class} (366 ms for class 0 – 9 devices, 1300 ms for class 10 – 15 devices) and subsequently returns to the RESTART state
4, 5	**FAIL**	a. The PSE completes classification prior to detection or after application of full operating voltage at the PI **or** b. The PSE does not complete classification within T_{Class} (366 ms for class 0 – 9 devices, 1300 ms for class 10 – 15 devices) and does not return to the RESTART state

Possible Problems:

Test PSE3.3 – PSE Write Timeslot

Purpose: To verify that a PSE properly issues write timeslots

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.1.2
[2] IEEE Std. 802.3-2022, Figure 104-11
[3] IEEE Std. 802.3dd, Table 104-12
[4] IEEE Std. 802.3-2022, PICS SCCP6, SCCP7, SCCP8, SCCP9, SCCP10, SCCP21, SCCP24

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Power Supply
- Oscilloscope

Last Modification: January, 2024

Discussion: There are two types of write time slots: Write 1 and Write 0 time slots. The PSE shall use a Write 1 time slot to transmit a logic 1 to the PD and a Write 0 time slot to transmit a logic 0 to the PD. All write time slots shall be $t_{WRITESLOT}$ in duration. The PSE shall initiate both types of write time slots by pulling V_{PSE} low. To generate a Write 1 time slot, after pulling V_{PSE} low, the PSE shall pull up V_{PSE} within the range of t_{W1L}. To generate a Write 0 time slot, after pulling the V_{PSE} low, the PSE shall pull up V_{PSE} within the range of t_{W0L}. All data and commands shall be transmitted least significant bit first using SCCP.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid wakeup current and detection signature to the DUT
2. Wait until the DUT issues a SCCP reset pulse and respond with a valid PD presence pulse
3. Capture and decode the next 16 write timeslots issued by the DUT.
   Note – Each timeslot begins when V_{PSE} falls below 2V (V_{TL}) and ends when the subsequent timeslot begins

Observable Results:

Step	Status	Description
3	**PASS**	a. After SCCP initialization, the DUT issues a broadcast address command (0xCC) **and** b. Data is transmitted least significant bit first **and** c. All timeslots are a maximum of 3.85 ms in duration **and** All write timeslots follow the timing requirements for either a write 0 or write 1 timeslot: d. After initiation of write 1 timeslots, V_{PSE} is low for 0.09 to 0.64 ms (t_{W1L}) before V_{PSE} rises to 3V (V_{TH}) **and** e. After initiation of write 0 timeslots, V_{PSE} is low for 1.8 to 2.6 ms (t_{W0L}) before V_{PSE} rises to 3V (V_{TH})
3	**FAIL**	a. After SCCP initialization, the DUT does not issue a broadcast address command (0xCC) **or**

		b. Data is transmitted most significant bit first **or** c. At least one timeslot is greater than 2.78 ms in duration **or** At least one timeslot does not follow the timing requirements for either a write 0 or write 1 timeslot: d. After initiation of write 1 timeslots, V_{PSE} is not low for 0.09 to 0.64 ms (t_{W1L}) before V_{PSE} rises to 3V (V_{TH}) **or** e. After initiation of write 0 timeslots, V_{PSE} is not low for 1.8 to 2.6 ms (t_{W0L}) before V_{PSE} rises to 3V (V_{TH})

Possible Problems:

Test PSE3.4 – PSE Read Timeslot

Purpose: To verify that a PSE properly initiates and reads data from a connected PD during read timeslots

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.1.3
[2] IEEE Std. 802.3-2022, Figure 104-12
[3] IEEE Std. 802.3dd, Table 104-12
[4] IEEE Std. 802.3-2022, PICS SCCP12, SCCP13, SCCP14, SCCP19

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Power Supply
- Oscilloscope

Last Modification: January, 2024

Discussion: The PD can only transmit data to the PSE when the PSE issues read time slots. Therefore, the PSE shall generate read time slots immediately after issuing a function command, which requires data from the PD so that the PD can provide the requested data. All read time slots shall be $t_{READSLOT}$ in duration. The PSE shall initiate a read time slot by pulling V_{PSE} low and then pulling-up V_{PSE} within t_{W1L}. After the PSE initiates the read time slot, the PD shall begin transmitting a 1 or 0 at its PI. The PD shall transmit a 1 by leaving V_{PD} high and transmit a 0 by pulling V_{PD} low. When transmitting a 0, the PD shall hold V_{PD} low and then release V_{PD} within t_{R0L}. V_{PSE} and V_{PD} will be pulled back to the high idle state by the PSE's pull-up current. Output data from the PD is valid for t_{MSR} after the falling edge that initiated the read time slot. Therefore, the PSE shall release V_{PSE} and then sample the subsequent voltage within t_{MSR} from the start of the read time slot SCCP electrical requirements.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid wakeup current and detection signature to the DUT
2. Wait until the DUT issues a SCCP reset pulse and respond with a valid PD presence pulse
3. Capture and decode the next 16 write timeslots issued by the DUT.
4. Use the PoDL PD simulator to respond to the next 24 read timeslots with the appropriate function format. **Note –** Each timeslot begins when V_{PSE} falls below 2V (V_{TL}) and ends when the subsequent timeslot begins
5. Repeat the test (steps 1 – 4) with step 4 modified so that the PoDL PD simulator pulls the SCCP line low at 0.88 ms ($t_{MSR(MIN)}$ − 0.2 ms) after initiation of all read 0 timeslots except for those part of the CRC8
6. Repeat the test (steps 1 – 4) with step 4 modified so that the PoDL PD simulator pulls the SCCP line low at 1.32 ms ($t_{MSR(MAX)}$ + 0.2 ms) after initiation of all read 1 timeslots except for those part of the CRC8

Observable Results:

Step	Status	Description
4	**PASS**	a. V_{PSE} is pulled below 2V (V_{TL}) for 0.09 to 0.64 ms (t_{W1L}) before rising above 3V (V_{TH}) at the start of all read 1 timeslots **and** b. All read timeslots are a maximum of 5 ms ($t_{READSLOT}$) in duration **and** c. After step 4, the DUT recognizes the PD simulator response as valid

4	**FAIL**	a. V_{PSE} is not pulled below 2V (V_{TL}) for 0.09 to 0.64 ms (t_{W1L}) before rising above 3V (V_{TH}) at the start of all read 1 timeslots **or** b. At least one read timeslot is greater than 5 ms ($t_{READSLOT}$) in duration **or** c. After step 4, the DUT does not recognize the PD simulator response as valid

Possible Problems: The DUT response can be variable, and for this reason, the result arbiter (requirement c) is written vaguely. This requirement is seeking to observe that the DUT samples the SCCP voltage during the t_{MSR} period.

Test PSE3.5 – SCCP Electrical Characteristics

Purpose: To verify that a PSE limits the output voltage, output current, and rise and fall times of its SCCP signaling

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.1.3
[2] IEEE Std. 802.3-2022, Table 104-12
[3] IEEE Std. 802.3dd, Table 104-12
[4] IEEE Std. 802.3-2022, PICS SCCP20

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: A PSE or PD implementing SCCP shall comply with the electrical and timing requirements in Table 104–12. All voltages are referenced to the PI.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid wakeup current and detection signature to the DUT
2. Capture the voltage and current during the SCCP reset pulse and PD presence pulse
3. Mark the moment V_{PSE} begins to decrease from V_{PUP} during the reset pulse as t_1
4. Mark the moment V_{PSE} falls below 2V (V_{TL}) during the reset pulse as t_2
5. Calculate the fall time as $t_2 - t_1$
6. Mark the moment V_{PSE} begins to rise after t_2 as t_3
7. Mark the moment V_{PSE} rises above 3V (V_{TH}) after t_3 as t_4
8. Calculate the rise time as $t_4 - t_3$

Observable Results:

Step	Status	Description
2, 5, 8	**PASS**	a. The SCCP idle voltage is in the range of 4.7V to 5V (V_{PUP}) for class 0 to 9 DUTs, or the SCCP idle voltage is in the range of 4.7V to 5.5V (V_{PUP}) for class 10 to 15 DUTs **and** b. The DUT pull up current measured during the PD presence pulse is in the range of 9 to 15 mA (I_{PUP}) **and** c. The fall time is less than or equal to 0.25 ms (t_F) **and** d. The rise time is in the range of 0.025 to 0.5 ms (t_R)
2, 5, 8	**FAIL**	a. The SCCP idle voltage is not in the range of 4.7V to 5V (V_{PUP}) for class 0 to 9 DUTs, or the SCCP idle voltage is not in the range of 4.7V to 5.5V (V_{PUP}) for class 10 to 15 DUTs **or** b. The DUT pull up current measured during the PD presence pulse is not in the range of 9 to 15 mA (I_{PUP}) **or**

		a. The fall time is greater than 0.25 ms (t_F) **or** b. The rise time is not in the range of 0.025 to 0.5 ms (t_R)

Possible Problems:

Test PSE3.6 – Cable Resistance Measurement

Purpose: To verify that a PSE supports the read_VOLT_INFO, read_POWER_INFO, write_POWER_ASSIGN, and read_POWER_ASSIGN commands if it implements Cable Resistance Measurement (CRM)

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.7.2.6, 104.7.2.7, 104.7.2.8, 104.7.2.9
[2] IEEE Std. 802.3-dd, Subclause 104.7.2.6
[3] IEEE Std. 802.3-2022, Figure 104-13
[4] IEEE Std. 802.3-2022, Tables 104-14, 104-15, 104-16, 104-17
[5] IEEE Std. 802.3-2022, PICS SCCP27, SCCP28, SCCP29, SCCP31, SCCP33, SCCP34, SCCP35, PSE38

Resource Requirements:

- UNH-IOL PoDL PD Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: A PSE that implements cable resistance measurement may calculate cable resistance (dc loop resistance of the link segment) using the voltage and current at the PSE PI during the presence pulse and the voltage at the PD PI. All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_VOLT_INFO command. PD that supports cable resistance measurement may request a power allocation between 0.1 W and $P_{Class(max)}$ via the PD Requested Power, P_{PD_req}, field of the POWER_INFO register b[11:0]. All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_INFO command. A PSE that supports cable resistance measurement shall set PD Assigned Power (P_{PD_assign}) based on PD Requested Power, P_{PD_req}, and measured cable resistance. All PSEs and PDs that support cable resistance measurement shall support the 8-bit Write_POWER_ASSIGN command. After transmitting a Write_POWER_ASSIGN command, the PSE shall transmit a 16-bit POWER_ASSIGN write payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_ASSIGN command. Maximum average available power at the PD PI is P_{PD_assign}.

Test Setup: Use a cable channel with 5.5 Ohms of DC loop resistance

Test Procedure:

1. Present a valid wakeup current and detection signature to the DUT
2. Use the PoDL PD simulator to transmit a valid PD presence pulse when the DUT initializes SCCP
3. Use the PoDL PD simulator to transmit valid responses to the scratchpad read command when prompted by the DUT
   Note – If the DUT does not support Cable Resistance Measurement, the test is concluded
4. Use the PoDL PD simulator to transmit a response of 50 mV to the volt info command when prompted by the DUT
5. When the DUT issues a power info read command, request power equal to $P_{Class\_PSE}/2$ (W)
6. Read the value of the power_assign and CRC8 fields when the DUT initiates a write_POWER_ASSIGN function
7. Use the PoDL PD simulator to transmit a valid response (confirmation) to the read power assign command
8. When the DUT proceeds to the power on state, wait 75 ms then draw a load equal to $P_{Class\_PSE}/2$ (W)

Observable Results:

Step	Status	Description
2, 3, 4, 5, 6, 7, 8	**PASS**	a. The DUT conforms to the state diagram of figure 104-13 (all of the following are true) a. The DUT performs a SCRATCHPAD_READ? Command b. If the DUT supports CRM, it performs a VOLT_INFO READ? Command c. If the DUT supports CRM, it performs a POWER_INFO READ? Command d. If the DUT supports CRM, it performs a POWER_ASSIGN WRITE? command e. If the DUT supports CRM, it performs a POWER_ASSIGN READ? command **and** b. In step 6, the DUT transmitted value of the CRC8 field is computationally accurate **and** c. In step 8, the available power at the PI is less than or equal to $P_{class\_PSE}/2$
2, 3, 4, 5, 6, 7, 8	**FAIL**	a. The DUT does not conform to the state diagram of figure 104-13 (at least one of the following is true) a. The DUT does not perform a SCRATCHPAD_READ? Command b. If the DUT supports CRM, it does not perform a VOLT_INFO READ? Command c. If the DUT supports CRM, it does not perform a POWER_INFO READ? Command d. If the DUT supports CRM, it does not perform a POWER_ASSIGN WRITE? command e. If the DUT supports CRM, it does not perform a POWER_ASSIGN READ? command **or** b. In step 6, the DUT transmitted value of the CRC8 field is not computationally accurate **or** c. In step, the available power at the PI is greater than $P_{class\_PSE}/2$

Possible Problems:

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.