Power over Data Line

IEEE Clause 104
Powered Device
Conformance Test Plan
Version 2.4

Technical Document

Last Updated: September, 2023

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The University of New Hampshire
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MODIFICATION RECORD

June 2, 2017 Version 1.0
Wyman Smith: Preliminary release. First draft.

June, 2022 Version 2.0
Marc Tausanovitch: Updated per IEEE 802.3cg and current methodologies

September, 2022 Version 2.1
Marc Tausanovitch: Updated per IEEE 802.3dd and added tests 104.2.6, 104.2.8, 104.2.9

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Marc Tausanovitch: Updated per internal review

April, 2023 Version 2.3
Marc Tausanovitch: Updated per external review and 802.3-2022 and 802.3dd changes

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Marc Tausanovitch: Added group 3 (SCCP) tests

The University of New Hampshire
InterOperability Laboratory

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Craig Chabot	UNH InterOperability Laboratory
Wyman Smith	UNH InterOperability Laboratory
Tim Ryan	UNH InterOperability Laboratory
Marc Tausanovitch	UNH InterOperability Laboratory
Demetrios Galatis	UNH InterOperability Laboratory

INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the functionality of Power over Data Line (PoDL) Powered Devices (PD).

These tests are designed to determine if a product conforms to specifications defined in Clause 104 of the IEEE Std. 802.3bu. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many Power over Data Line environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration are not included here, and are generally covered in the test procedure section, below.

Test Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

TEST SETUP

Figure 1 is the general test setup used by the InterOperability Lab to perform the tests described in this test plan.

The DUT (PD) is connected to the UNH-IOL Powered Sourcing Equipment Simulator (PSE Simulator) which contains its own circuitry to perform detection, classification, and power on. A power supply is supplemented in the setup to allow for power to be delivered through the PSE Simulator. The PSE Simulator provides the tester various on-board breakouts for various measurement instruments. This allows data to be observed from the DUT during the tests included inside this test plan.

Each block is connected to the test station. This is either through an Ethernet Link via a Switch and Router or a USB connection. The DUT can also be connected to the test station if an interface is provided by the vendor. This connection is necessary if the vendor would like both SCCP and detection to be tested. The ability to enable or disable SCCP through this connection must also be available to the tester if both SCCP and detection is needed to be tested.

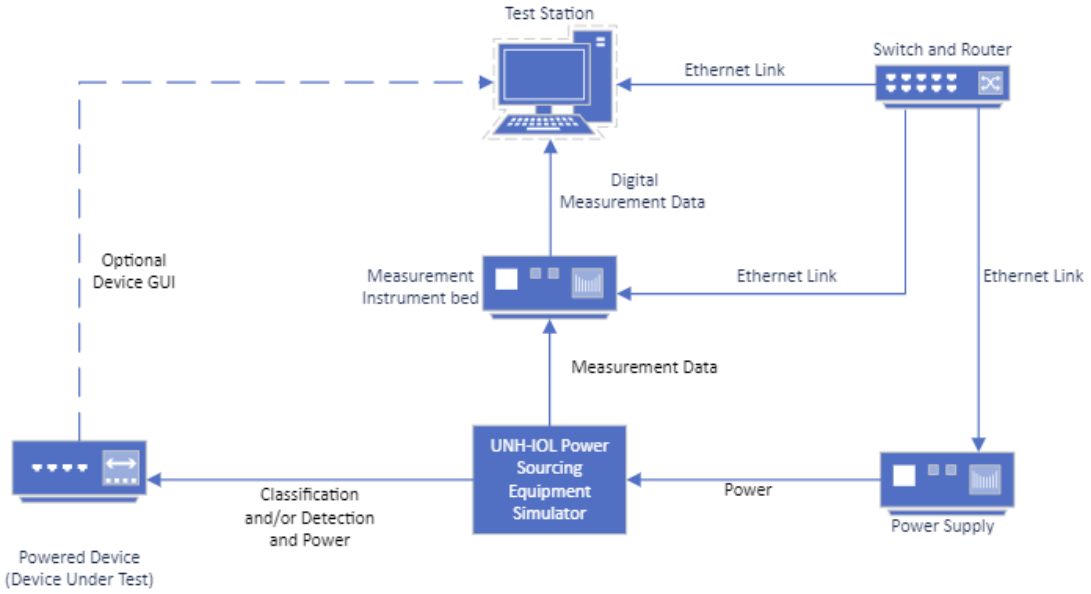

Figure 1: General Test Setup

Figure 2 is the setup used for PD2.7, which is responsible for testing the input capacitance of the DUT. This setup only requires the DUT and an LCR.

Figure 2: Test Setup for PD2.7

GROUP 1: PD Identification Characteristics

Overview:

The tests defined in this section verify the detection and classification characteristics of a Power over Data Line (PoDL) Powered Device (PD), as defined in Clause 104 of the IEEE Std. 802.3-2022 and IEEE Std. 802.3dd.

Test PD1.1– PD Pinout

Purpose: To verify that the PD conforms to the appropriate connecter pin assignment for its power class

References:

[1] IEEE Std. 802.3-2022, Subclause 104.5.2
[2] IEEE Std. 802.3-2022, Table 104-8
[3] IEEE Std. 802.3-2022, PICS PD1

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply

Last Modification: April, 2023

Discussion: Class 0 to class 9 PDs shall be able to operate per the Mode A column in Table 104–8. Class 10 to class 15 PDs shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the Mode A column and the Mode B column in Table 104–8.

Table 104–8—PD pinout

Contact	Mode A	Mode B
1	PI+	PI–
2	PI–	PI+

Test Setup: **Figure 1**

Test Procedure:

1. Connect the PSE simulator to the DUT PI using the Mode A connection
2. Apply a detection and power on waveform to the DUT
3. Repeat steps 1 and 2 using the Mode B connection

Observable Results:

Step	Status	Description
2	**PASS**	a. The DUT is a class 0 – 9 PD and only powers when using the Mode A connection **or** b. The DUT is a class Class 10 – 15 PD and powers when using Mode A and Mode B connections
2	**FAIL**	a. The DUT is a class 0 – 9 PD and powers when using the Mode A and Mode B connections **or** b. The DUT is a class 10 – 15 PD and does not power in both the Mode A and Mode B connections

Possible Problems:

Test PD1.2 – Class Power Requirements

Purpose: To ensure that the PD complies with the voltage, current, and power requirements associated with its class.

References:

[1] IEEE Std. 802.3-2022 Subclause 104.3
[2] IEEE Std. 802.3-2022, Table 104-1, 104-2
[3] IEEE Std. 802.3-2022, PICS PD2

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- DC Power Supply
- Digital Multimeter

Last Modification: April, 2023

Discussion: A PD must comply with the relevant power limits stated in table 104-1 and table 104-2. Class designations range from 0 - 15 and indicate the voltage limits, current limits, and power availability for the PD under nominal operating conditions.

Table 104–1—Class power requirements matrix for PSE, PI, and PD

	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
$V_{PSE(max)}$ (V)[a]	18	18	18	18	36	36	36	36	60	60
$V_{PSE\_OC(min)}$ (V)[b]	6	6	14.4	14.4	12	12	26	26	48	48
$V_{PSE(min)}$ (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48
$I_{PI(max)}$ (mA)[c]	101	227	249	471	97	339	215	461	735	1 360
$P_{Class(min)}$ (W)[d]	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3
$V_{PD(min)}$ (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7
$P_{PD(max)}$ (W)[e]	0.5	1	3	5	1	3	5	10	30	50

Table 104–2—Class power requirements matrix for PSE, PI, and PD for classes 10 through 15

Class	**10**	**11**	**12**	**13**	**14**	**15**
$V_{PSE(max)}$ (V)	30	30	30	58	58	58
$V_{PSE\_OC(min)}$ (V)	20	20	20	50	50	50
$V_{PSE(min)}$ (V)	20	20	20	50	50	50
$I_{PI(max)}$ (mA)	92	240	632	231	600	1579
$P_{class(min)}$ (W)	1.85	4.8	12.63	11.54	30	79
$V_{PD(min)}$ (V)	14	14	14	35	35	35
$P_{PD(max)}$ (W)	1.23	3.2	8.4	7.7	20	52

Test Setup: Figure 1

Test Procedure:

1. Apply a detection and power on waveform to the DUT
2. Configure the power supply so that $V_{PSE(max)}$ for the DUT power class is available at the DUT PI and record the applied voltage as V_{PD}
3. Continuously measure the current sourced to the DUT and record the measurement as I_{PD}
4. Measure the average power sourced to the DUT for 3 seconds and record the measurement as P_{PD}
   Note - The average power is calculated using a sliding window with a width of 1 second, according to the equation below
   $$P_{PD} = \int_{T_0}^{T_0 + 1\,s} V_{PD}(t) * I_{PD}(t)\, dt$$
5. Repeat steps 3 - 4 with $V_{PSE(min)}$ for the DUT power class is available at the DUT PI

Observable Results:

Step	Status	Description
4, 5	**PASS**	a. All measurements of I_{PD} are less than or equal to $I_{PI(max)}$ for the DUT power class **and** b. All measurements of P_{PD} are less than or equal to $P_{PD(max)}$ for the DUT power class
4, 5	**FAIL**	a. At least one measurement of I_{PD} is greater than $I_{PI(max)}$ for the DUT power class **or** b. At least one measurement of P_{PD} is greater than $P_{PD(max)}$ for the DUT power class

Possible Problems:

Test PD1.3 – Detection Signature

Purpose: To determine if the PD implements detection and to verify that it does so correctly.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.5.4
[2] IEEE Std. 802.3-2022, Subclause 104.5.5
[3] IEEE Std. 802.3-dd, Table 104-9
[4] IEEE Std. 802.3-2022, Table 104-10
[5] IEEE Std. 802.3-2022, PICS PD4, PD5, PD6, PD7, PD8, PD9

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- DC Power Supply
- Digital Multimeter

Last Modification: April, 2023

Discussion: Class 0 and Class 1 PDs, or PDs that do not implement classification shall enable a valid detection signature when VPD is less than V_{sig_enable} min and may enable a valid detection signature when VPD is less than V_{sig_enable} max. A PD that presents an invalid detection signature greater than V_{bad_hi} max as specified in Table 104–10 shall implement classification as specified in 104.7.

Table 104–9—Valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Min	Max	Unit
V_{good}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	4.05	4.55	V
$I_{signature\_limit}$	V_{PD} < $V_{sig\_disable}$ max		24	mA
$V_{sig\_disable}$, Classes 0 to 9	V_{PD} rising	4.6	5.75	V
$V_{sig\_disable}$, Classes 10 to 15	V_{PD} rising	6.0	7.5	V
V_{sig_enable}	V_{PD} falling	3.6	4.3	V

Table 104–10—Non-valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Min	Max	Unit
V_{bad_hi}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	5.15	—	V
V_{bad_lo}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	—	3.7	V

-

Test Setup: Figure 1

Test Procedure:

1. Configure the power supply so that 3.6 V ($V_{sig\_enable(min)}$) is available at the DUT PI
2. Continuously measure the voltage at the DUT PI and define this measurement as V_{PD}
3. Apply a detection probe current of 7 mA to the DUT with an open circuit voltage of 5.5 V $V_{OC(max)}$
4. Increase the detection probe current by 100 µA and wait at least 1 ms (T_{sig_hold})
5. Repeat step 4 until a detection probe current of 17 mA is sourced to the DUT
6. Configure the power supply so that the appropriate level of $V_{sig\_disable}$ max is available at the DUT PI
7. Measure the current sourced to the DUT.

Observable Results:

Step	Status	Description
5, 7	**PASS**	a. In step 5, all measurements of V_{PD} are in the range of 4.05 - 4.55 V (V_{good}) **and** b. In step 7, the current sourced to the DUT is not in the range of 7 - 17 mA ($I_{signature\_limit}$) **or** a. In step 5, the PD presents a detection signature greater than 5.15 V (V_{bad_hi}) and implements classification
5, 7	**FAIL**	a. In step 5, at least one measurement of V_{PD} is outside the range of 4.05 - 4.55 V (V_{good}) (applicable only if pass condition c. is not met) **or** b. In step 7, the current sourced to the DUT is in the range of 7 - 17 mA ($I_{signature\_limit}$)

Possible Problems:

- If the voltage at the PI of the DUT enters the $V_{sig\_disable}$ range at any time or the DUT disables present_det_sig (IEEE Std. 802.3-2022, Subclause 104.5.4.3) for another reason, it will not present a valid detection signature

GROUP 2: PD Power Characteristics

Overview:

The tests defined in this section verify the power electrical characteristics of a Power over Data Line (PoDL) Powered Device (PD), as defined in Clause 104 of the IEEE Std. 802.3-2022 and IEEE Std. 802.3dd.

Test PD2.1– Current Derivatives

Purpose: To verify that the PD limits its load current slew to the appropriate value

References:

[1] IEEE Std. 802.3-2022, Subclause 104.5.7
[2] IEEE Std. 802.3-2022, Tables 104-1, 104-2, 104-11
[3] IEEE Std. 802.3-2022, PICS PD10

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Digital Multimeter

Last Modification: April, 2023

Discussion: When the PD is powered with a voltage in the range of V_{PD}, it shall limit its input current slew to 1 A/ms (type A and C PDs), 10 A/ms (type B PDs), or 0.1 A/ms (type E PDs).

Table 104–11—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input current dI/dt		A/ms	—	1	A, C	See 104.5.7.4
				—	10	B	
				—	0.1	E	
2	Input voltage dV/dt		V/ms	—	20	A, C	
				—	200	B	
				—	2	E	

Test Setup: **Figure 1**

Test Procedure:

1. Apply a detection and power on waveform to the DUT
2. Configure the power supply so that $V_{PD(min)}$ for the DUT power class is available at the DUT PI
3. Measure the current continuously for 2 seconds and define this as $I_{PD}(t)$
4. Calculate the current derivative, $dI_{PD}(t)/dt$
5. Repeat the test (steps 1 – 4) with step 2 modified so that $V_{PSE(max)}$ for the DUT power class is available at the DUT PI

Observable Results:

Step	Status	Description
4	**PASS**	a. All measurements of $dI_{PD}(t)/dt$ are less than or equal to the respective limit for the DUT type
4	**FAIL**	a. At least one measurement of $dI_{PD}(t)/dt$ is greater than the respective limit for the DUT type

Possible Problems:

Test PD2.2 – Discharge Characteristics

Purpose: To ensure that the PD discharges safely when disconnected from a PSE.

References:

[1] IEEE Std. 802.3dd, Subclause 104.5.7.1
[2] IEEE Std. 802.3-2022, Tables 104-7, 104-12
[3] IEEE Std. 802.3-2022, PICS PD10
[4] IEEE Std. 802.3dd, PICS PD11

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- DC Power Supply
- Digital Oscilloscope

Last Modification: April, 2023

Discussion: When there is no PSE or the PSE is not sourcing power, the PD might present a voltage on the (unpowered) pair. This can cause a current to flow from the PD. In order to constrain this current, the voltage across a 5 k resistor connected across the PD PI shall not exceed V_{PUP} as defined in Table 104–12, after a delay of T_{OFF} max (see Table 104-7) after the removal of PSE power from the PD PI.

Table 104–12—SCCP electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	PSE/PD Type	Additional information
1	PSE Pull-up Voltage (Classes 0 to 9)	V_{PUP}	V	$V_{good\_PSE\ max}$	5	All	See Table 104–6
	PSE Pull-up Voltage (Classes 10 to 15)				5.5		
2	PSE Pull-up Current	I_{PUP}	mA	9	16	All	

Test Setup: **Figure 1**

Test Procedure:

1. Apply a detection and power on waveform to the DUT
2. Configure the power supply so that $V_{PSE(max)}$ for the DUT power class is available at the DUT PI
3. Place a 5 kΩ resistor across the DUT PI
4. Continuously measure the voltage at the DUT PI and define this measurement as V_{PD}
5. Disconnect the PSE Simulator from the DUT and mark this time as t = 0
6. Define T_0 as the moment t = 500 ms (T_{OFF} max)

Observable Results:

Step	Status	Description
6	**PASS**	a. V_{PD} does not exceed V_{PUP} max after T_0
6	**FAIL**	a. V_{PD} exceeds V_{PUP} max after T_0

Possible Problems:

Test PD2.3– Input Voltage

Purpose: To verify that the PD turns on and off at the proper voltage levels for its class and with the correct timing.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.5.7.2
[2] IEEE Std. 802.3-2022, Subclause 104.2
[3] IEEE Std. 802.3-2022, Tables 104-1, 104-11
[4] IEEE Std. 802.3-2022, PICS PD12, PD13, PD14, PD15

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Digital Oscilloscope
- Digital Multimeter

Last Modification: April, 2023

Discussion: The PD shall turn on at a voltage less than or equal to V_{On} max and with a delay greater than T_{power_dly} min. After the PD turns on, the PD shall stay on over the range from V_{PD} min to V_{PSE} max. The PD shall turn off at a voltage in the range of V_{PD} min to V_{Off} min. Table 104–1 defines the values for V_{PD} min and V_{PSE} max. Table 104–11 defines the values for V_{On}, T_{power_dly}, and V_{Off}.

The PD shall turn on or off without startup oscillation and within the first trial when a voltage in the range of V_{PSE} (as defined in Table 104–1) is applied with a series resistance within the range of valid dc loop resistance (see 104.2).

Test Setup: **Figure 1**

Test Procedure:

1. Continuously measure the current sourced to the DUT
2. Increase the voltage at the DUT PI from 0 to V_{On} for the DUT power class with a slew rate of +1 V/s
3. Remove power from the DUT
4. Increase the voltage applied to the DUT from 0 V to V_{On} using the maximum possible slew rate
5. Increase the voltage applied to the DUT PI to $V_{PSE(max)}$ for the DUT power class
6. Decrease the voltage applied to the DUT PI to $V_{PD(min)}$ for the DUT power class
7. Reduce the voltage applied to the DUT PI to V_{Off} using a slew rate of -1 V/s
8. Repeat the test (steps 1 – 4) using cabling with a DC loop resistance specified by the table below

Power Class	**DC Loop Resistance**	**Units**
0, 1	5.5 ± 5%	Ohms
2, 3, 4, 5, 6, 7, 8, 9	6 ± 5%	
10, 13	60 ± 5%	
11, 14	22 ± 5%	
12, 15	9 ± 5%	

Observable Results:

Step	Status	Description
2, 4, 6, 7	**PASS**	a. In step 2, the DUT powers on at a voltage less than or equal to V_{On} **and** b. In step 2, the DUT powers on without startup oscillations **and** c. In step 4, the DUT waits at least T_{power_dly} before powering up **and** d. In step 6, the DUT remains powered **and** e. In step 7, the DUT powers off at a voltage in the range of V_{Off} to $V_{PD(min)}$
2, 4, 6, 7	**FAIL**	a. In step 2, the DUT does not power on **or** b. In step 2, the DUT powers on with startup oscillations **or** c. In step 4, the DUT does not wait at least T_{power_dly} before powering up **or** d. In step 6, the DUT powers off **or** e. In step 7, the DUT does not power off at a voltage in the range of V_{Off} to $V_{PD(min)}$

Possible Problems:

- The power on state of the device may not be obvious from the current draw. An external indicator such as an LED could be used to manually determine when the DUT powers on.

Test PD2.4 – Sleep State

Purpose: To verify that the PD enters and exits the sleep state correctly and that the PD does not exhibit any error while in the sleep state.

References:

[4] IEEE Std. 802.3-2022, Subclause 104.5.7.2
[5] IEEE Std. 802.3-2022, Subclause 104.5.7.3
[6] IEEE Std. 802.3-2022, Table 104-11
[7] IEEE Std. 802.3-2022, PICS PD16, PD18
[8] IEEE Std. 802.3dd, PICS PD17

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Digital Multimeter

Last Modification: April, 2023

Discussion: When the input voltage to a PD is less than V_{sig_enable}, the PD should operate in the sleep state. While in this state, it must limit its current draw to be less than 0.1 mA (I_{Sleep_PD}). A PD that requires detection and application of power shall draw current in the range of I_{Wakeup_PD} for at least T_{Wakeup_PD} when V_{PD} is within the range of V_{Sleep_PD} as specified in Table 104–11

Test Setup: **Figure 1**

Test Procedure:

1. Apply a detection and power on waveform to the DUT
2. Reduce the DUT input voltage to 3.575 V ($V_{Sleep\_PD(max)}$) to force the DUT into the sleep mode
3. Continuously measure the current draw of the DUT in the sleep state for at least 2 seconds
4. Cause the DUT to request to wake up and capture the current waveform
5. Repeat the test (steps 1 - 4) with step 2 modified so that 3.1 V ($V_{Sleep\_PD(min)}$) is applied to the DUT

Observable Results:

Step	Status	Description
3, 4	**PASS**	a. In step 3, the DUT does not draw more than 0.1 mA **and** b. In step 4, the DUT draws between 1.3 mA - 1.8 mA for at least 0.2 ms
3, 5	**FAIL**	b. In step 3, the DUT draws more than 0.1 mA **or** c. In step 4, the DUT does not draw between 1.3 mA - 1.8 mA for at least 0.2 ms

Possible Problems:

- It may not be possible to force the PD to remain in the sleep state, as it may immediately request wakeup. Likewise, it may not be possible to force the PD to initiate wake up if it is in the sleep state

Test PD2.5 – Input Current

Purpose: To ensure that a PD adheres to the correct current limits between the detection and power on states.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.5.7.3
[2] IEEE Std. 802.3-2022, Table 104-11
[3] IEEE Std. 802.3-2022, PICS PD19

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Digital Multimeter

Last Modification: September, 2023

Discussion: A PD shall draw less than 5 mA (I_{PD_pwr1} max) for constant PD input voltage between $V_{sig\_disable}$ max and V_{On} min not including current due to inrush

Test Setup: **Figure 1**

Test Procedure:

1. Configure the power supply so that 5.75 V is available at the DUT PI
2. Increase the voltage applied to the DUT by 0.25 V and wait at least T_{power_dly}
3. Measure the current drawn by the DUT
4. Repeat steps 2 - 4 until V_{On} min is available at the DUT PI

Observable Results:

Step	Status	Description
3	**PASS**	a. The DUT current draw does not exceed 5 mA
3	**FAIL**	a. The DUT current draw exceeds 5 mA

Possible Problems:

- V_{On} min is referenced in subclause 104.5.7.3 but its value is not defined in clause 104. Pending further noticed, the value of V_{On} min is assumed to be equal to V_{PD} min which is defined for each possible DUT class type

Test PD2.6 – Ripple and Transients

Purpose: To ensure data integrity is maintained by verifying the PD meets voltage and current ripple and transient limits.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.5.7.4
[2] IEEE Std. 802.3-2022, Tables 104-1, 104-11
[3] IEEE Std. 802.3-2022, Figure 104-9
[4] IEEE Std. 802.3-2022, Equations 104-1, 104-2, 104-3
[5] IEEE Std. 802.3-2022, PICS PD20, PD21, PD22, PD23, PD24, PD25

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- DC Power Supply
- DC Programmable Load
- Digital Oscilloscope

Last Modification: April, 2023

Discussion: A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI. The input impedance, Zin(f), and transfer function, H1(f), of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PD as specified by Table 104–11 item (3a), f1 = 31.8 kHz ± 1%. When measuring the ripple voltage for a Type B or Type F PD as specified by Table 104–11 item (3a), f1 = 318 kHz ± 1%. When measuring the ripple voltage for a Type E PD as specified by Table 104–11 item (3a), f1 = 3.18 kHz ± 1%.

When measuring the ripple voltages for a Type A or Type C PD as specified by Table 104–11 item (3b), the voltage observed at the MDI/PI with the differential probe where f1 = 31.8 kHz ± 1% shall be post-processed with transfer function H2(f) specified in Equation (104–3) where f2 = 1 MHz ± 1%. When measuring the ripple voltages for a Type B or Type F PD as specified by Table 104–11 item (3b), the voltage observed at the MDI/PI with the differential probe where f1 = 318 kHz ± 1% shall be post-processed with transfer function H2(f) specified in Equation (104–3) where f2 = 10 MHz ± 1%. When measuring the ripple voltages for a Type E PD as specified by Table 104–11 item (3b), the voltage observed at the MDI/PI with the differential probe where f1 = 3.18 kHz ± 1% shall be post-processed with transfer function H2(f) specified in Equation (104–3) where f2 = 0.1 MHz ± 1%

$$Z_{in}(f) = 100\Omega \pm 0.1\% \times \frac{\sqrt{f^2 + f_1^2}}{f} \quad (104\text{–}1)$$

$$H_1(f) = \frac{f}{\sqrt{f^2 + f_1^2}} \quad (104\text{–}2)$$

$$H_2(f) = \frac{f}{\sqrt{f^2 + f_2^2}} \quad (104\text{–}3)$$

Test Setup: Figure 1

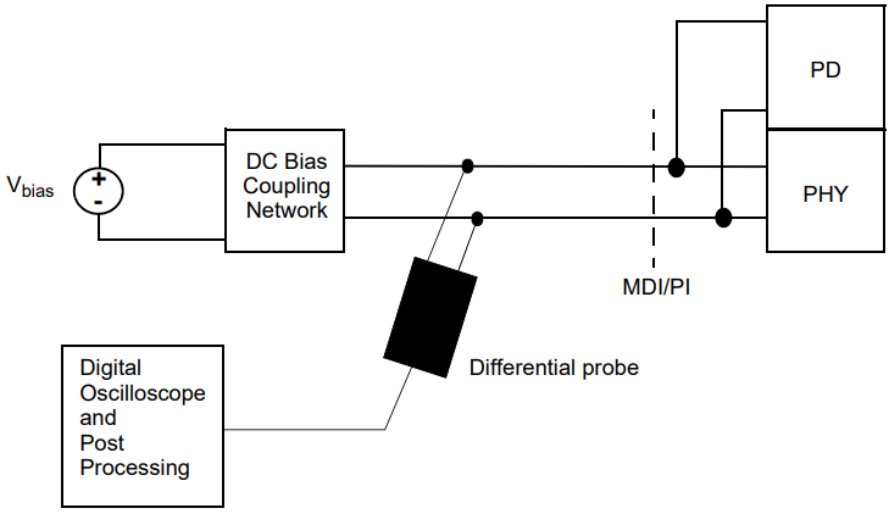

Figure 104–9—PD ripple voltage test fixture

Test Procedure:

1. Issue a detection and power on waveform to the DUT
2. Increase the voltage applied to the DUT to $V_{PSE(max)}$
3. Select the appropriate transfer function H1(f) for the DUT type and apply it to the probe
   Note - The transfer function represents a passive first order low-pass filter network at the probe input. Assuming a 100 Ω differential probe impedance, this corresponds to a balanced configuration of 2x 1 µF for type E devices, 2x 100 nF for type A and C devices, and 2x 10 nF for type B and F devices
4. Measure the peak to peak voltage noise at the DUT PI
5. Apply the appropriate transfer function H2(f) for the DUT type in post-processing
   Note – For type A and type C devices, f_2 = 1 MHz. For type B and F devices, f_2 = 10 MHz. For type E devices, f_2 = 0.1 MHz
6. Repeat the test (steps 1 - 5) with step 2 modified so that $V_{PD(min)}$ is available at the DUT PI

Observable Results:

Step	Status	Description
4, 5	**PASS**	a. All measurements in step 4 are less than or equal to 0.1 V_{PP} **and** b. All measurements in step 5 are less than or equal to 0.01 V_{PP}
4, 5	**FAIL**	a. At least one measurement in step 4 is greater than 0.1 V_{PP} **or** b. At least one measurement in step 5 is greater than 0.01 V_{PP}

Possible Problems:

Test PD2.7 – Input Capacitance

Purpose: To verify that a PD has a valid input capacitance for its given state of operation.

References:

[1] IEEE Std. 802.3-2022, Table 104-11
[2] IEEE Std. 802.3dd, Table 104-11
[3] IEEE Std. 802.3-2022, PICS PD10

Resource Requirements:

- Power Supply
- LCR Meter

Last Modification: April, 2023

Discussion: Type, A, B, C, and D PDs must exhibit less than 0.2 µF input capacitance during the DO_CLASSIFICATION state. Type E PDs must exhibit less than 0.8 µF input capacitance during the DO_CLASSIFICATION state. Class 4 PDs must limit C_{IN} to 5 µF during the DO_DETECTION, MDI_POWER1, and MDI_POWER_DELAY states. Classes 1 - 3 and 5 - 9 must limit C_{IN} to 10 µF during these states.

Test Setup: **Figure 2**

1. Use the LCR to perform a capacitance measurement using a bias current in the range of 9 mA - 16 mA (I_{valid}) and a test voltage of 0.05 V_{RMS} at 1 kHz and define this measurement as C_{IN}

Observable Results:

Step	Status	Description
1	**PASS**	A. For class 4 devices, C_{IN} is less than or equal to 5 µF **or** B. For class 1 - 3 and 5 - 9, C_{IN} is less than or equal to 10 µF
1	**FAIL**	C. For class 4 devices, C_{IN} is greater than 5 µF **or** D. For class 1 - 3 and 5 - 9, C_{IN} is greater than 10 µF

Possible Problems:

- The output capacitance may be difficult to reliably measure during the detection state
- Depending on how the DUT was designed, it may not be possible to force the LCR test voltage to the DUT PI while sourcing a valid detection current

Test PD2.8 – Maintain Full Voltage Signature

Purpose: To verify that a PD presents a valid maintain full voltage signature while under nominal operation.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.5.8
[2] IEEE Std. 802.3-2022, Table 104-11
[3] IEEE Std. 802.3-2022, PICS PD27, PD28, PD29

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Digital Multimeter

Last Modification: September, 2022

Discussion: For a PD to remain fully powered by the PSE, it must present a valid maintain full voltage signature (MFVS). The MFVS consists of a current draw of at least 11 mA (I_{hold_PD}) for a minimum duration of 10 ms (T_{MFVS_PD}). This can be followed by an optional dropout for no longer than 300 ms (T_{MFVDO} min).

Test Setup: **Figure 1**

Test Procedure:

1. Power on the DUT and reduce the input voltage to $V_{PD(min)}$.
2. Capture the current waveform with a window of at least 2 seconds and define it as I_{PD}.
3. Repeat step 2 with an input voltage of $V_{PSE(max)}$.

Observable Results:

Step	Status	Description
2	**PASS**	A. I_{PD} is greater than or equal to 11 mA for at least 10 ms continuously in any sliding window of 310 ms
2	**FAIL**	B. I_{PD} is not greater than 11 mA for at least 10 ms continuously in any sliding window of 310 ms

Possible Problems:

- The DUT may intentionally remove MFVS if it no longer requires operating power

Test PD2.9 – PD Isolation

Purpose: To verify that a PD maintains sufficient DC isolation between the MDI leads and ground.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.6.1
[2] IEEE Std. 802.3-2022, PICS PDEL1

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Ammeter

Last Modification: September, 2022

Discussion: In order to prevent the formation of a ground loop, a PD shall provide at least 1MΩ DC isolation between all accessible external conductors, including ground, and all MDI leads.

Test Setup: **Figure 1**

Test Procedure:

1. Apply a 5V test voltage between the device chassis ground and the PoDL+ line and measure the resulting current. Calculate the resistance.
2. Repeat Step 1 with applying the test voltage between chassis ground and PoDL- line
3. If there are any additional external conductors, repeat step 1 as necessary while applying the test voltage between chassis ground and and individual external conductor

Observable Results:

Step	Status	Description
1	**PASS**	a. The calculated isolation resistance is at least 1 MΩ DC
1	**FAIL**	b. The calculated isolation resistance is less than 1 MΩ DC

Possible Problems:

- It may be difficult to identify and validate the isolation of all external conductors, especially for devices without an obvious chassis or enclosure.

GROUP 3: PD SCCP Characteristics

Overview:

The tests defined in this section verify the Serial Communication Classification Protocol (SCCP) implementation of a Power over Data Line (PoDL) Powered Device (PD), as defined in Clause 104 of the IEEE Std. 802.3-2022 and IEEE Std. 802.3dd. SCCP is a current-sinking, open-drain protocol that relies on a PSE master device to initiate transactions and to provide the necessary pull up current. SCCP includes functions that allow a connected PD to communicate its class data and the ability to perform optional cable resistance measurements for advanced power negotiation.

The following tests apply to all PoDL PDs that implement SCCP.

Editor's Note: The set of test requirements in group 3 are only valid for Type E PDs. Conformance requirements for types A, B, C, D, and F may be added at a later date.

Test PD3.1 – SCCP Initialization

Purpose: To verify that a PD implementing SCCP properly indicates its presence when a PSE issues an SCCP reset command.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.1
[2] IEEE Std. 802.3-2022, Figure 104-10
[3] IEEE Std. 802.3dd, Table 104-12
[4] IEEE Std. 802.3-2022, PICS SCCP1, SCCP2, SCCP4, SCCP5, SCCP22

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: PDs that do not implement physical layer detection are required to perform classification via SCCP. All SCCP communication with a PD shall begin with an initialization sequence that consists of a reset pulse from the PSE followed by a presence pulse from the PD. During the initialization sequence the PSE shall transmit the reset pulse by first driving V_{PSE} low and then releasing to the pull up at t_{RSTL}. The PSE shall then go into receive mode (RX). When the PD detects the rising edge at the PD PI, it shall wait t_{PDH} and then transmit a presence pulse by pulling V_{PD} low for t_{PDL}.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse to the DUT using the PSE Simulator
2. Mark the time where the port voltage rises to 3 V (V_{TH}) after the PSE has released the reset pulse as t = 0 s
3. Mark the time where the port voltage begins to decrease after t = 0 as t_1.
4. Mark the time that the port voltage begins to increase after t_1 as t_2

Observable Results:

Step	Status	Description
3, 4	**PASS**	a. T_1 is in the range of 0.7 to 1.3 ms (T_{PDH}) **and** b. T_2 is in the range of 2.8 to 5.2 ms (T_{PDLOW}) for PDs that do not support link segment resistance measurement or T_2 is in the range of 21 to 39 ms (T_{PDLOW}) for PDs that do support link segment resistance measurement
3, 4	**FAIL**	a. T_1 is not in the range of 0.7 to 1.3 ms (T_{PDH}) or the PD does not issue a presence pulse **or** b. T_2 is not in the range of 2.8 to 5.2 ms (T_{PDLOW}) for PDs that do not support link segment resistance measurement or T_2 is not in the range of 21 to 39 ms (T_{PDLOW}) for PDs that do support link segment resistance measurement

Possible Problems:

Test PD3.2 – SCCP Signaling Rise and Fall Time

Purpose: To verify that a PD implementing SCCP conforms to the SCCP rise and fall time requirements

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.1.3
[2] IEEE Std. 802.3-2022, Figure 104-10
[3] IEEE Std. 802.3-2022, Table 104-12
[4] IEEE Std. 802.3dd, Table 104-12
[5] IEEE Std. 802.3-2022, PICS SCCP20

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: A PD implementing SCCP shall comply with the electrical and timing requirements in Table 104–12. All voltages are referenced to the PI.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse to the DUT using the PSE Simulator
2. Capture the SCCP initialization waveform
3. Mark the time the DUT first pulls the SCCP line low during the PD presence pulse as t_1
4. Mark the time when the port voltage first reaches 2 V (V_{TL}) after t_1 as t_2
5. Compute the fall time as $t_2 – t_1$
6. Mark the time the DUT first releases the SCCP line after t_2 as t_3
7. Mark the time when the port voltage first reaches 3 V (V_{TH}) after t_3 as t_4
8. Compute the fall time as $t_4 – t_3$
9. Repeat the test (steps 1 – 8) with step 1 modified so that $V_{PUP} = V_{PUP(MAX)}$, I_{PUP} = 16mA
10. Repeat the test (steps 1 – 8) with step 1 modified so that V_{PUP} = 4.7V I_{PUP} = 9mA

Observable Results:

Step	Status	Description
5, 8	**PASS**	a. The DUT fall time is less than 0.25 ms (t_F) **and** b. The DUT rise time is in the range of 0.025 to 0.5 ms (t_R)
5, 8	**FAIL**	a. The DUT fall time is not less than 0.25 ms (t_F) **or** b. The DUT rise time is not in the range of 0.025 to 0.5 ms (t_R)

Possible Problems:

Test PD3.3 – Support Scratchpad Read

Purpose: To verify that a PD implementing SCCP supports the scratchpad read command and that it sends data least significant bit first.

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.2
[2] IEEE Std. 802.3-2022, Table 104-13
[3] IEEE Std. 802.3-2022, PICS SCCP21, SCCP23, SCCP25, SCCP26, SCC27, SCCP28

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: September, 2023

Discussion: All data and commands shall be transmitted least significant bit first using SCCP.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse, broadcast address command, and scratchpad read command to the DUT using the PSE Simulator
2. Initiate and capture 24 read timeslots
3. Decode the DUT response

Observable Results:

Step	Status	Description
3	**PASS**	a. The DUT responds to the scratchpad read command with the proper class type info field as set for in table 104-13 [3] **and** b. The DUT transmits data LSB first **and** c. The CRC8 is computationally accurate
3	**FAIL**	a. The DUT does not respond to the scratchpad read command with the proper class type info field as set for in table 104-13 [3] **and** b. The DUT transmits data MSB first **and** c. The CRC8 is not computationally accurate

Possible Problems:

Test PD3.4 – Write Timeslot Timing

Purpose: To verify that a PD implementing SCCP samples data with the correct timing when the PSE initiates a write timeslot.

References:

[1] IEEE Std. 802.3-2022, Subclauses 104.7.1.2, 104.7.2.4
[2] IEEE Std. 802.3-2022, Figure 104-11
[3] IEEE Std. 802.3-2022, Tables 104-12, 104-13
[4] IEEE Std. 802.3-2022, PICS SCCP11

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: The PSE shall use a Write 1 time slot to transmit a logic 1 to the PD and a Write 0 time slot to transmit a logic 0 to the PD. The PSE shall initiate both types of write time slots by pulling V_{PSE} low. The PD shall sample the V_{PD} within the range of t_{ssw} after the falling edge during a Write 1 or Write 0 operation.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse and broadcast address command to the DUT using the PSE Simulator
2. Use the PSE Simulator to send a scratchpad read command to the DUT.
3. When the PSE issues write 1 timeslots during step 2, configure the PSE to pull the SCCP line high at 1.45 ms ($t_{SSW(MAX)}$ + 0.02 ms) after the start of the timeslot
4. Initiate, capture, and decode 24 read timeslots
5. Repeat the test (steps 1 – 4) with step 3 modified so that the PSE pulls the SCCP line high at 0.75 ms ($t_{SSW(MIN)}$ - 0.02 ms) after initiating write0timeslots

Observable Results:

Step	Status	Description
4	**PASS**	a. The DUT does not respond with the proper class type info
4	**FAIL**	a. The DUT responds with the proper class type info

Possible Problems:

Test PD3.5 – Read Timeslot Timing

Purpose: To verify that a PD implementing SCCP transmits data with the correct timing when the PSE initiates a read timeslot

References:

[1] IEEE Std. 802.3-2022, Subclause 104.7.1.3
[2] IEEE Std. 802.3-2022, Figure 104-12
[3] IEEE Std. 802.3-2022, Table 104-12
[4] IEEE Std. 802.3-2022, PICS SCCP15, SCCP16, SCCP17, SCCP18

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: The PSE shall initiate a read time slot by pulling V_{PSE} low and then pulling-up V_{PSE} within t_{W1L}. After the PSE initiates the read time slot, the PD shall begin transmitting a 1 or 0 at its PI. The PD shall transmit a 1 by leaving V_{PD} high and transmit a 0 by pulling V_{PD} low. When transmitting a 0, the PD shall hold V_{PD} low and then release V_{PD} within t_{R0L}.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse, broadcast address command, and read scratchpad command to the DUT using the PSE Simulator
2. Initiate and capture 24 read timeslots

Observable Results:

Step	Status	Description
2	**PASS**	All timeslots conform to the timing specifications for either a write 0 or write 1 timeslot: a. During read 1 timeslots, the DUT does not pull the SCCP line low **and** b. During read 0 timeslots, the DUT pulls the SCCP line low for a duration of 1.75 to 3.25 ms (t_{R0L}) following initiation of the read timeslot
2	**FAIL**	All timeslots do not conform to the timing specifications for either a write 0 or write 1 timeslot: a. The DUT pulls the SCCP line low for a duration less than 1.75 ms ($t_{R0L(MIN)}$) or greater than 3.25 ms ($t_{R0L(MAX)}$) following initiation of the read timeslot

Possible Problems:

Test PD3.6 – Unsupported SCCP Command

Purpose: To verify that a PD implementing SCCP will respond to an invalid command with all 1's

References:

[1] IEEE Std. 802.3dd, Subclause 104.7.2
[2] IEEE Std. 802.3dd, PICS SCCP21a

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: The PD shall return all 1s in the payload and CRC8 fields for any unsupported command.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse and broadcast address command to the DUT using the PSE Simulator
2. Initiate 8 write timeslots to send 0x55 to the DUT (invalid command)
3. Initiate, capture, and decode 24 read timeslots
4. Present a valid SCCP reset pulse to the DUT using the PSE Simulator
5. Initiate 8 write timeslots to send 0x55 to the DUT (invalid address)
6. Initiate 8 write timeslots to send a valid scratchpad read command to the DUT
7. Initiate, capture, and decode 24 read timeslots

Observable Results:

Step	Status	Description
3, 7	**PASS**	a. The DUT responds with 1 during all read timeslots
3, 7	**FAIL**	a. The DUT responds with 0 during any read timeslot

Possible Problems:

Test PD3.7 – Volt Info Command

Purpose: To verify that a PD implementing SCCP with cable resistance measurement capability supports the Read_VOLT_INFO command.

References:

[1] IEEE Std. 802.3dd, Subclause 104.7.2.6
[2] IEEE Std. 802.3dd, PICS SCCP29, SCCP30

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_VOLT_INFO command. After receiving a Read_VOLT_INFO command, the PD shall respond with a 16-bit VOLT_INFO read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. The voltage measurement returned by the Read_VOLT_INFO command is an 8-bit unsigned value with each least-significant bit equal to 10 mV. The value returned may be less than the actual PD PI voltage and may be any value up to 20 mV greater than the actual voltage at the PD PI.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse, broadcast address command, and read volt info command to the DUT using the PSE Simulator. Measure the voltage applied to the DUT PI during the t_{PDH} period of the SCCP reset pulse
2. Issue, capture, and decode 24 read timeslots
3. Convert the decoded binary stream into the volt info data using the following formula:

$$Volt\ info\ (V) = 0.01V * b[7:0]$$

Observable Results:

Step	Status	Description
3, 7	**PASS**	a. Received bits [15:8] are all 0 **and** b. The receive volt info field is less than the voltage applied to the PD PI during SCCP initialization, plus 20 mV
3, 7	**FAIL**	a. Received bits [15:8] are not all 0 **and** b. The receive volt info field is greater than the voltage applied to the PD PI during SCCP initialization, plus 20 mV
	N/A	The DUT does not support cable resistance measurement

Possible Problems:

Test PD3.8 – Power Commands

Purpose: To verify that a PD implementing SCCP with cable resistance measurement capability supports the Read_POWER_INFO, write_POWER_ASSIGN, and read_POWER_ASSIGN commands.

References:

[1] IEEE Std. 802.3dd, Subclause 104.7.2.7, 104.7.2.8, 104.7.2.9
[2] IEEE Std. 802.3dd, PICS SCCP31, SCCP32, SCCP33, SCCP34, SCCP35, SCCP36

Resource Requirements:

- UNH-IOL PoDL PSE Simulator
- Power Supply
- Oscilloscope

Last Modification: August, 2023

Discussion: All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_INFO command. After receiving a Read_POWER_INFO command, the PD shall respond with a 16-bit POWER_INFO read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5.

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Write_POWER_ASSIGN command. After transmitting a Write_POWER_ASSIGN command, the PSE shall transmit a 16-bit POWER_ASSIGN write payload followed by an 8-bit CRC8 field as specified in 104.7.2.5

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_ASSIGN command. After receiving a Read_POWER_ASSIGN command, the PD shall respond with a 16-bit POWER_ASSIGN read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5.

Test Setup: **Figure 1**

Test Procedure:

1. Present a valid SCCP reset pulse, broadcast address command, and read power info command to the DUT using the PSE Simulator
2. Issue, capture, and decode 24 read timeslots
3. Convert the decoded binary stream into the power info data using the following formula:
$$Power\ info\ (W) = 0.025W * b[11:0]$$
4. Present a valid SCCP reset pulse, broadcast address command, and write power assign command to the DUT using the PSE Simulator
5. Initiate 16 write timeslots to transmit the received power info in step 3 back to the PD. Bits [15:12] are transmitted as 0. Bits [11:0] are calculated using the following formula:
$$Power\ assigned\ (W)/0.025W\ = b[11:0]$$
6. Transmit the 8-bit CRC8 field
7. Present a valid SCCP reset pulse, broadcast address command, and read power assign command to the DUT using the PSE Simulator
8. Initiate, capture, and decode 24 read timeslots

Observable Results:

Step	Status	Description
3, 8	**PASS**	a. Received bits [15:12] are all 0 for all read operations **and** b. The DUT requested power is greater than or equal to 0.1 W and less than or equal to $P_{Class(MAX)}$ **and** c. The DUT responds with the correct PSE assigned power value in step 8
3, 8	**FAIL**	a. Received bits [15:12] are not all 0 for all read operations **or** b. The DUT requested power is less than 0.1 W or greater than $P_{Class(MAX)}$ **or** c. The DUT does not respond with the correct PSE assigned power value in step 8
	N/A	The DUT does not support cable resistance measurement

Possible Problems: