UNH-IOL
IEEE 1588 Consortium

Test Plan for Ingress & Egress Port Latency Measurement

Version 1.0.0

Technical Document

NOTICE: This is a living document. All contents are subject to change.
Individual tests and/or test groups may be added/deleted/renumbered in forthcoming revisions.
General feedback and comments are welcome, please contact ptplab@iol.unh.edu.

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Modification Record

Version	Date	Editor(s)	Comments
1.0.0	2018-03-07	Bob Noseworthy	Initial Test Suite release with single port standard's based support (no test modes required).
0.0.1	2015-02-11	Bob Noseworthy	Initial Pre-release Review Test Suite

Acknowledgements

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Garrick Craft	UNH InterOperability Laboratory
Jeff Laird	UNH InterOperability Laboratory
Bob Noseworthy	UNH InterOperability Laboratory
Brandon Smith	UNH InterOperability Laboratory
Ethan Stewart	UNH InterOperability Laboratory
Xavier McNulty	UNH InterOperability Laboratory

Introduction

Test Plan Scope: To focus on the evaluation of a Port's egress and ingress latency in relation to the port's timestamping plane via direct measurement of the device under test (DUT).

The **University of New Hampshire's InterOperability Laboratory** (UNH-IOL) is a non-profit institution designed to provide third party neutral validation of networking products. This document defines the tests that will be executed by the **UNH-IOL IEEE 1588/Precision-Time-Protocol Consortium** to provide independent validation of industry member's IEEE 1588 products.

These tests are designed to determine if a product conforms to certain requirements defined in the IEEE 1588-2008 standard (hereafter referred to as the "1588"). Specifically this test plan focuses on the DUT's 1588 Port's correction for known Port Ingress and Egress delays. These latencies must be properly accounted for in a 1588 system or time error can accumlate. Such error would be a result of the asymmetry between the media and the timestamping plane.

Successful completion of all tests contained in this suite does not guarantee that the tested device will successfully operate with other 1588 products. However, when combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 1588 environments.

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-number, dot-notated naming system is used to catalog the tests (e.g., "Test 9.1.1"), where the first number always indicates the specific section of the referenced standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests in the appropriate groups without requiring the renumbering of subsequent un-related tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Test Label: The test label and title constitute the first line of the test block. The test label is the concatenation of the short test suite name, group number, and the test number within the group, separated by periods

Purpose: The Purpose is a brief statement outlining what the test attempts to achieve. It is usually phrased as a simple assertion of the feature or capability to be tested.

Device Type Pre-Requisites, & Compliance Classifier: The Device Type Pre-requisites and Compliance Classifier section notes for each part of the test what the pre-requisite conditions are for the given Device Type. The Compliance Classifier denotes whether the test part, for the identified Device Type meeting the identified pre-requisite conditions, is one of the following:

Classifier	Meaning
Mandatory	Test part is required by the referenced standards and/or specifications if the DUT matches the Device Type.
Conditional Mandatory	Test part is required by the referenced standards and/or specifications if the pre-requisite condition is true and the DUT matches the Device Type.
Optional	Test part has a pass/fail criteria, but failure does not imply the device is not compliant based on this result alone.
Informative	Test part has no pass/fail, but the observations may have value.

References: The References section specifies all reference material external to the test plan, including the specific references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g. [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the test suite document itself (e.g. ”Appendix 5.A” or ”Table 5.1.1-1”).

Resource Requirements: The Resource Requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements for abstract test gear. In some cases precise equipment requirements may be provided with examples of specific manufacturer/model information provided.

Modification History: The Modification History logs the changes for this test since its introduction.

Discussion: The Discussion is a general discussion of the test and relevant section of the specification, including any assumptions made in the design or implementation of the test as well as known limitations.

Test Setup: The setup section describes the initial configuration of the test environment. Elements of the test procedure may change the test environment as the test progresses.

Procedure: The procedure section contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with requirements to record observable results. These procedures should be the ideal test methodology, independent of specific tool limitations or restrictions.

Observable Results: This section lists the specific observable items that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable. A general note on scripting: All tests are presumed to initially be considered failing, and remain so if any single fail-condition is met for the test part in question. Only if no fail conditions are met, and the explicitly stated pass-conditions observed, will the test be deemed a pass.

If, for any reason, none of the conditions of a part of a test are met (either pass or fail) then that part of the test is considered a failure (exceptions only being for WARN or INFO conditions that are met).

A strong preference is to have any part of a test err on the side of falsely failing a device rather than falsely passing the device. Whether through automation or manual execution, tests can have only one of five outcomes:

Status	Meaning
PASS	Test part meets all PASS criteria, with no FAIL or WARN conditions met.
FAIL	Test part meets at least one FAIL criteria, or fails to meet any criteria.
N/A	Test part is Not Applicable to the device.
WARN	Test part does not meet a failing criteria, but behavior is not recommended and Warned against.
INFO	Test part has no pass/fail criteria, but the observation may have value to the device manufacturer or industry-at-large.

Possible Problems: This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

Summary of Test Pre-requisites and Compliance Classifiers

Test LTNCY.1.1 — Port Egress Latency Behavior on a 1-Step TC

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	1-Step TC	DUT must provide a mechanism to insert the egress time-stamp for a packet into the transmitted packet as a 1-Step operation. The DUT must also provide a 1PPS signal.	Informative

Test LTNCY.1.2 — Port Ingress Latency Behavior on a 1-Step TC

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	1-Step TC	DUT must provide a mechanism to insert the ingress time-stamp for a packet received by the port under test into the transmitted packet on a port not under test. The DUT must also provide a 1PPS signal.	Informative

Test LTNCY.2.1 — Port Egress Latency Behavior on a Single Active Link

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	TC,BC or OC	DUT must either (a) respond to Delay_Req Messages; or (b) respond to Pdelay_Req Messages; or (c) provide a mechanism to insert the egress time-stamp for a packet into a subsequently transmitted packet; or (d) provide a means to the test station to read the egress time-stamp. The DUT must also provide a 1PPS signal with known delay from signal appearance at the signal header, to true one second roll-over of the timestamper.	**Conditional Mandatory**

Test LTNCY.2.2 — Port Ingress Latency Behavior on a Single Active Link

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	TC,BC or OC	DUT must either (a) respond to Delay_Req Messages; or (b) respond to Pdelay_Req Messages; or (c) provide a mechanism to insert the ingress time-stamp for a packet into a subsequently transmitted packet; or (d) provide a means to the test station to read the ingress time-stamp. The DUT must also provide a 1PPS signal.	**Conditional Mandatory**

SECTION LTNCY: Port Latency Measurement

Overview:

This selection of tests verifies various requirements of IEEE 1588 Transparent Clocks defined by the IEEE 1588-2008 standard.

The functionality verified in this section is intended to be independent of any particular IEEE 1588 profile; focusing instead on standard defined behaviors of a Transparent Clock (TC), and more specifically, those aspects that would be most likely to be specific to a given silicon implementation. The tests in this section do not presume which IEEE 1588 profile or profiles the silicon may be intented to support.

Comments and questions regarding the documentation and/or implementation of these tests are welcome, and may be sent to ptplab@iol.unh.edu.

Notes:

These tests are currently targeted at Ethernet-based, full-duplex, point-to-point transports; some modifications may be required for other network transports.

Group 1: Port Latency on a 1-step Transparent Clock

Overview:

This group collects tests relating to the measurement of the latency of a Port of the DUT. These tests focus on establishing a baseline set of measurements for an active link on a Transparent Clock. Future groups of tests examine latency for other device classes as well as the potential causes for latency variation and the management ability to update latency correction fields.

Note: The tests in this group can generally be replaced with the test expectations of the group 2 tests. This test group is left in this test plan version for legacy reasons only and will likely be removed in future updates.

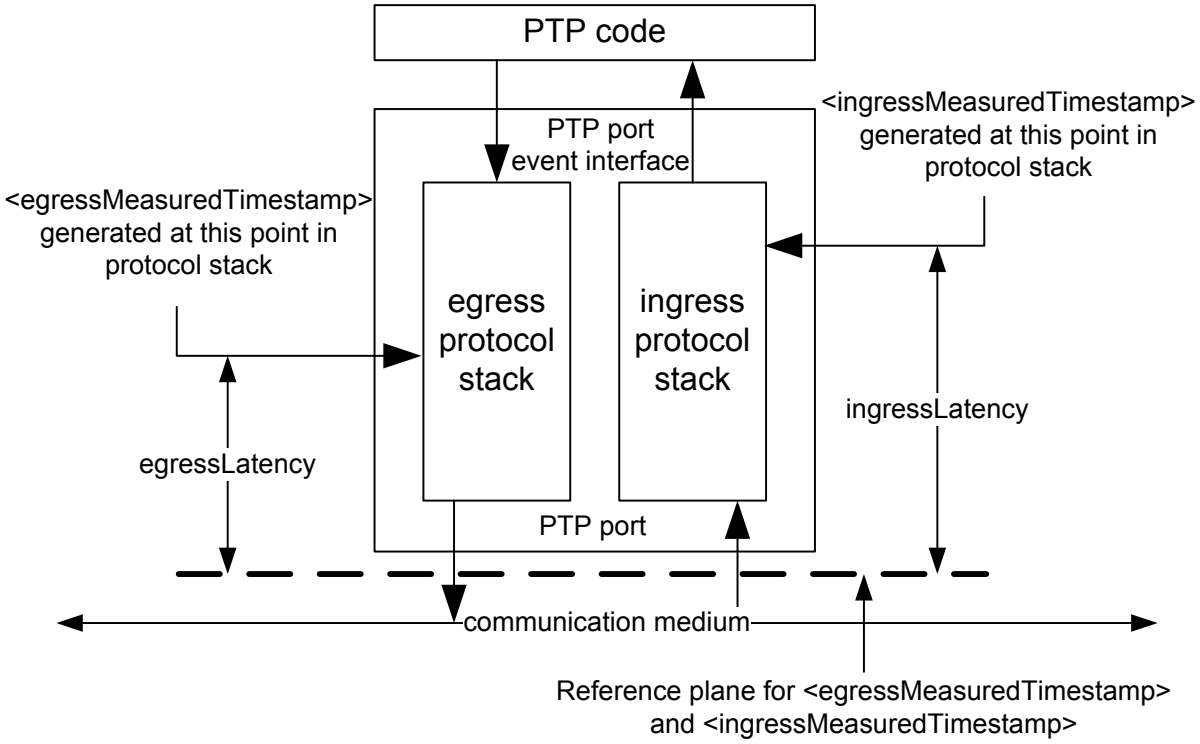

Figure G1.1: Redrawn IEEE Std 1588-2008 Figure 19: Definition of Latency Constants

Test LTNCY.1.1 — Port Egress Latency Behavior on a 1-Step TC

Purpose: To measure the Device's Port under test to determine the Port's Egress Latency relative to the MDI and DUT's time-stamper time-base.

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	1-Step TC	DUT must provide a mechanism to insert the egress time-stamp for a packet into the transmitted packet as a 1-Step operation. The DUT must also provide a 1PPS signal.	Informative

References: [1] IEEE Std 1588-2008: clause 7.3.4.1 [3] *Ibid.*: Figure 19
[2] *Ibid.*: clause 7.3.4.2

Resource Requirements: *Traffic Generator* capable of arbitrary frame generation.
Digital Sampling Oscilloscope (DSO) capable of sampling the transmitted signal sufficiently fast to decode the signal and recover the transmitted bitstream (eg: 2GSps for 100Base-TX) and also sampling the 1PPS output from the DUT in the same capture.
Line tap capable of providing the transmitted signal from the DUT to the DSO. This may be as simple as a differential probe (eg: for 100Base-TX), or a 50/50 optical splitter (eg: for 1000Base-SX), or as complex as linetap capable of providing a directionally decoupled signal from the DUT's transmitter to the DSO (eg: for 1000Base-T or 10GBase-T).

Modification History: 2015-02-11 — Initial Draft Release

Discussion: In an IEEE 1588 PTP network, for a slave to determine the time offset from the grandmaster with high precision, the slave must know the combined path delay of all link segments as well as delays through any intervening internetworking equipment. Path delay can be determined via two standard's based methodologies, end-to-end (E2E), or peer-to-peer (P2P).

In either case, the computed path delay is impacted by any uncorrected asymmetry which can occur either in the actual network link (eg: 2 fiber links where one fiber path is substantially different in length than the other) or, all too commonly, through the incorrect (or lack of) correction of the physical (PHY) layer's ingress and egress delays. These PHY delays are typically far greater on ingress than egress for any given communication technology due to receive equalization and error correction techniques.

This test measures the Device's Port under test to determine the Port's Egress Latency relative to the Media Dependent Interface (MDI) and DUT's timestamper timebase. It is presumed that the DUT will be correcting the timestamp based on a stored value of the known Egress Latency for the Port. If this stored value is accurate to correct the latency to the MDI, then the measured latency error should ideally be zero.

This test is currently designated as "Informative" as no general standard's set requirement exists for how small the error must be. In the specific case of a given application for a given profile, a limit may exist but this is not the general case.

Test Setup: Connect a channel of the DSO to the 1PPS from the DUT. Set the DSO to trigger on this channel on the rising edge of the 1PPS. Set the trigger level as low as possible while avoiding noise-induced false-triggers. Connect the *Line tap* to the transmitter output of the DUT, with the tap connected to a channel of the DSO. Connect the *Traffic Generator* to a DUT port not under test. Configure the *Traffic Generator* to send traffic that will be forwarded by the TC out the port under test and timestamped.

Test Procedure:

Part A: *1-Step TC Port Egress Latency Error.*

A:1 From the *Traffic Generator*, send traffic that the TC will 1-step timestamp on egress on the port under test. The rate should be at least one packet a second, or faster if possible provided the DUT timestamps each packet sent.

a) If the rate is not sufficiently high, the probability of the DSO capturing a packet sent in proximity to the DUT's 1PPS will be low.

A:2 Trigger the DSO to perform a single capture.

A:3 Analyze the capture to determine the start time of any transmitted packets, as well as the embedded timestamp sent by the DUT.

a) Download the capture trace and recover the bitstream.

b) Correct the DSO's timebase to that of the DUT (refer to Appendix A: Egress Latency Calculation when 1PPS available)

c) Compare the captured frame's start time to that of the DUT's Egress timestamp, correcting for any test setup delays $(1PPS_{SignalLatency} and Line Tap_{SignalLatency})$.

A:4 Repeat steps A:2 and A:3 until sufficient frames have been analyzed (>=250).

Observable Results:

Part:Step	Status	Description
A:1	INFO	The delta between the captured frame's start time vs the DUT's reported Egress timestamp is reported as the Egress timestamp error. The Max, Min, Mean, and Standard Deviation of the observed deltas is provided.

Possible Problems: None.

Test LTNCY.1.2 — Port Ingress Latency Behavior on a 1-Step TC

Purpose: To measure the Device's Port under test to determine the Port's Ingress Latency relative to the MDI and DUT's time-stamper time-base.

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	1-Step TC	DUT must provide a mechanism to insert the ingress time-stamp for a packet received by the port under test into the transmitted packet on a port not under test. The DUT must also provide a 1PPS signal.	Informative

References: [1] IEEE Std 1588-2008: clause 7.3.4.1 [3] *Ibid.*: Figure 19
[2] *Ibid.*: clause 7.3.4.2

Resource Requirements: *Traffic Generator* capable of arbitrary frame generation.
Traffic Monitor capable of capturing arbitrary frames.
Digital Sampling Oscilloscope (DSO) capable of sampling the transmitted signal sufficiently fast to decode the signal and recover the transmitted bitstream (eg: 2GSps for 100Base-TX) and also sampling the 1PPS output from the DUT in the same capture.
Line tap capable of providing the signal being transmitted to the DUT to the DSO. This may be as simple as a differential probe (eg: for 100Base-TX), or a 50/50 optical splitter (eg: for 1000Base-SX), or as complex as linetap capable of providing a directionally decoupled signal from the *Traffic Generator's* transmitter to the DSO (eg: for 1000Base-T or 10GBase-T).

Modification History: 2015-02-11 — Initial Draft Release

Discussion: In an IEEE 1588 PTP network, for a slave to determine the time offset from the grandmaster with high precision, the slave must know the combined path delay of all link segments as well as delays through any intervening internetworking equipment. Path delay can be determined via two standard's based methodologies, end-to-end (E2E), or peer-to-peer (P2P).

In either case, the computed path delay is impacted by any uncorrected asymmetry which can occur either in the actual network link (eg: 2 fiber links where one fiber path is substantially different in length than the other) or, all too commonly, through the incorrect (or lack of) correction of the physical (PHY) layer's ingress and egress delays. These PHY delays are typically far greater on ingress than egress for any given communication technology due to receive equalization and error correction techniques.

This test measures the Device's Port under test to determine the Port's Ingress Latency relative to the Media Dependent Interface (MDI) and DUT's timestamper timebase. It is presumed that the DUT will be correcting the timestamp based on a stored value of the known Ingress Latency for the Port. If this stored value is accurate to correct the latency to the MDI, then the measured latency error should ideally be zero.

This test is currently designated as "Informative" as no general standard's set requirement exists for how small the error must be. In the specific case of a given application for a given profile, a limit may exist but this is not the general case.

Test Setup: Connect a channel of the DSO to the 1PPS from the DUT. Set the DSO to trigger on this channel on the rising edge of the 1PPS. Set the trigger level as low as possible while avoiding noise-induced false-triggers. Connect the *Line tap* to the receiver input of the DUT, with the tap connected to a channel of the DSO. Note the delay of the path from the linetap to the DSO minus the delay of the path from the linetap to the receiver input of the DUT (using known-length cables), this delay is referred to as $LineTap_{SignalLatency}$.
Connect the *Traffic Generator* to the DUT port under test through the *Line tap*. Configure the *Traffic Generator* to send traffic that will be timestamped by the TC on the port under test and forwarded to the port not under test

where the *Traffic Monitor is connected*.
Connect the *Traffic Monitor* to a DUT port not under test to receive the traffic sent by the *Traffic Generator* containing the timestamp inserted by the TC.

Test Procedure:

Part A: *1-Step TC Port Ingress Latency.*

A:1 From the *Traffic Generator*, send traffic that the TC will timestamp on ingress on the port under test. The rate should be at least one packet a second, or faster if possible provided the DUT timestamps each packet sent.
  a) If the rate is not sufficiently high, the probability of the DSO capturing a packet sent in proximity to the DUT's 1PPS will be low.

A:2 Trigger the DSO to perform a single capture.

A:3 Analyze the capture to determine the arrival time of any received packets, as well as the embedded timestamp sent by the DUT.
  a) Download the capture trace and recover the bitstream.
  b) Correct the DSO's timebase to that of the DUT (refer to Appendix B: Ingress Latency Calculation when 1PPS available)
  c) Compare the captured frame's arrival time to that of the DUT's Ingress timestamp, correcting for any test setup delays ($1PPS_{SignalLatency} and Line Tap_{SignalLatency}$).

A:4 Repeat steps A:2 and A:3 until sufficient frames have been analyzed (>=250).

Observable Results:

Part:Step	Status	Description
A:1	INFO	The delta between the captured frame's arrival time vs the DUT's reported Ingress timestamp is reported as the Ingress timestamp error. The Max, Min, Mean, and Standard Deviation of the observed deltas is provided.

Possible Problems: None.

Group 2: Port Latency on a Single Active Link

Overview:

This group collects tests relating to the measurement of the latency of a Port of the DUT. These tests focus on establishing a baseline set of measurements for an arbitrary active link. Subsequent groups of tests examine the potential causes for latency variation and the management ability to update latency correction fields.

Note: The tests in this group are intended to be the principal tests performed in this test plan, either on an OC, BC or TC, that support either one-step or two-step, with either E2E or P2P peer delay measurement support. As some device types and capabilities may not be testable (eg: an E2E slave-only device), test modes or management access to ingress/egress time-stamps are required or the tests will not be able to be performed on such devices.

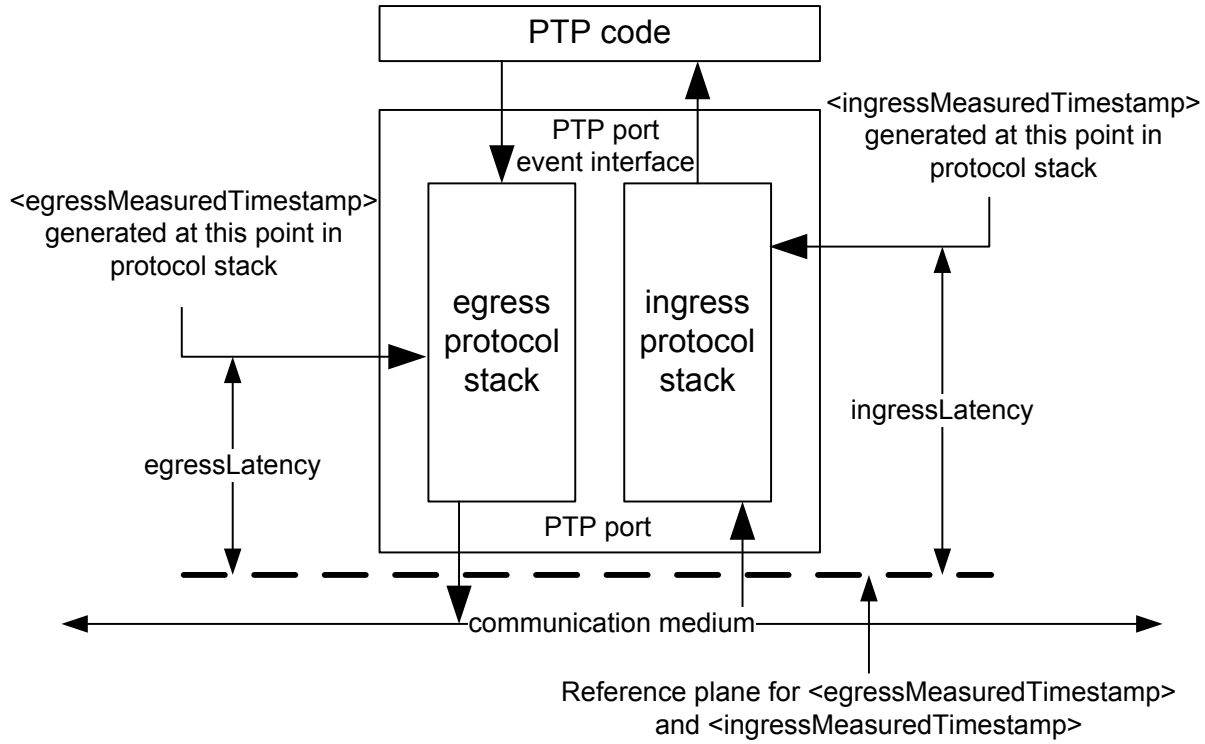

Figure G2.2: Redrawn IEEE Std 1588-2008 Figure 19: Definition of Latency Constants

Test LTNCY.2.1 — Port Egress Latency Behavior on a Single Active Link

Purpose: To measure the Device's Port under test to determine the Port's Egress Latency relative to the MDI and DUT's time-stamper time-base.

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	TC,BC or OC	DUT must either (a) respond to Delay_Req Messages; or (b) respond to Pdelay_Req Messages; or (c) provide a mechanism to insert the egress time-stamp for a packet into a subsequently transmitted packet; or (d) provide a means to the test station to read the egress time-stamp. The DUT must also provide a 1PPS signal with known delay from signal appearance at the signal header, to true one second roll-over of the timestamper.	Informative

References: [1] IEEE Std 1588-2008: clause 7.3.4.1 [3] *Ibid*: Figure 19
[2] *Ibid*: clause 7.3.4.2

Resource Requirements: One or two test stations capable of acting as both a *Traffic Generator* and *Traffic Monitor*.
Traffic Generator capable of arbitrary frame generation with hardware timestamping of transmitted frames.
Traffic Monitor capable of capturing traffic and hardware timestamping of received frames.

Modification History: 2018-03-07 — Initial Draft Release

Discussion: In an IEEE 1588 PTP network, for a slave to determine the time offset from the grandmaster with high precision, the slave must know the combined path delay of all link segments as well as delays through any intervening internetworking equipment. Path delay can be determined via two standard's based methodologies, end-to-end (E2E), or peer-to-peer (P2P).

In either case, the computed path delay is impacted by any uncorrected asymmetry which can occur either in the actual network link (eg: 2 fiber links where one fiber path is substantially different in length than the other) or, all too commonly, through the incorrect (or lack of) correction of the physical (PHY) layer's ingress and egress delays. These PHY delays are typically far greater on ingress than egress for any given communication technology due to receive equalization and error correction techniques.

This test measures the Device's Port under test to determine the Port's Egress Latency relative to the Media Dependent Interface (MDI) and DUT's timestamper timebase. It is presumed that the DUT will be correcting the timestamp based on a stored value of the known Egress Latency for the Port. If this stored value is accurate to correct the latency to the MDI, then the measured latency should ideally be zero.

Test Setup: Connect a channel of the DSO to the 1PPS from the DUT. Set the DSO to trigger on this channel on the rising edge of the 1PPS. Set the trigger level as low as possible while avoiding noise-induced false-triggers.
Connect the *Line tap* to the receiver input of the DUT port under test, with the tap connected to a channel of the DSO. Note the delay of the path from the linetap to the DSO minus the delay of the path from the linetap to the receiver input of the DUT (using known-length cables), this delay is referred to as $LineTap_{SignalLatency}$.
Connect the *Traffic Generator* to the DUT port under test through the *Line tap*. Configure the *Traffic Generator* to send traffic that will be timestamped by the DUT on the port under test.
If the DUT responds to Delay_Req or Pdelay_Req messages, only one *Traffic Monitor* is required, and the port connected is the port under test.
If the DUT is a BC or TC and can only receive a packet on one port, and emit the packet on another port (while egress time-stamping that packet), then the port emitting the packet is the port under test. In this case, two *Traffic Monitors* will be required. If the egress time stamp is provided via management access, or by another means (eg: sent as a test mode on a third port,etc) this this test is adapted to the DUT's particular test mode features.

Test Procedure:

Part A: *Port Egress Latency Behavior.*

A:1 From the *Traffic Generator*, send traffic that the DUT timestamp on egress on the port under test. The rate should be at least one packet a second, or faster if possible provided the DUT timestamps each packet sent.

a) Traffic would typically be a packet such as a Pdelay_Req that the DUT will respond to on the same port with a two-step Pdelay_Resp packet followed by a Pdelay_Resp_Follow_Up with an egress timestamp embedded within the packet.

b) Traffic should be timed such that the packet is received by the DUT sufficiently before the one second roll-over that the DUT's timestamped egress packet would be as close to the one second roll-over as possible. (eg: if a Pdelay_Req message typically takes 2ms to be responded to with a Pdelay_Resp_Follow_Up, send the Pdelay_Req from the *Traffic Generator* 2ms before the one second roll-over.)

A:2 Trigger the DSO to perform a single capture.

A:3 Analyze the capture to determine the start time of any transmitted packets, as well as the embedded timestamp sent by the DUT.

a) Download the capture trace and recover the bitstream.

b) Correct the DSO's timebase to that of the DUT (refer to Appendix A: Egress Latency Calculation when 1PPS available)

c) Compare the captured frame's start time to that of the DUT's Egress timestamp, correcting for any test setup delays ($1PPS_{SignalLatency} and Line Tap_{SignalLatency}$).

A:4 Repeat steps A:2 and A:3 until sufficient frames have been analyzed (>=1000 typically).

Observable Results:

Part:Step	Status	Description
A:1	INFO	The delta between the captured frame's start time vs the DUT's reported Egress timestamp is reported as the Egress timestamp error. The Max, Min, Mean, and Standard Deviation of the observed deltas is provided.

Possible Problems: None.

Test LTNCY.2.2 — Port Ingress Latency Behavior on a Single Active Link

Purpose: To measure the Device's Port under test to determine the Port's Ingress Latency relative to the MDI and DUT's time-stamper time-base.

Device Type Prerequisites and Compliance Classifier:

Part	Applies To Device Type	Prerequisite Conditions	Classifier
A	TC,BC or OC	DUT must either (a) respond to Delay_Req Messages; or (b) respond to Pdelay_Req Messages; or (c) provide a mechanism to insert the ingress time-stamp for a packet into a subsequently transmitted packet; or (d) provide a means to the test station to read the ingress time-stamp. The DUT must also provide a 1PPS signal.	Informative

References: [1] IEEE Std 1588-2008: clause 7.3.4.1 [3] *Ibid*: Figure 19
[2] *Ibid*: clause 7.3.4.2

Resource Requirements: One or two test stations capable of acting as both a *Traffic Generator* and *Traffic Monitor*.
Traffic Generator capable of arbitrary frame generation with hardware timestamping of transmitted frames.
Traffic Monitor capable of capturing traffic and hardware timestamping of received frames.

Modification History: 2018-03-07 — Initial Draft Release

Discussion: In an IEEE 1588 PTP network, for a slave to determine the time offset from the grandmaster with high precision, the slave must know the combined path delay of all link segments as well as delays through any intervening internetworking equipment. Path delay can be determined via two standard's based methodologies, end-to-end (E2E), or peer-to-peer (P2P).

In either case, the computed path delay is impacted by any uncorrected asymmetry which can occur either in the actual network link (eg: 2 fiber links where one fiber path is substantially different in length than the other) or, all too commonly, through the incorrect (or lack of) correction of the physical (PHY) layer's ingress and egress delays. These PHY delays are typically far greater on ingress than egress for any given communication technology due to receive equalization and error correction techniques.

This test measures the Device's Port under test to determine the Port's Ingress Latency relative to the Media Dependent Interface (MDI) and DUT's timestamper timebase. It is presumed that the DUT will be correcting the timestamp based on a stored value of the known Ingress Latency for the Port. If this stored value is accurate to correct the latency to the MDI, then the measured latency should ideally be zero.

Test Setup: Connect a channel of the DSO to the 1PPS from the DUT. Set the DSO to trigger on this channel on the rising edge of the 1PPS. Set the trigger level as low as possible while avoiding noise-induced false-triggers.
Connect the *Line tap* to the transmit output of the DUT port under test, with the tap connected to a channel of the DSO. Note the delay of the path from the linetap to the DSO minus the delay of the path from the linetap to the transmit output t of the DUT (using known-length cables), this delay is referred to as $LineTap_{SignalLatency}$.
Connect the *Traffic Generator* to the DUT port under test through the *Line tap*. Configure the *Traffic Generator* to send traffic that will be timestamped by the DUT on the port under test.
If the DUT responds to Delay_Req or Pdelay_Req messages, only one *Traffic Monitor* is required, and the port connected is the port under test.
If the DUT is a BC or TC and can only receive a packet on one port (while ingress time-stamping that packet), and emit the packet on another port, then the port receiving the packet is the port under test. In this case, two *Traffic Monitors* will be required. If the ingress time stamp is provided via management access, or by another means (eg: sent as a test mode on a third port,etc) this this test is adapted to the DUT's particular test mode features.

Test Procedure:

Part A: *Port Ingress Latency Behavior.*

A:1 From the *Traffic Generator*, send traffic that the DUT timestamp on ingress on the port under test. The rate should be at least one packet a second, or faster if possible provided the DUT timestamps each packet sent.

a) Traffic would typically be a packet such as a Pdelay_Req that the DUT will respond to on the same port with a Pdelay_Resp packet with an ingress timestamp embedded within the packet.

b) Traffic should be timed such that the packet is received by the DUT sufficiently before the one second roll-over that the DUT's timestamped egress packet would be as close to the one second roll-over as possible. (eg: if a Pdelay_Req message typically takes 1ms to be responded to, send the Pdelay_Req from the *Traffic Generator* 1ms before the one second roll-over.)

A:2 Trigger the DSO to perform a single capture.

A:3 Analyze the capture to determine the start time of any transmitted packets, as well as the embedded timestamp sent by the DUT.

a) Download the capture trace and recover the bitstream.

b) Correct the DSO's timebase to that of the DUT (refer to Appendix B: Ingress Latency Calculation when 1PPS available)

c) Compare the captured frame's start time to that of the DUT's Egress timestamp, correcting for any test setup delays $(1PPS_{SignalLatency} and Line Tap_{SignalLatency})$.

A:4 Repeat steps A:2 and A:3 until sufficient frames have been analyzed (>=1000 typically).

Observable Results:

Part:Step	Status	Description
A:1	INFO	The delta between the captured frame's start time vs the DUT's reported Ingress timestamp is reported as the Ingress timestamp error. The Max, Min, Mean, and Standard Deviation of the observed deltas is provided.

Possible Problems: None.

Appendix A Egress Latency Calculation when 1PPS available

For proper path delay calculations to occur, the egress and ingress latencies must be symmetrical at what is generally referred to as a time-stamping plane. A typical transceiver will have higher latencies on receive (ingress) than on transmit (egress). To correct for this, a PTP Port must compensate for the known asymmetrical physical layer delays to a common time-stamping plane. This plane generally should be at the media dependent interconnect (MDI) of the PTP Port (eg: RJ-45 connector). While accurate time can be relayed independent of the plane's location, IEEE 802.1AS requires the corrections to occur at the MDI such that the path delay corresponds to the actual link delay, thereby allowing for the reliable detection of undesired legacy network equipment (eg: full-duplex repeaters / buffered distributors) that would otherwise introduce packet delay variation.

Any error in the Port's correction for the egress latency to a common time-stamping plane can contribute to asymmetry and thus static error in recovered time. The process to evaluate an implementation's egress time-stamp latency when a 1PPS is present is explained in detail in this appendix.

Initial assumptions include that the implementation's transmit clock rate and time-stamper clock rate are stable over a brief observation window (tens to hundreds of microseconds). Another assumption, for the technique described in the appendix, the device under test (DUT) is presumed to not be syntonizing nor synchronizing its local clock with any other entity. Reported Egress Latency measurements will be reported in the time base of the DUT's time-stamping clock.

The methodology explained in this appendix also presumes the DUT exposes a one pulses per second (1PPS) indication driven by the DUT's time-stamper. The delay from the 1 second roll over (999,999,999ns to 000,000,000ns) to the external signal pin being driven must be known and is referred to as the $1PPS_{SignalLatency}$.

The basic setup requires a real-time digital storage oscilloscope (DSO) to capture the transmitted signaling from the DUT. For example, with 100Base-TX, this would mean the differential pair transmitted on the twisted pair cable. This differential signal is sampled at 500ps per sample or faster. The DSO is triggered by the rising edge of the 1PPS signal, with a trigger level set as low as possible to detect the event as early as possible, while avoiding false triggers.

The easiest setup for this technique involves a DUT that transmit packets that will have an egress time-stamp inserted into them as a one-step operation; otherwise, the DUT must provide the time-stamp for the time-stamped packet through some means (eg: Pdelay_Resp_Follow_Up message containing the egress time-stamp for a Pdelay_Resp message transmitted by the DUT).

With the time-stamp for each transmitted packet known, the remaining difficulty is in establishing the start of frame of each time-stamped transmitted packet relative to the DUT's 1PPS signal. This is done by first recovering the ideal clock of the transmitted signal. This clock is then used to sample the transmitted signal to determine the symbols sent as well as the start of each unit interval (UI) relative to the 1PPS from the DUT. Once the symbol data and relative time is known, it is a straightforward process to identify each packet sent, and where the start of each frame occurs within each packet. IEEE 1588-2008 defines per 7.3.4.1 the time-stamping point of an Ethernet packet as the first bit of data following the Start of Frame Delimiter (Sof or SFD), as shown in A.1 below and is quoted as follows: "Unless otherwise specified in a transport-specific annex to this standard, the message time-stamp point for an event message shall be the beginning of the first symbol after the Start of Frame (SOF) delimiter."

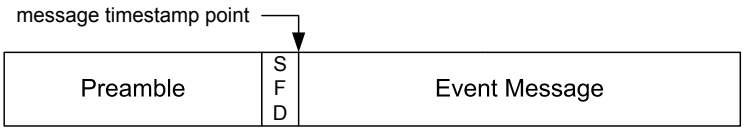

Figure A.1: Time-stamping point in Packet

For each given capture from the DSO, 'n' time-stamped frames may be observed. The DUT's time-stamp for each frame must be recorded, as well as the time the time-stamp point is observed relative to the DUT's 1PPS (generally referred to as the *relative SoF time*). If 10 frames were captured in a single capture from the DSO, the error between observed egress time and reported egress time could be readily calculated for these 10 frames, however the end result would only be valid if the time-stamper and network transmission rate were synchronous, and the DSO's sampling rate (at 500ps/sample) was also synchronous with the DUT's transmissions. As this is generally not the case, the rate difference between the transmitted time-stamped packets, the associated time-stamps, and the DSO's sampling rate must be computed and corrected. Given the high quality of most DSO samplers, the majority of any timing error would typically be in the variation of the DUT's actual transmission rate from the ideal.

When multiple packets are available in the DSO capture, the rate ratio can be determined by first computing the difference between the *relative SoF time* of a time-stamped frame and the previous *relative SoF time*. The difference between the associated time-stamp and the previous time-stamp is also computed. The *relative SoF time* difference is then divided by the associated time-stamp difference to compute the instantaneous rate ratio. This is done for all observed time-stamped frames and an average rate ratio computed. This average rate ratio is then multiplied by the originally calculated *relative SoF time*, thus correcting the *relative SoF time* to the time-stamper's timebase.

When only one packet is available in the DSO capture, the recovered bit rate of the transmitted signal can be used as this is analogous to the rate ratio determination process outlined above. The recovered bit rate divided by the nominal bit rate (eg: 8ns for 100Base-TX) thus yields the rate ratio of the DSO sample rate to the DUT's clock rate. The DUT's time-stamper and packet transmission system are generally synchronous and thus this is presumed to be the case. This rate ratio is then multiplied by the originally calculated *relative SoF time*, thus correcting the *relative SoF time* to the time-stamper's timebase. Either technique has been shown to produce identical results (to 16 significant figures), which is readily supported by inspection when the two approaches are examined.

Note, without the correction described above, the absolute value of the observed error between *relative SoF time* and associated time-stamp would grow linearly the farther the observed *relative SoF time* is from the observed 1PPS signal on the DSO, due typically to the rate difference between the DUT and the DSO. The 1PPS signal serves as the point of known commonality between the two time-bases, as this signal serves as the zero-time for the captured network signal, from which the *relative SoF time* is derived, and the zero time for the DUT's time-stamper. With the correction applied to bring the *relative SoF time* into the time-stamper's timebase, the observed error does not grow linearly, but instead varies in a Gaussian manner as expected (principally attributed to the wander of the DUT's oscillator).

As the various clocks do not change substantially within the small (200microsecond) capture window of the DSO, there is a need to collect a statistically significant number of observations to establish the range of variation of the error between *relative SoF time* and associated fractional second portion of the time-stamp. Generally a number of 100 to 250 observations are pursued, however the sample size should be large enough to establish the nature of the underlying distribution, presumed to be Gaussian in this case.

Appendix B Ingress Latency Calculation when 1PPS available

This Appendix follows a similar discussion regarding the Egress Latency calculation when a 1PPS is available. To ease identification of the differences between the two appendices, the identical text is muted (gray).

For proper path delay calculations to occur, the egress and ingress latencies must be symmetrical at what is generally referred to as a time-stamping plane. A typical transceiver will have higher latencies on receive (ingress) than on transmit (egress). To correct for this, a PTP Port must compensate for the known asymmetrical physical layer delays to a common time-stamping plane. This plane generally should be at the media dependent interconnect (MDI) of the PTP Port (eg: RJ-45 connector). While accurate time can be relayed independent of the plane's location, IEEE 802.1AS requires the corrections to occur at the MDI such that the path delay corresponds to the actual link delay, thereby allowing for the reliable detection of undesired legacy network equipment (eg: full-duplex repeaters / buffered distributors) that would otherwise introduce packet delay variation.

Any error in the Port's correction for the ingress latency to a common time-stamping plane can contribute to asymmetry and thus static error in recovered time. The process to evaluate an implementation's ingress time-stamp latency when a 1PPS is present is explained in detail in this appendix.

Initial assumptions include that the implementation's time-stamper clock rate and the Test Stations' transmit clock rate are stable over a brief observation window (tens to hundreds of microseconds). Another assumption, for the technique described in the appendix, the device under test (DUT) is presumed to not be syntonizing nor synchronizing its local clock with any other entity. Reported Ingress Latency measurements will be reported in the time base of the DUT's time-stamping clock.

The methodology explained in this appendix also presumes the DUT exposes a one pulses per second (1PPS) indication driven by the DUT's time-stamper. The delay from the 1 second roll over (999,999,999ns to 000,000,000ns) to the external signal pin being driven must be known and is referred to as the $1PPS_{SignalLatency}$.

The basic setup requires a real-time digital storage oscilloscope (DSO) to capture the transmitted signaling to and from the DUT. For example, with 100Base-TX, this would mean the differential pair received/transmitted on the twisted pair cable. This differential signal is sampled at 500ps per sample or faster. The DSO is triggered by the rising edge of the 1PPS signal, with a trigger level set as low as possible to detect the event as early as possible, while avoiding false triggers.

The easiest setup for this technique involves a DUT that receives packets that will have an ingress time-stamp inserted into them and then retransmitted out the same or a different port; otherwise, the DUT must provide the time-stamp for the time-stamped packet through some means (eg: Pdelay_Resp message containing the ingress time-stamp for a Pdelay_Req message transmitted by the DUT).

With the time-stamp for each received packet known, the remaining difficulty is in establishing the start of frame of each time-stamped received packet relative to the DUT's 1PPS signal. This is done by first recovering the ideal clock of the signal received by the DUT. This clock is then used to sample the signal received by the DUT to determine the symbols sent as well as the start of each unit interval (UI) relative to the 1PPS from the DUT. Once the symbol data and relative time is known, it is a straightforward process to identify each packet sent, and where the start of each frame occurs within each packet. IEEE 1588-2008 defines per 7.3.4.1 the time-stamping point of an Ethernet packet as the first bit of data following the Start of Frame Delimiter (Sof or SFD), as shown in B.1 below and is quoted as follows: "Unless otherwise specified in a transport-specific annex to this standard, the message time-stamp point for an event message shall be the beginning of the first symbol after the Start of Frame (SOF) delimiter."

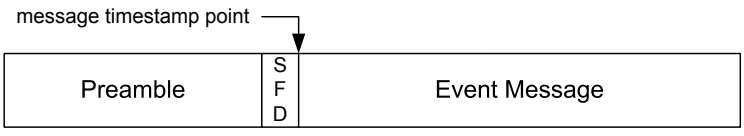

Figure B.1: Time-stamping point in Packet

Properly correcting the timebases of the DSO and DUT are further complicated in the case of determining the Ingress latency of the DUT as the link-partner providing the network signal and transmitting packets to the DUT is generally not running synchronously to the DUT's timebase. This results in the need to compensate for the rate ratio difference of both the DUT and DSO, and the Link Partner and DSO.

For each given capture from the DSO, 'n' time-stamped frames may be observed. The DUT's time-stamp for each frame must be recorded, as well as the time the time-stamp point is observed relative to the DUT's 1PPS (generally referred to as the *relative SoF time*). If 10 frames were captured in a single capture from the DSO, the error between observed ingress time and reported ingress time could be readily calculated for these 10 frames, however the end result would only be valid if the time-stamper and network transmission rate were synchronous, and the DSO's sampling rate (at 500ps/sample) was also synchronous with the DUT's transmissions. As this is generally not the case, the rate difference between the received time-stamped packets, the associated time-stamps, and the DSO's sampling rate must be computed and corrected. Given the high quality of most DSO samplers, the majority of any timing error would typically be in the variation of the DUT's actual transmission rate from the ideal, and in the case of Ingress Latency determination, the rate difference between the link-partner's transmission rate and the DUT's timestamper rate. The DUT is generally presumed to always timestamp in a consistent timebase for both Ingress and Egress timestamping purposes, thus it is guaranteed that the DUT's timestamper timebase will be advancing at a rate different than the link-partner's transmission rate. This rate difference will unavoidably manifest as a linearly increasing (or decreasing depending on positive or negative rate ratio differences between the DUT and the link-partner). This error will continue to increase until the DUT's Ingress Timestamper's next quantization level is reached, at which point the error will 'wrap' back to zero and again begin linearly increasing. Even in light of this anticpated error, the timestamper latency error's observed max minus min values should generally stay within the DUT's Ingress Timestampers quantizer's LSB.

When multiple packets are available in the DSO capture, the rate ratio is determined by first computing the difference between the *relative SoF time* of a time-stamped frame and the previous *relative SoF time*. The difference between the associated time-stamp and the previous time-stamp is also computed. The *relative SoF time* difference is then divided by the associated time-stamp difference to compute the instantaneous rate ratio. This is done for all observed time-stamped frames and an average rate ratio computed. This average rate ratio is then multiplied by the originally calculated *relative SoF time*, thus correcting the *relative SoF time* to the time-stamper's timebase. When only one packet is available in the DSO capture, the recovered bit rate of the received signal can be used as this is analogous to the rate ratio determination process outlined above. The recovered bit rate divided by the nominal bit rate (eg: 8ns for 100Base-TX) thus yields the rate ratio of the DSO sample rate to the DUT's clock rate. The DUT's time-stamper and packet transmission system are generally synchronous and thus this is presumed to be the case. This rate ratio is then multiplied by the originally calculated *relative SoF time*, thus correcting the *relative SoF time* to the time-stamper's timebase. Either technique has been shown to produce identical results (to 16 significant figures), which is readily supported by inspection when the two approaches are examined. In the Egress Latency error measurement case, only one rate ratio was necessary to be compensated for - the rate difference between consecutive timestamps from the DUT's timestamper and the difference between consecutive start of frames as timed by the DSO. In the case of Ingress Latency error measurement, this same ratio must be computed, but conveys the rate difference between the DUT's timestamper and that of the link partner's transmitted bitrate. In addition to this rate ratio, the rate ratio between the DUT's system rate and the DSO's timebase must be computed. As there is no timestamped frames being sent to the DSO from the DUT's timebase, the only option is to utilize the second methodoly outlined above and calculate the network transmission bitrate from the DUT, with the presumption the DUT's timebase is synchronous to the DUT's network transmissions. If this is not the case alternate approaches may be necessary.

Note, without the correction described above, the absolute value of the observed error between *relative SoF time* and associated time-stamp would grow linearly the farther the observed *relative SoF time* is from the observed 1PPS signal on the DSO, due typically to the rate difference between the DUT and the DSO. The 1PPS signal serves as the point of known commonality between the two time-bases, as this signal serves as the zero-time for captured network signals, from which the *relative SoF time* is derived, and the zero time for the DUT's time-stamper. With the correction applied to bring the *relative SoF time* into the time-stamper's timebase, the observed error does not grow linearly, but instead varies in Gaussian-like manner as expected.

As the various clocks do not change substantially within the small (200microsecond) capture window of the DSO, there is a need to collect a statistically significant number of observations to establish the range of variation of the error between *relative SoF time* and associated time-stamp. Generally a number of 100 to 250 observations are pursued, however the sample size should be large enough to establish the nature of the underlying distribution, presumed to have Gaussian tails at the edge of a of an otherwise uniform distribution across the DUT's minimum quantization level, resulting from the rate difference between the DUT and its link-partner. This behavior is readily seen in the example shown in B.2 below. Note that the example clearly shows a device with a 10ns timestamp granularity.

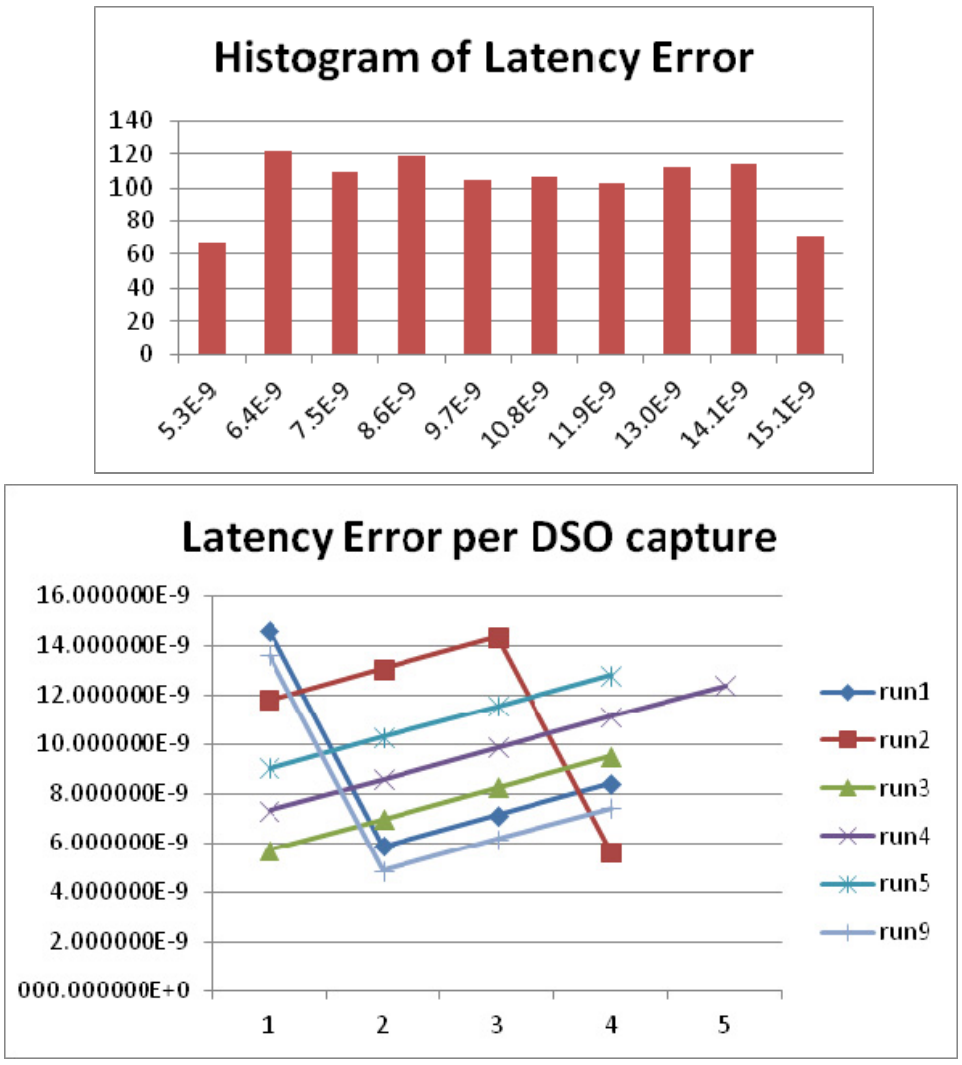

Figure B.2: Example distribution and time-stamp error of observed ingress data (250 total runs)