

UNH-IOL 10 GIGABIT ETHERNET CONSORTIUM

**SFF-8431 SFP+ Host Conformance
Test Suite
Version 1.0**

Technical Document



Last Updated: April 9, 2014

10 Gigabit Ethernet Consortium

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MODIFICATION RECORD

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Christopher Bridges: Initial preliminary draft.

April 9, 2014 Version 0.2

Michael Klempa: Minor edits

May 20, 2014 Version 1.0

Michael Klempa: Initial version

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Michael Klempa	UNH InterOperability Laboratory
AJ McQuade	UNH InterOperability Laboratory
Jeff Lapak	UNH InterOperability Laboratory
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INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the standards conformance of SFP+ hosts to the SFF-8431 Standard.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent test

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross-references to the SFF-8431 standards and other documentation that might be helpful in understanding and evaluating the test and results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the configuration of the test environment. Small changes in the configuration should not be included here, but rather included in the procedure section below.

Procedure

The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

The observable results section lists observations that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

GROUP 1: ELECTRICAL SIGNALING REQUIREMENTS

Overview:

The tests defined in this section verify the electrical signaling characteristics of the SFP+ host defined in Chapter 3 of SFF-8431. Additionally, electrical signaling characteristics for SFP+ hosts that support passive direct attach cables are defined in Appendix E of SFF-8431.

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Test 1.1 – Output AC Common Mode Voltage

Purpose: To verify that the Output AC Common Mode Voltage is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 11 – Host Transmitter Output Electrical Specifications at B
- [2] SFF-8431 Rev. 4.1 Table 33 – Host Transmitter Output Specifications at B for Cu
- [3] SFF-8431 Rev. 4.1 Appendix D.15 – AC Common Mode Voltage
- [4] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition
- [5] SFF-8431 Rev. 4.1 Appendix D.1.1 – Test Pattern Definition

Resource Requirements: See Appendix I

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ Hosts. Reference [2] specifies the transmitter characteristics for SFP+ Hosts that the optional support passive direct attach cables. These specifications include conformance requirements for the maximum Output AC Common-Mode Voltage defined in [3].

In this test, the differential amplitude is measured while the DUT is connected to the DSO. The common mode voltage can be found by averaging the signal+ and signal- at any time. RMS AC common-mode voltage may be calculated by applying the histogram function over 1 UI to the common mode signal.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT so that it is sourcing test pattern 3 (PRBS31) [4].
2. Connect the DUT's transmitter to the DSO.
3. Apply a histogram function over 1 UI of the common mode signal.
4. Measure the common mode RMS amplitude.

Observable Results:

If the DUT supports passive direct attach cables

- a. The maximum output AC common-mode voltage should be no greater than 12 mV RMS.

If the DUT does not support passive direct attach cables

- a. The maximum output AC common-mode voltage should be no more than 15 mV RMS.

Possible Problems: None.

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Test 1.2 – Output Rise and Fall Times

Purpose: To verify that the Output Rise and Fall Times are within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 12 – Host Transmitter Output Jitter and Eye Mask Specifications at B
- [2] SFF-8431 Rev. 4.1 Appendix D.6 – Rise and Fall Times
- [3] SFF-8431 Rev. 4.1 Appendix D.1.1 – Test Pattern Definition

Resource Requirements: See Appendix I

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. This specification includes conformance requirements for the rising and falling edge transition times defined in [2].

In this test, the transition time is measured while the DUT is connected to the DSO. The transition times are to be measured at the 20% and 80% levels as defined in [2]. Reference [2] also requires that the measurement be done using the square wave test pattern defined.

Test Setup: See Appendix I

Procedure:

1. Configure the DUT so that it is sourcing the eight ones eight zeroes pattern with no equalization.
2. Connect the DUT's transmitter to the DSO.
3. Measure the rising and falling edge transition times.

Observable Results:

- a. The rising and falling edge transition times should not be less than 34ps.

Possible Problems: None.

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Test 1.3 – Voltage Modulation Amplitude for 10GSFP+ Cu

Purpose: To verify that the Voltage Modulation Amplitude (VMA) is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 33 – Host Transmitter Output Specifications at B for Cu
- [2] SFF-8431 Rev. 4.1 Appendix D.7 – Voltage Modulation Amplitude (VMA)

Resource Requirements: See Appendix I

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. This specification includes conformance requirements for the VMA defined in [2].

For the purpose of this test, VMA is defined as the difference between the nominal one and zero levels of an electrical signal.

This test is only required for hosts that support Cu. However, this measurement is required for test 1.4 - Transmitter Q_{sq} .

Test Setup: See Appendix I

Procedure:

1. Configure the DUT so that it is sourcing the eight ones eight zeroes pattern.
2. Use the DSO to find the value of a time interval 8 UI long centered on the average level of the high and low section of the resulting square wave.
3. Measure the average voltage level in the central 20% of each of these time intervals.
4. VMA is the difference of these two levels.

Observable Results:

- a. The VMA should not be less than 300mV.

Possible Problems: None.

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Test 1.4 – Transmitter Q_{sq}

Purpose: To verify that the Transmitter Q_{sq} is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 12 – Host Transmitter Output Jitter and Eye Mask Specifications at B
- [2] SFF-8431 Rev. 4.1 Table 33 – Host Transmitter Output Specifications at B for Cu
- [3] SFF-8431 Rev. 4.1 Appendix D.8 – Relative Noise (RN)

Resource Requirements: See Appendix I

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. Reference [2] specifies the transmitter characteristics for 10GSFP+ Cu hosts. This specification includes conformance requirements for the RN defined in [2].

For this test, the transmitter Q_{sq} is found by the equation:

$$Q_{sq} = \frac{1}{RN}$$

RN is found by the equation:

$$RN = \frac{2 * noise(RMS)}{(xMA)}$$

Where xMA is defined as VMA for the purpose of this test and noise(RMS) is defined by the equation:

$$noise(RMS) = \sqrt{\frac{logicONEnoise(RMS)^2 + logicZEROnoise(RMS)^2}{2}}$$

Test Setup: See Appendix I

Procedure:

1. Measure logicONEnoise(RMS) and logicZEROnoise(RMS) and the VMA.
2. Calculate noise(RMS)
3. Calculate RN using noise(RMS) and the VMA.
4. Calculate Q_{sq}

Observable Results:

If the DUT supports passive direct attach cables

- a. The Q_{sq} should not be less than 63.1.

If the DUT does not support passive direct attach cables

- a. The Q_{sq} should not be less than 50.

Possible Problems: None.

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Test 1.5 – Single Ended Output Voltage Range

Purpose: To verify that the single ended output voltage range is within conformance limits.

References:

[1]SFF-8431 Rev. 4.1 Table 11 Host Transmitter Output Electrical Specifications at B

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. This specification includes conformance requirements for the single ended output voltage range.

Test Setup: See Appendix I

Procedure:

1. Connect the DUT to the DSO
2. Measure the single ended output voltage for both positive and negative channels.

Observable Results:

- b. The single ended output voltages should be within -0.3 V and 4.0 V.

Possible Problems: None.

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Test 1.6 – Eye Mask

Purpose: To verify that the Eye Mask Hit Ratio is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 12 – Host Transmitter Output Jitter and Eye Mask Specifications at B
- [2] SFF-8431 Rev. 4.1 Appendix D.2 – Eye Mask Compliance
- [3] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

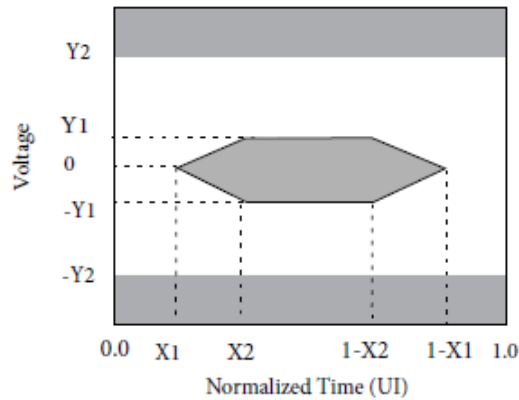
Resource Requirements: See Appendix I

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ devices. This specification includes conformance requirements for the eye mask compliance defined in [2].

In this test, the eye diagram is measured while the DUT is connected to DSO. Reference [1] also requires that the DUT be transmitting test pattern 3 (PRBS31) defined in [3].



$$X1=0.12 \text{ UI}$$

$$X2=0.33 \text{ UI}$$

$$Y1=95 \text{ mV}$$

$$Y2=350 \text{ mV}$$

Test Setup: See Appendix I

Procedure:

1. Configure the DUT so that it is sourcing test pattern 3 (PRBS31).
2. Connect the DUT's transmitter to DSO.
3. Capture the eye diagram.

Observable Results:

- a. The eye mask hit ratio should not exceed 5×10^{-5}

Possible Problems: None.

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Test 1.7 – Total Jitter

Purpose: To verify that the Total Jitter (TJ) is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 12 – Host Transmitter Output Jitter and Eye Mask Specifications at B
- [2] SFF-8431 Rev. 4.1 Appendix D.5 – 99% Jitter (J2) and Total Jitter (TJ)
- [3] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: See Appendix I

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ host devices. This specification includes conformance requirements for the peak-to-peak transmit jitter defined in [2].

Total jitter is defined as the sum of the deterministic jitter and random jitter. Test pattern PRBS31 as defined in [3] will be used.

Test Setup: See Appendix I

Procedure:

1. Set the DUT to transmit test pattern 3 (PRBS31).
2. Connect the DUT's transmitter to DSO.
3. Measure the total jitter.

Observable Results:

- a. The total jitter should not exceed 0.28 UI(p-p)

Possible Problems: None.

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Test 1.8 – Data Dependent Jitter

Purpose: To verify that the Data Dependent Jitter (DDJ) is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 12 – Host Transmitter Output Jitter and Eye Mask Specifications at B
- [2] SFF-8431 Rev. 4.1 Appendix D.3 – Data Dependent Jitter (DDJ) and Pulse Width Shrinkage (DDPWS)
- [3] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: See Appendix I

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ host devices. This specification includes conformance requirements for the data dependent jitter defined in [2].

A PRBS31 test pattern as defined in [3] will be used. Data dependent jitter is defined as:

$$DDJ = \max(\Delta t_1, \Delta t_2, \dots, \Delta t_n) - \min(\Delta t_1, \Delta t_2, \dots, \Delta t_n)$$

Test Setup: See Appendix I

Procedure:

1. Set the DUT to transmit test pattern 3 (PRBS31).
2. Use the DSO to find DDJ.

Observable Results:

- a. The data dependent jitter should not exceed 0.1 UI(p-p)

Possible Problems: None.

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Test 1.9 – Data Dependent Pulse Width Shrinkage

Purpose: To verify that the Data Dependent Pulse Width Shrinkage (DDPWS) is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 12 – Host Transmitter Output Jitter and Eye Mask Specifications at B
- [2] SFF-8431 Rev. 4.1 Appendix D.3 – Data Dependent Jitter (DDJ) and Pulse Width Shrinkage (DDPWS)
- [3] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: See Appendix I

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ host devices. This specification includes conformance requirements for the data dependant pulse width shrinkage defined in [2]. DDPWS is determined as the difference between one symbol period and the minimum of all the differences between pairs of adjacent edges. PRBS31 as defined in [3] will be used.

Test Setup: See Appendix I

Procedure:

1. Set the DUT to transmit test pattern 3 (PRBS31).
2. Use the DSO to find DDPWS.

Observable Results:

- a. The data dependent jitter should not exceed 0.055 UI(p-p)

Possible Problems: None.

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Test 1.10 – Uncorrelated Jitter

Purpose: To verify that the Uncorrelated Jitter (UJ) is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 12 – Host Transmitter Output Jitter and Eye Mask Specifications at B
- [2] SFF-8431 Rev. 4.1 Appendix D.4 – Uncorrelated Jitter (UJ)
- [3] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: See Appendix I

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ host devices. This specification includes conformance requirements for the uncorrelated jitter defined in [2]. UJ is defined as a measure of any jitter that is un-correlated to the 64B/66B bit stream. PRBS31 as defined in [3] will be used.

Test Setup: See Appendix I

Procedure:

1. Set the DUT to transmit test pattern 3 (PRBS31).
2. Use the DSO to find UJ.

Observable Results:

- a. The uncorrelated jitter should not exceed 0.023 UI(RMS)

Possible Problems: None.

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Test 1.11 – TWDP_C for 10GSFP+ Cu

Purpose: To verify that the TWDP_C is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 33 – Host Transmitter Output Specifications at B for Cu
- [2] SFF-8431 Rev. 4.1 Appendix G – Matlab Code for TWDP
- [3] SFF-8431 Rev. 4.1 Table 34 – 10GSFP+ Cu TWDP_C Stressor
- [4] IEEE Std. 802.3-2012, subclause 68.6.1 – Test patterns

Resource Requirements: See Appendix I

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ host devices. This specification includes conformance requirements for the maximum TWDP_C where the stressors are specified in [2]. Reference [3] contains the Matlab code required for this test. PRBS9 as defined in [4] will be used.

This test is only required for hosts that support passive direct attach cables.

Test Setup: See Appendix I

Test Procedure:

1. Configure the DUT so that it is sourcing PRBS9.
2. Connect the DUT's transmitter to the DSO.
3. Capture an entire PRBS9 pattern.
4. Use the Matlab script in [3] to calculate the TWDP_C

Observable Results:

- a. The Maximum TWDP_C should not exceed 10.7 dBe.

Possible Problems: None.

GROUP 2: IMPEDANCE REQUIREMENTS

Overview:

The tests defined in this section verify the impedance characteristics of the SFP+ hosts defined in Chapter 3 of SFF-8431.

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Test 2.1 – Termination Mismatch

Purpose: To verify that the Termination Mismatch is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 11 – Host Transmitter Output Electrical Specifications at B
- [2] SFF-8431 Rev. 4.1 Appendix D.16 – Termination Mismatch

Resource Requirements: See Appendix II

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. This specification includes conformance requirements for termination mismatch defined in [2].

For the purpose of this test, the termination mismatch is defined as the percentage difference between the two low-frequency impedances to common of a differential electrical port.

$$\Delta Z_m = 2 * \frac{Z_p - Z_n}{Z_p + Z_n} * 100$$

Test Setup: See Appendix II

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's transmitter to the VNA through the module compliance board.
3. Observe the positive and negative impedances of the DUT at 1MHz.
4. Using the values from the positive and negative impedances, compute the termination mismatch.

Observable Results:

- a. The termination mismatch at 1MHz should not exceed 5%.

Possible Problems: None.

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Test 2.2 – Differential S-Parameters

Purpose: To verify that the Differential S-Parameters are within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 11 – Host Transmitter Output Electrical Specifications at B
- [2] SFF-8431 Rev. 4.1 Table 13 - Host Receiver Input Electrical Specifications at C and C”

Resource Requirements: See Appendix II

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. This specification includes conformance requirements for the differential output/input return loss.

For frequencies from 10 MHz to 11.1 GHz, both the differential input and output return loss of the driver should not exceed the limit given in the equation below:

$$\left\{ \begin{array}{ll} -12 & 0.01 \leq f < 2 \text{ GHz} \\ -6.68 + 12.1 * \log_{10} \left(\frac{f}{5.5} \right) & 2 < f \leq 11.1 \text{ GHz} \end{array} \right\} (dB)$$

Test Setup: See Appendix II

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT’s transmitter to the VNA.
3. Measure the differential output/input return loss at the DUT transmitter from 10 MHz to 11.1 GHz.

Observable Results:

- a. The differential output return loss should exceed the limits described by [1].
- b. The differential input return loss should exceed the limits described by [2].

Possible Problems: None.

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Test 2.3 – Reflected Input Differential to Common Mode Conversion

Purpose: To verify that the Reflected Differential to Common Mode Conversion is within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 13 - Host Receiver Input Electrical Specifications at C and C''

Resource Requirements: See Appendix II

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. This specification includes conformance requirements for the reflected differential to common mode conversion.

For frequencies from 10 MHz to 11.1 GHz, the reflected differential to common mode conversion of the receiver should not exceed the limit given in the equation below:

$$\{-10 \qquad 0.01 \leq f < 11.1 \text{ GHz}\} \text{ (dB)}$$

Test Setup: See Appendix II

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's receiver to the VNA.
3. Measure the reflection coefficient at the DUT receiver from 10 MHz to 11.1 GHz.

Observable Results:

- a. Differential to common mode return loss should exceed the limit line as specified in [1].

Possible Problems: None.

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Test 2.4 – Common Mode Output Reflection Coefficient

Purpose: To verify that the Common Mode Output Reflection Coefficient is within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 11 - Host Transmitter Output Electrical Specifications at B

Resource Requirements: See Appendix II

Last Modification: April 9, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ hosts. This specification includes conformance requirements for the common mode output reflection coefficient.

For frequencies from 10 MHz to 11.1 GHz, the reflected differential to common mode conversion of the transmitter should not exceed the limit given in the equation below:

$$\left\{ \begin{array}{ll} -7 + 1.6 * f & 0.01 \leq f < 2.5 \text{ GHz} \\ -3 & 2.5 \leq f < 11.1 \text{ GHz} \end{array} \right\} \text{ (dB)}$$

Test Setup: See Appendix II

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's transmitter to the VNA.
3. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.

Observable Results:

- a. The common mode return loss should exceed the limit line as specified in [1].

Possible Problems: None.

GROUP 3: RECEIVER REQUIREMENTS

Overview:

The test defined in this section verifies receiver characteristics of the SFP+ hosts defined in Chapter 3 of SFF-8431.

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Test 3.1 – Receiver Bit Error Rate Test for Hosts Supporting Limiting Modules

Purpose: To verify that the Receiver BER test for Hosts Supporting Limiting Modules is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 14 – Host Receiver Supporting Limiting Module Input Compliance Test Signal Calibrated at C”
- [2] SFF-8431 Rev. 4.1 Appendix D.5 – 99% Jitter (J2) and Total Jitter (TJ)
- [3] SFF-8431 Rev. 4.1 Appendix D.11 – Test Method for a host receiver for a limiting module
- [4] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: Appendix III

Last Modification: September 23, 2013

Discussion:

Reference [1] and [2] specify the required BER for host receivers at test point C”. Reference [1] contains information on the stress generator settings required for this test.

In this test, there are two test conditions; once each for the sensitivity and overload vertical eye parameters conditions. BER is measured while the DUT is subjected to a compliant input signal with interference as specified in [1]. The jitter tolerance test setup in Figure 50 or its equivalent shall meet the receiver eye mask defined in [1]. Random jitter is added to the test signal using an interference generator which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The random interference generator must have a minimum power spectrum -3 dB point of 6 GHz with a crest factor of no less than 7. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask defined in [3]. The compliance test pattern will be used. For this test, the maximum allowable hit ratio is 10^{-12} . The failure probability for the eye masks or eye mask hit ratio is defined as the rate at which the signal will cross the eye mask.

Test Setup: Appendix III

Procedure:

1. Set the BERT to transmit test pattern 3 (PRBS31) that meets the requirements of [1] for the sensitivity vertical eye parameter condition.
2. Measure the BER at the DUT.
3. Repeat this test for the overload vertical eye parameter condition.

Observable Results:

- a. The BER should be no greater than 10^{-12} for both cases.

Possible Problems: None.

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Test 3.2 – Receiver Bit Error Rate Test for Hosts Supporting Linear Modules

Purpose: To verify that the Receiver BER test for Hosts Supporting Linear Modules is within the conformance limits.

References:

- [1] SFF-8431 Rev. 4.1 Table 15 – Host receiver supporting linear module input compliance test signal calibrated at C"
- [2] SFF-8431 Rev. 4.1 Table 35 – 10GSFP+ Host Receiver Input Stress Generator at C"
- [3] SFF-8431 Rev. 4.1 Appendix D.5 – 99% Jitter (J2) and Total Jitter (TJ)
- [4] SFF-8431 Rev. 4.1 Table 35 10GSFP+ Host receiver input stress Generator at C"
- [5] SFF-8431 Rev. 4.1 Appendix D.13.1 – Test description and procedure for host receiver for linear module
- [6] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: Appendix III

Last Modification: September 23, 2013

Discussion:

Reference [1] and [3] specify the required BER for host receivers at test point C". References [1] and [2] contain information on the stress generator settings required for this test.

In this test, there are two test conditions; once each for the sensitivity and overload vertical eye parameter conditions. This test also needs to be done over each compliance stress test condition [1]. BER is measured while the DUT is subjected to a compliant input signal with interference as specified in [1]. The jitter tolerance test setup in Figure 52 or its equivalent shall meet the receiver eye mask defined in [1].

A noise source defined in [1] is added which has a spectrum of the noise source at the summing point is white with a 3 dB frequency of at least 10 GHz. The crest factor should be at least 6. The filter bandwidth will depend on the WDP case, which are defined in [5]. The cross talk sourcing pattern will be PRBS31. Under all specified test conditions, a BER of better than 1×10^{-12} shall be achieved. The transmitter of the port under test and all other ports operate in normal operation, including termination. The transmitter of the port being tested is terminated through the Host Compliance Board with a DC block and 50Ω at each Tx SMA connector. The failure probability for the eye masks or eye mask hit ratio is defined as the rate at which the signal will cross the eye mask.

Test Setup: Appendix III

Procedure:

1. Set the BERT to transmit test pattern 3 (PRBS31) that meets the requirements of [1] for the sensitivity vertical eye parameter condition.
2. Measure the BER at the DUT.
3. Repeat this test for the overload vertical eye parameter condition.
4. Repeat this test for all appropriate application stressors.

Observable Results:

- a. The BER should be no greater than 10^{-12} for all testable conditions.

Possible Problems: None.

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

*The University of New Hampshire
InterOperability Laboratory*

Appendix I - Setup for Electrical signaling measurements

Purpose: To specify the setup for electrical based tests in this test suite

References:

[6] SFF-8431 Rev. 4.1 Subclause 3.3.1- Host Compliance Points

Resource Requirements:

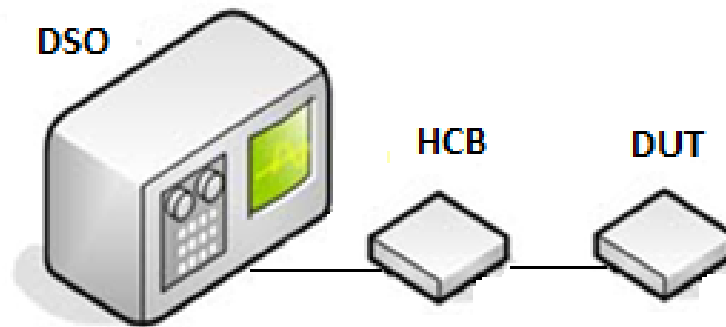
- DSO
- SFP+ Host Compliance Boards

Last Modification: September 23, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:

The DUT output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



*The University of New Hampshire
InterOperability Laboratory*

Appendix II - Setup for VNA measurements

Purpose: To specify the setup for VNA based tests in this test suite

References:

[1] SFF-8431 Rev. 4.1 Subclause 3.3.1- Host Compliance Points

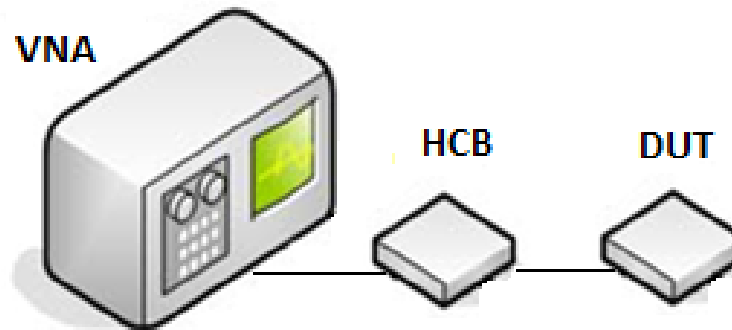
Resource Requirements:

- VNA
- SFP+ Module Compliance Board.

Last Modification: September 23, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The DUT output is connected to the host compliance board which is then connected to the VNA. The VNA should be properly calibrated before use.

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InterOperability Laboratory*

Appendix III - Setup for receiver tests

References:

- [1] SFF-8431 Rev. 4.1 Subclause 3.3.1- Host Compliance Points
- [2] SFF-8431 Rev. 4.1 Table 14- Host receiver supporting limiting module Input compliance test signal calibrated at C”
- [3] SFF-8431 Rev. 4.1 Table 15 Host receiver supporting linear module input compliance test signal calibrated at C”
- [4] SFF-8431 Rev. 4.1 Table 35 10GSFP+ Host receiver input stress Generator at C”

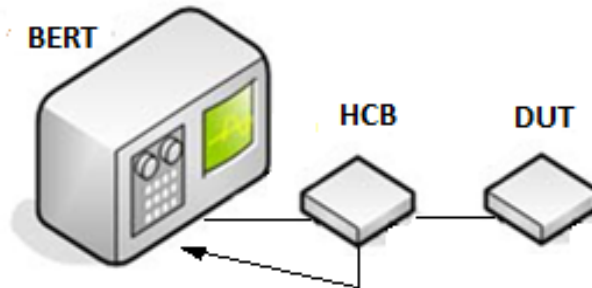
Resource Requirements:

- DSO
- BERT
- De-emphasis Signal Converter
- SFP+ Module Compliance Boards

Last Modification: September 23, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The BERT sends traffic through the de-emphasis signal converter to the DUT connected to a SFP+ host compliance board. This traffic is then looped back through the host compliance board into a DSO. The test setup should be configured to create the following stress values:

For test 3.1 use reference [2] to calibrate the crosstalk source. For test 3.2 use reference [3] to calibrate the crosstalk source. For devices supporting Cu the additional requirements in reference [4] must also be met