Ethernet

MDIO Auto-Negotiation Registers Test Suite For Twisted-Pair PHYs

V1.0

Technical Document

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MODIFICATION RECORD

Revision	Release Date	Author(s)	Comments
1.0.0	January 7, 2015	Kathryn Dube, Stephen Johnson	Initial Release

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Kathryn Dube	University of New Hampshire
Jeffrey Lapak	University of New Hampshire
Stephen Johnson	University of New Hampshire

Definitions

DUT: Device under test.

EEE: Energy Efficient Ethernet.

Link partner: The device at the opposite end of a link segment from the local station.

MDIO: Management Data Input Output.

Page Sequence: A group of FLP Bursts containing a Message Page and its specified number of Unformatted Pages with proper Flag field bit values.

INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (UNH-IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functioning of their Clause 45 Auto-Negotiation based products. The tests do not determine if a product conforms to the IEEE 802.3 standard, nor are they purely interoperability tests. Rather, they provide one method to isolate problems within an auto-negotiating device. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other auto-negotiating devices. However, combined with satisfactory operation in the UNH-IOL's interoperability test bed, these tests provide a reasonable level of confidence that the device under test (DUT) will function well in most auto-negotiating environments.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross-references to the IEEE 802.3 standards and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification
This specifies the date of the last modification to this test.

Discussion
The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup
The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure
The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results
The observable results section lists observables that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems
This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

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GROUP 1: Control Registers

Scope: The following tests cover Control Registers specific to Auto-Negotiation.

Overview: These tests are designed to verify that the DUT properly implements the Control Registers defined in the MDIO interface register set as it pertains to the Auto-Negotiation function. The register functions tested are defined in Clause 45 and Clause 55 of the IEEE 802.3 standard.

NOTE: These tests are performed for the Ethernet Consortia. These tests cannot be performed if MDIO interface register access is not provided.

Test #MDIO.1.1: AN Reset

Purpose: To verify that bit 7.0.15 resets the PHY.

References:

[1] IEEE Std 802.3-2012, subclause 28.3.1 – State diagram variables
[2] IEEE Std 802.3-2012, subclause 45.2.7.1.1 – AN reset
[3] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram
[4] IEEE Std 802.3-2012, Table 28-8 – State diagram variable to MII register mapping
[5] IEEE Std 802.3-2012, Table 45-181 – AN control register bit definitions

Resource Requirements: See **Appendix 22.A**

Last Modification: February 23, 2015

Discussion: Bit 7.0.15 of the AN Control Register gives management the ability to reset all of the AN Registers, as well as restarting the Auto-Negotiation process. The default value of bit 7.0.15 is zero. The default value for each bit of the Control Register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default Value of Bit 7.0.15

1. Initialize the DUT.
2. Read Register 7.0 twice.

Part b: Operational State after AN Reset

3. Set bit 7.0.15 to 1.
4. Read Register 7.0.

Part c: Auto-Negotiation State after AN Reset

5. Configure the DUT to transmit its Base Page.
6. Set bit 7.0.15.
7. Observe transmissions from the DUT.

Part d: Resetting of the AN Control Register

8. Initialize the DUT.
9. Read Register 7.0.
10. Set Register 7.0 to a value that is different from the value found in the previous step.
11. Set bit 7.0.15 to one.
12. Read Register 7.0.

Observable Results:

a. The default value of bit 7.0.15 should be 0.
b. After an AN Reset, the PHY should be in an operational state.
c. The DUT should cease transmissions for break_link_timer, and then restart Auto-Negotiation by sending its Base Page.
d. The DUT should set Register 7.0 to its default value after an AN Reset.

Possible Problems: If the DUT does not have a default value in Register 7.0, then part d cannot be performed.

Test #MDIO.1.2: Auto-Negotiation Enable

Purpose: To verify that bit 7.0.12 enables and disables the Auto-Negotiation process.

References:

[1] IEEE Std 802.3-2012, sublcause 22.2.4.1.4 – Auto-Negotiation enable
[2] IEEE Std 802.3-2012, sublcause 28.3.1 – State diagram variables
[3] IEEE Std 802.3-2012, subclause 45.2.1.1.3 – Speed selection
[4] IEEE Std 802.3-2012, subclause 45.2.7.1.3 – Auto-Negotiation enable
[5] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram
[6] IEEE Std 802.3-2012, Table 45-181 – AN control register bit definitions
[7] IEEE Std 802.3-2012, Table 45-182 – AN status register

Resource Requirements: See **Appendix 22.A**.

Last Modification: February 23, 2015

Discussion: Management has the ability to enable Auto-Negotiation by setting bit 7.0.12 to one and to disable Auto-Negotiation by setting bit 7.0.12 to zero. If the management has set bit 7.0.12 to zero, a link will be established using bits 1.0.13, 1.0.6 and 1.0.5:2. When bit 7.0.12 is set to one, the DUT should transmit FLP Bursts and establish a link using the Auto-Negotiation process. The default value of bit 7.0.12 is one if the device supports the Auto-Negotiation process.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default Value of Bit 7.0.12

1. Perform an AN Reset.
2. Read Register 7.0.

Part b: Disable Auto-Negotiation

3. Enable Auto-Negotiation.
4. Set bit 7.0.12 to 0.
5. Observe transmissions from the DUT.

Part c: break_link_timer Before Link Signaling

6. Repeat steps 3-5.
7. If present, measure the gap between the last FLP Burst and the start of link signaling.

Part d: Enable Auto-Negotiation

8. Disable Auto-Negotiation.
9. Set bit 7.0.12 to 1.
10. Observe transmissions from the DUT.

Observable Results:

a. If the DUT supports the Auto-Negotiation function, the default value of 7.0.12 should be 1.
b. The DUT should cease Auto-Negotiation and proceed to transmit valid link signaling (based on bits 1.0.6, 1.0.13 and 1.0.5:2).
c. INFORMATIVE: The DUT may wait break_link_timer before transmitting link signaling.
d. The DUT should cease link signaling, wait break_link_timer, and then transmit its Base Page.

Possible Problems: If the PHY does not maintain a default value in Register 7.0, part a cannot be performed. If Auto-Negotiation cannot be disabled then part c cannot be performed.

Test #MDIO.1.3: Extended Next Page Control

Purpose: To verify that bit 7.0.13 controls the sending of Extended Next Pages.

References:

[1] IEEE Std 802.3-2012, sublcause 28.2.3.4 – Next Page function
[2] IEEE Std 802.3-2012, subclause 45.2.7.1.2 – Extended Next Page control
[3] IEEE Std 802.3-2012, subclause 45.2.7.6 – AN advertisement register
[4] IEEE Std 802.3-2012, Table 45-183 – AN advertisement register bit definitions

Resource Requirements: See **Appendix 22.A**.

Last Modification: February 23, 2015

Discussion: When bit 7.0.13 is set to one, Extended Next Pages are exchanged if both the DUT and its Link Partner are capable. Bit 7.0.13 should be set to one if a device desires to enable the exchange of Extended Next Pages. If the Extended Next Page Ability bit (bit 7.16.12) is set to zero, a write to bit 7.0.13 should have no effect. If bit 7.16.12 is set to 1, the DUT should not allow bit 7.0.13 to be set to 0, or when bit 7.0.13 is set to 0, the DUT should set bit 7.16.12 to 0. This is done so that the advertised ability of the PHY matches the DUTs desire to transmit Extended Next Pages. The default value of bit 7.0.13 is 1 when bit 7.16.12 is set to 1. When bit 7.16.12 is set to 0, bit 7.0.13 should be 0.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default Value of Bit 7.0.13

1. Initialize the DUT.
2. Read bit 7.16.12.
3. Read bit 7.0.13

Part b: Write Ability of Bit 7.0.13 when an Extended Next Page Exchange is not Desired

1. Set bit 7.16.12 to 0.
2. Read bit 7.0.13.
3. Set bit 7.0.13 to 1.
4. Read bit 7.0.13.

Part c: XNP Control and XNP Advertisement Mismatch When 7.16.12 is Set to 0

5. Set bits 7.16.12 and 7.0.13 to 1.
6. Set bit 7.16.12 to 0.
7. Read bit 7.0.13.
8. Send a Base Page with the Acknowledge, Next Page, and Extended Next Page bits set to one to the DUT to put it into the COMPLETE ACKNOWLEDGE state.
9. Observed transmissions from the DUT.

Part d: XNP Control and XNP Advertisement Mismatch When 7.16.12 is Set to 1

10. Set bit 7.16.12 to 1.
11. Set bit 7.0.13 to 0.
12. Read bits 7.0.13 and 7.16.12.

Observable Results:

a. If bit 7.16.12 is set to 1, then the default value of bit 7.0.13 is 1. If bit 7.16.12 is set to 0, then the default value of bit 7.0.13 is 0.
b. The DUT should allow bit 7.0.13 to be set to 1.
c. The DUT should enter the COMPLETE ACKNOWLEDGE state and send a Non Extended Next Page.
d. The DUT should not allow bit 7.0.13 to be set to 0 when bit 7.16.12 is set to 1, or the DUT should set bit 7.16.12 to 0 when bit 7.0.13 is set to 0.

Possible Problems: If the PHY does not maintain a default value in Register 7.0, part a cannot be performed. During parts b and d, it may not be possible to read the value of Register 7.0 before management changes the value.

Test #MDIO.1.4: Restart Auto-Negotiation

Purpose: To verify that bit 7.0.9 restarts Auto-Negotiation.

References:

[1] IEEE Std 802.3-2012, subclause 22.2.4.1.7 – Restart Auto-Negotiation
[2] IEEE Std 802.3-2012, subclause 28.3.1 – State diagram variables
[3] IEEE Std 802.3-2012, subclause 45.2.7.1.4 – Restart Auto-Negotiation
[4] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram
[5] IEEE Std 802.3-2012, Table 45-181 – AN control register bit definitions
[6] IEEE Std 802.3-2012, Table 45-182 – AN status register

Resource Requirements: See **Appendix 22.A**

Last Modification: February 23, 2015

Discussion: The AN Control Register allows management to restart the Auto-Negotiation process by setting bit 7.0.9 to 1. This restarts the Auto-Negotiation process without resetting the entire PHY. The default value of bit 7.0.9 is 0.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default value of bit 7.0.9

1. Perform an AN Reset
2. Read register 7.0.

Part b: Restarting the Auto-Negotiation Process

3. Enable Auto-Negotiation.
4. Set bit 7.0.9 to 1.
5. Observe transmissions from the DUT.

Observable Results:

a. The default value of bit 7.0.9 should be 0.
b. The DUT should cease transmissions, wait approximately break_link_timer, and then restart the Auto-negotiation process by transmitting its Base Page.

Possible Problems: If the PHY does not maintain a default value in Register 7.0, part a cannot be performed.

Test #MDIO.1.5: Speed Selection

Purpose: To verify that the DUT transmits appropriate signaling according to bits 1.0.6, 1.0.13, 1.0.5:2, and 1.7.10:0 when Auto-Negotiation has been disabled.

References:

[1] IEEE Std 802.3-2012, subclause 45.2.1.1.3 – Speed Selection
[2] IEEE Std 802.3-2012, subclause 45.2.1.6.1 – PMA/PMD Type Selection
[3] IEEE Std 802.3-2012, Table 45-4 – PMA/PMD control 1 register bit definitions
[4] IEEE Std 802.3-2012, Table 45-7 – PMA/PMD control 2 register bit definitions

Resource Requirements: See **Appendix 22.A**

Last Modification: March 17, 2015

Discussion: Link speed can be selected using either the Auto-Negotiation process, or manual speed selection. When Auto-Negotiation is disabled, bits 1.0.6, 1.0.13, 1.0.5:2, and 1.7.5:0 should configure the DUT based on the following tables. When the DUT is configured for 1000BASE-T operation, it should transmit Base Pages advertising 1000BASE-T support only (ie. FLP Bursts advertising 8001) or cease all transmissions. When the DUT is configured for 10GBASE-T operation, it should transmit Base Pages advertising Extended Next Page support only (ie. FLP Bursts advertising 9001) or cease all transmissions.

When Auto-Negotiation is enabled, bits 1.0.6, 1.0.13 and 1.0.5:2 can be read or written, however, writing to these bits should have no effect on the link configuration. When a link has been established, these bits may be written by management to reflect the operating speed of the link. The default values of bits 1.0.6, 1.0.13, and 1.5:2 should reflect a supported speed at which the PHY can operate according to Register 1.4 (PMA/PMD speed ability register). The management entity may not allow unsupported speeds to be written.

Value of bit 1.0.6	Value of bit 1.0.13	Speed
0	0	10BASE-T
0	1	100BASE-TX
1	0	1000BASE-T
1	1	Bits 1.0.5:2 select speed

VALUE OF BITS 1.0.5:2	SPEED
0000	10GBASE-T
0001	10PASS-TS/2BASE-TL
0010	40GB/S

0011	100GB/S
X1XX	RESERVED
1XXX	RESERVED

VALUE OF BITS 1.7.5:0	SPEED
001111	10BASE-T
001110	100BASE-TX
001100	1000BASE-T
001001	10GBASE-T

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default Value of Bits 1.0.6, 1.0.13, 1.0.5:2, and 1.7.5:0:

1. Perform an AN reset.
2. Read bits 1.0.6, 1.0.13, 1.0.5:2, and 1.7.5:0.

Part b: Supported Speed Selection with Auto-Negotiation Disabled

3. Disable Auto-Negotiation.
4. Set bits 1.0.6, 1.0.13, 1.0.5:2, and 1.7.5:0 to a supported speed.
5. Observe transmissions from the DUT.
6. Repeat steps 3-5 with all supported combinations in the tables above.

Part c: Unsupported Speed Selection with Auto-Negotiation Disabled

7. Disable Auto-Negotiation.
8. Set bits 1.0.6, 1.0.13, and 1.0.5:2 to an unsupported speed.
9. Read Registers 1.0.
10. Repeat steps 7-9 with all unsupported combinations in the tables above.

Part d: Behavior with Unsupported Speed Selections with Auto-Negotiation Disabled

11. Repeat steps 7 and 8.
12. Observe transmissions from the DUT.
13. Repeat steps 11 and 12 with all unsupported combinations that the DUT allows to be written.

Part e: Unsupported Type Selection with Auto-Negotiation Disabled

14. Disable Auto-Negotiation.
15. Set bits 1.7.5:0 to an unsupported speed.
16. Read Registers 1.7.
17. Repeat steps 14-16 with all unsupported combinations in the tables above.

Part f: Setting Bits 1.0.6, 1.0.13 with Auto-Negotiation Enabled

18. Enable Auto-Negotiation
19. Establish a link with the DUT.
20. Set bit 1.0.6 to one and bit 1.0.13 to zero.
21. Repeat step 13 setting bit 1.0.6 to zero and a bit 1.0.13 to one.

Part g: Indication of Link Speed

22. Enable Auto-Negotiation.
23. Establish a link at a speed not indicated by bits 1.0.6, 1.0.13, and 1.0.5:2 using Auto-Negotiation.
24. Read the value of bits 1.0.6, 1.0.13, and 1.0.5:2.

Observable Results:

a. The default value of bits 1.0.6, 1.0.13, 1.0.5:2, and 1.7.5:0 should reflect a supported speed.
b. The DUT should transmit appropriate signaling according to the table above.
c. INFORMATIVE: The DUT may or may not allow bits 1.0.6, 1.0.13, and 1.0.5:2 to be set to unsupported speeds.
d. If the DUT allows unsupported speeds to be selected, the DUT should not transmit any signaling.
e. The DUT should not allow bit 1.7.5:0 to be set to unsupported type abilities.
f. The setting of bits 1.0.6 and 1.0.13 should not have any effect on the link configuration.
g. INFORMATIVE: When Auto-Negotiation is enabled, the DUT may or may not indicate the operating speed of the link through bits 1.0.6, 1.0.13, and 1.0.5:2.

Possible Problems: If the PHY does not maintain a default value in Register 1.0, part a cannot be performed.

Test #MDIO.1.6: 10GBASE-T Advertisement

Purpose: To verify that the 10GBASE-T AN Control Register bits 7.32.13:12 and 7.32.0 properly control the advertisement of 10GBASE-T ability, port type, and LD loop timing.

References:

[1] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.10.3 – Port Type
[2] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.10.4 – 10GBASE-T Capability
[3] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.10.7 – LD Loop Timing Ability
[4] IEEE Std 802.3, 2012 Edition, Table 45-187 – 10GBASE-T AN Control Register
[5] IEEE Std 802.3, 2012 Edition, Table 55-15 – 10GBASE-T Base and Next Pages Bit Assignments

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: In order for 10GBASE-T devices to automatically configure themselves, they must complete the exchange of a Base Page and one Extended Next Page during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MDIO Registers 7.18:16 (AN Advertisement Registers) as well as MDIO Registers 7.24:22 (AN XNP Transmit Registers). However, such an approach would require each systems management to be capable of properly following Clause 28's Extended Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 10GBASE-T PHYs also incorporate the option of having an automatic embedded Extended Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 10GBASE-T port. The system accomplishes this by writing to the 10GBASE-T AN Control Register. To specify the port type of the device, whether or not 10GBASE-T advertisement is desired, and whether or not LD loop timing is advertised, the system writes to bits 7.32.13:12 and bit 7.32.0. If an automatic embedded management entity is not present, or disabled, then the system's management entity is required to properly complete the Extended Next Page exchange by the properly timed writing of Registers 7.24:22. In such an event, it is recommended that the contents of Register 7.32 accurately reflect the abilities advertised in bits U17, U16, and U13 of the 10GBASE-T Extended Next Page.

Test Setup: See **Appendix 22.B**

Part a: 10GBASE-T Advertisement

1. Set bit 7.32.12 to 1.
2. Restart Auto-Negotiation.
3. Send a Base Page and 10GBASE-T Extended Next Page Sequence to the DUT.
4. Observe transmissions from the DUT.
5. Repeat steps 1-4 setting bit 7.32.12 to 0.

Part b: Port Type Advertisement

6. Set bit 7.32.13 to 1.
7. Send a Base Page and 10GBASE-T Extended Next Page Sequence to the DUT.
8. Observe transmissions from the DUT.
9. Repeat steps 6-8 setting bit 7.32.13 to 0.

Part c: LD Loop Timing Advertisement

10. Set bit 7.32.0 to 1.
11. Send a Base Page and 10GBASE-T Extended Next Page Sequence to the DUT.
12. Observe transmissions from the DUT.
13. Repeat steps 10-12 setting bit 7.32.0 to 0.

Observable Results:

a. Bit U16 in the 10GBASE-T Extended Next Page sent by the DUT should match the value of bit 7.32.12.
b. Bit U13 in the 10GBASE-T Extended Next Page sent by the DUT should match the value of bit 7.32.13.
c. Bit U17 in the 10GBASE-T Extended Next Page sent by the DUT should match the value of bit 7.32.0.

Possible Problems: None

Test #MDIO.1.7: 10GBASE-T AN Control Register bits 7.32.15:14

Purpose: To verify that the 10GBASE-T AN Control Register bits 7.32.15:14 properly control MASTER/SLAVE Manual Configuration.

References:

[1] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.10.1 – MASTER/SLAVE Manual Config Enable
[2] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.10.2 – MASTER/SLAVE Config Value
[3] IEEE Std 802.3, 2012 Edition, Table 45-187 – 10GBASE-T AN Control Register
[4] IEEE Std 802.3, 2012 Edition, Table 55-15 – 10GBASE-T Base and Next Pages Bit Assignments

Resource Requirements: See **Appendix 22.A**

Last Modification: March 9, 2015

Discussion: In order for 10GBASE-T devices to automatically configure themselves, they must complete the exchange of a Base Page and one Extended Next Page during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MDIO Registers 7.18:16 (AN Advertisement Registers) as well as MDIO Registers 7.24:22 (AN XNP Transmit Registers). However, such an approach would require each systems management to be capable of properly following Clause 28's Extended Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 10GBASE-T PHYs also incorporate the option of having an automatic embedded Extended Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 10GBASE-T port. The system accomplishes this by writing to the 10GBASE-T AN Control Register. To specify that the port should be forced to either MASTER or SLAVE, the system must set bit 7.32.15 to 1, and set 7.23.14 to either 1 or 0. Once set, the system can enable the port, reset the port, or restart Auto-Negotiation and the embedded Extended Next Page exchange controller will do the rest of the page exchange work. If an automatic embedded management entity is not present, or disabled, then the system's management entity is required to properly complete the Extended Next Page exchange by the properly timed writing of Registers 7.24:22. In such an event it is recommended that the contents of Register 7.32 accurately reflect the abilities advertised in bits U11 and U12 of the 10GBASE-T Extended Next Page. The default value of bits 7.32.15:14 is 0.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default Value of Bits 7.32.15:14

1. Perform an AN Reset.
2. Read bits 7.32.15:14.

Part b: MASTER/SLAVE Manual Configuration Enabled

3. Set bits 7.32.15 and 7.32.14 to 1.
4. Restart Auto-Negotiation.
5. Send a Base Page and 10GBASE-T Extended Next Page Sequence with the DUT.
6. Observe transmissions from the DUT.
7. Repeat steps 3-6 setting bit 7.32.14 to 0.

Part c: MASTER/SLAVE Manual Configuration Disabled

8. Set bits 7.32.15 and 7.32.14 to 0.
9. Restart Auto-Negotiation.
10. Send a Base Page and 10GBASE-T Extended Next Page Sequence with the DUT.
11. Observe transmissions from the DUT.
12. Repeat steps 8-11 setting bit 7.32.14 to 1.

Observable Results:

a. The default value of bits 7.32.15:14 should be 0.
b. When bit 7.32.15 is set to 1, bits U11 & U12 in the 10GBASE-T Extended Next Page transmitted by the DUT should match the value of 7.32.15:14.
c. INFORMATIVE: When bit 7.32.15 is set to zero, bits U11 & U12 in the 10GBASE-T Extended Next Page transmitted by the DUT may or may not match the value of bits 7.32.15:14.

Possible Problems: None

GROUP 2: ADVERTISEMENT REGISTERS

Scope: The following tests cover Auto-Negotiation operation specific to Advertisement Registers in the management register set.

Overview: These tests are designed to verify that the DUT properly implements Advertisement Registers within the MDIO register set as it pertains to the Auto-Negotiation function. Register functions tested are defined in Clause 45 of IEEE 802.3.

NOTE: These tests are performed for the Ethernet Consortia. These tests cannot be performed if MDIO management register access is not provided.

Test #MDIO.2.1: AN Advertisement Register

Purpose: To verify that the AN Advertisement Register (Register 7.16) can be set according to Table 45-183 and is reflected in the link codewords transmitted by the DUT.

References:

[1] IEEE Std 802.3-2012, subclause 45.2.7.6 – AN advertisement register
[2] IEEE Std 802.3-2012, Table 45-183 – AN Advertisement register bit definitions
[3] IEEE Std 802.3-2012, Annex 28A – Selector Field definitions
[4] IEEE Std 802.3-2012, Annex 28B – IEEE 802.3 Selector Base Page definition
[5] IEEE Std 802.3-2012, Annex 28D – Description of extensions to Clause 28 and associated annexes

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: The AN Advertisement Register (Register 7.16) allows the management to advertise its desired abilities to its Link Partner. After the DUT is initialized, the default value of Register 7.16 should be as follows: a Selector Field set to 00001, a Technology Ability Field set to supported abilities found in Register 1.4, and the Acknowledge bit set to 0. The Selector Field bits are all read/write, however the DUT should not allow reserved Selector Field combinations to be transmitted. The DUT must allow the IEEE 802.3 Ethernet Selector Field combination to be transmitted, and the DUT may allow other non-reserved combinations to be transmitted.

The Technology Ability Field bits are all read/write, however the DUT should not allow unsupported technologies to be written or transmitted. The DUT must allow all supported technologies to be written and transmitted.

The Remote Fault bit is read/write and should be transmitted as written.

The Next Page and Extended Next Page bits should be read/write if the DUT supports the technology. If the DUT does not support the exchange of Next Pages then bit 7.16.15 should be set to 0. If the DUT does not support the exchange of Extended Next Pages then bit 7.16.12 should be set to 0. If the DUT implements an automatic embedded management entity, similar to the mechanism described in Annex 40C, bit 7.16.15 may not directly map to the DUT's transmitted link codeword.

The Acknowledge bit is read only and should be set to 0.

The link codeword transmitted by the DUT should exactly match the value found in Register 7.16 with the exception of the Next Page bit if the DUT implements an automatic embedded management entity.

Management may write to Register 7.16 at any time, including during an Auto-Negotiation restart, so that only supported Selector Fields and technologies are advertised. This may happen in such a manner that some user values written to Register 7.16 are not observable.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default Value of Register 7.16

1. Perform a AN Reset.
2. Read Register 7.16.

Part b: Ethernet Selector Field Transmission

3. Set bits 7.16.4:0 to 00001.
4. Restart Auto-Negotiation.
5. Observe transmissions from the DUT.

Part c: Read/Write Ability of the Selector Field

6. Set bit 7.16.0 to 1.
7. Read Register 7.16.
8. Repeat steps 6 and 7, setting each bit of the Selector Field to 1.
9. Repeat steps 6 and 7, setting bit 4.0 to 0.

Part d: Transmission of Reserved Selector Field

10. Set bits 7.16.4:0 to 0.
11. Restart Auto-Negotiation.
12. Observe transmissions from the DUT.
13. Repeat steps 10-12 setting bits 7.16.4:0 to 1.

Part e: Transmission of Non-Reserved Selector Field Values

14. Set bits 7.16.4:0 to 00010.
15. Restart Auto-Negotiation.
16. Observe transmissions from the DUT.
17. Repeat steps 14-16 with the following values: 00011, 00100 and 00101.

Part f: Read/Write Ability of the Technology Ability Field and the Extended Next Page Bit

18. Set bits 7.16.12:5 to 1.
19. Read Register 7.16.
20. Repeat steps 18 and 19 setting bits 7.16.12:5 to 0.

Part g: Transmission of the Technology Ability Field and the Extended Next Page Bit

21. Set bits 7.16.12:5 to 1.
22. Restart Auto-Negotiation.
23. Observe transmissions from the DUT.
24. Repeat steps 21-23 setting bits 7.16.12:5 to 0.

Part h: Transmission of the Remote Fault Bit

25. Set bit 7.16.13 to 1.
26. Restart Auto-Negotiation.
27. Observe transmissions from the DUT.
28. Repeat steps 25-27 setting bit 7.16.13 to 0.

Part i: Read Only Status of the Acknowledge Bit

29. Set bit 7.16.14 to 1.
30. Read Register 7.16.

Part j: Read/Write Ability of the Next Page Bit

31. Set bit 7.16.15 to 1.
32. Read Register 7.16.
33. Repeat steps 31 and 32 setting bit 7.16.15 to 0.

Part k: Transmission of Link Codewords

34. Set Register 7.16 to 0xFFFF.
35. Restart Auto-Negotiation.
36. Read Register 7.16.
37. Observe transmissions from the DUT.
38. Repeat steps 34-37 setting Register 7.16 to 0x0001.

Observable Results:

a. Register 7.16 should have the following configuration:
   - The Selector field set to 00001
   - Bit 7.16.14 set to zero
   - The Technology Ability Field set to supported technologies based on Register 1.4

b. The DUT should allow IEEE 802.3 Ethernet Selector Field code value (00001) to be transmitted.
c. The DUT should allow bits 7.16.4:0 to be written.
d. The DUT should not allow reserved Selector Field codes (00000 and 11111) to be transmitted.
e. INFORMATIVE: A device may or may not allow the other defined Selector Field Codes (00010, 00011, 00100, and 00101) to be transmitted.
f. The DUT should not allow bits 7.16.12:5 to be written if the DUT does not support that technology.
g. The DUT should only allow supported abilities to be transmitted.
h. The DUT should allow the Remote Fault bit to be transmitted.
i. The DUT should not allow the Acknowledge Bit to be written.
j. The DUT should allow the Next Page bit to be written.
k. The link codewords transmitted by the DUT should exactly match Register 7.16, with the exception of the Next Page bit if the DUT implements an automatic embedded management entity.

Possible Problems: During parts a, c, and f it may not be possible to read the value of Register 7.16 before management changes the value. If management does not allow non-Ethernet defined Selector Field combinations to be written, then part e cannot be performed.

Test #MDIO.2.2: AN XNP Transmit Register

Purpose: To verify that the AN XNP Transmit Registers can be set according to Table 45-185 and is reflected in the Extended Next Pages transmitted by the DUT.

References:
[1] IEEE Std 802.3-2012, subclause 28.2.3.4 – Next Page function
[2] IEEE Std 802.3-2012, subclause 45.2.7.8 – AN XNP transmit register
[3] IEEE Std 802.3-2012, Table 45-185 – AN XNP transmit register bit definitions

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: During an Extended Next Page exchange, management must have the ability to control the contents of the pages to be transmitted. The AN XNP Transmit Register is used for this purpose. After an AN Reset, the default value of Registers 7.24:22 represents a null message page. The transmission of Extended Next Pages is often controlled by an automatic embedded management entity which may change the values of Registers 7.24:22 or directly control the transmission of Extended Next Pages. Devices that automatically control the Extended Next Page exchange may allow for the transmission of additional Extended Next Pages.

Test Setup: See **Appendix 22.B**

Procedure:
Part a: Default Value of the AN XNP Transmit Registers
1. Perform an AN Reset.
2. Read Registers 7.22, 7.23, and 7.24.

Part b: Read/Write Ability of the AN XNP Transmit Registers
3. Set Registers 7.23 and 7.24 to 0xFFFF.
4. Set Register 7.22 to 0xFFFF.
5. Read Registers 7.22, 7.23, and 7.24
6. Repeat steps 3-5 setting Registers 7.22, 7.23, and 7.24 to 0x0000.

Part c: Transmission of Extended Next Pages
7. Configure the DUT to desire a user-controlled Extended Next Page exchange.
8. Send a Base Page with the Acknowledge, Next Page, and Extended Next Page bits set to one to the DUT to put it into the COMPLETE ACKNOWLEDGE state.
9. Set Registers 7.23 and 7.24 to 0xFFFF.
10. Set Register 7.22 to 0xFFFF.
11. Read Registers 7.22, 7.23, and 7.24.
12. Observe transmissions from the DUT.
13. Restart Auto-Negotiation.

14. Repeat steps 6 through 12 setting Register 7.22, 7.23, and 7.24 to 0x0000.

Part d: Transmission of Toggle and Acknowledge Bits

15. Configure the DUT to send multiple Extended Next Pages.
16. Monitor the value of the transmitted Toggle and Acknowledge bits.

Observable Results:

a. After a device is initialized, the value of the AN XNP Transmit registers should represent a Null Message Page.
b. The DUT should allow all bits except the Toggle and Acknowledge bits to be written.
c. The Extended Next Pages transmitted by the DUT should have bits 7.15, 7.13, 7.12, and 7.10:0 set corresponding to the value in Register 7.22.
d. The Extended Next Pages transmitted by the DUT should have bit 7.22.14 set to 0, and bit 7.22.11 set to the opposite of the value of bit 7.16.11 in the initial link codeword sent by the DUT.

Possible Problems: During part a it may not be possible to read the value of Registers 7.24:22 before management changes the value. If the DUT does not allow a user-controlled Extended Next Page exchange part c cannot be performed.

Test #MDIO.2.3: Control of mr_next_page_loaded

Purpose: To verify that mr_next_page_loaded is set when the AN XNP Transmit Register is written, and cleared in the NEXT PAGE WAIT state and the TRANSMIT DISABLE state.

References:

[1] IEEE Std 802.3-2012, subclause 28.2.4.1.8 – State diagram variable to MII register mapping
[2] IEEE Std 802.3-2012, subclause 28.3.1 – State diagram variables
[3] IEEE Std 802.3-2012, subclause 45.2.7.8 – AN XNP transmit register
[4] IEEE Std 802.3-2012, Table 28-8 – State diagram variable to MII register mapping
[5] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18,2015

Discussion: The mr_next_page_loaded variable controls the transition between pages during Auto-Negotiation. The variable mr_next_page_loaded is automatically set when management writes the AN XNP Transmit Register 7.22 but not 7.23 or 7.24, but should be cleared in both the TRANSMIT DISABLE and NEXT PAGE WAIT states. The DUT should continue sending its previous page with the Acknowledge bit set until mr_next_page_loaded is set to true.

Test Setup: See **Appendix 22.A**

Procedure:

Part a: Continued Transmissions while in the COMPLETE ACKNOWLEDGE State:

1. Configure the DUT to desire a user-controlled Extended Next Page exchange.
2. Send a Base Page with the Next Page, Extended Next Page, and Acknowledge bits set to 1 to the DUT to cause it to enter the COMPLETE ACKNOWLEDGE state.
3. Observe transmissions from the DUT.

Part b: Setting mr_next_page_loaded in the COMPLETE ACKNOWLEDGE state:

4. Restart Auto-Negotiation.
5. Send a Base Page with the Next Page, Extended Next Page, and Acknowledge bits to 1 set to the DUT to cause it to enter the COMPLETE ACKNOWLEDGE state.
6. Write any value to Register 7.22 while the DUT is in the COMPLETE ACKNOWLEDGE state
7. Observe transmissions from the DUT.

Part c: mr_next_page_loaded is not Set to True when 7.23 or 7.24 are Written:

8. Restart Auto-Negotiation.
9. Send a Base Page with the Next Page, Extended Next Page, and Acknowledge bits to 1 set to the DUT to cause it to enter the COMPLETE ACKNOWLEDGE state.

10. Write any value to Register 7.23 and 7.24 while the DUT is in the COMPLETE ACKNOWLEDGE state
11. Observe transmissions from the DUT.

Part d: Setting mr_next_page_loaded to False in the NEXT PAGE WAIT State:

12. Restart Auto-Negotiation.
13. Send a Base Page with the Next Page and Acknowledge bits to 1 set to the DUT to cause it to enter the COMPLETE ACKNOWLEDGE state.
14. Write any value to Register 7.22 while the DUT is in the COMPLETE ACKNOWLEDGE state
15. Send a Next Page with the Acknowledge, Extended Next Page, and Next Page bits set to 1 to the DUT to cause it to re-enter the COMPLETE ACKNOWLEDGE state.
16. Observe transmissions from the DUT.

Observable Results:

a. The DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its Base Page with the Acknowledge bit set to 1.
b. The DUT should start transmitting its first Extended Next Page, with a proper Toggle bit value and the Acknowledge bit set to 0.
c. The DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its Base Page with the Acknowledge bit set to 1.
d. The DUT should remain the COMPLETE ACKNOWLEDGE state and continue to send its first Extended Next Page with the Acknowledge bit set to 1.

Possible Problems: If the DUT does not allow a user-controlled Extended Next Page exchange, this test cannot be performed.

GROUP 3: STATUS REGISTERS

Scope: The following tests cover Auto-Negotiation operation specific to Status Registers in the management register set.

Overview: These tests are designed to verify that the DUT properly implements the Status Registers within the MDIO register set as it pertains to the Auto-Negotiation function. Register functions tested are defined in Clause 45 and Clause 55 of IEEE 802.3.

NOTE: These tests are performed for the Ethernet Consortia. These tests cannot be performed if MDIO management register access is not provided.

Test #MDIO.3.1: Auto-Negotiation Complete

Purpose: To verify that bit 7.1.5 is properly set upon completion of Auto-Negotiation and entrance into the FLP LINK GOOD state.

References:

[1] IEEE Std 802.3-2012, subclause 28.3.1 – State diagram variables
[2] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram
[3] IEEE Std 802.3-2012, subclause 45.2.7.2.4 – Auto-Negotiation complete
[4] IEEE Std 802.3-2012, Table 45-182 – AN status register

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: Once a link has been established, management needs to be made aware that frame transmission and reception can commence. Bit 7.1.5 is set when Auto-Negotiation is complete and a link has been established.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Entrance into the FLP LINK GOOD State with Auto-Negotiation Disabled

1. Disable Auto-Negotiation.
2. Send link signaling to the DUT in order to establish a link.
3. Read bit 7.1.5.

Part b: Entrance into the FLP LINK GOOD CHECK State with Auto-Negotiation Enabled

4. Enable Auto-Negotiation.
5. Send a Base Page to the DUT so it enters the FLP LINK GOOD CHECK state.
6. Read bit 7.1.5.

Part c: Entrance into the FLP LINK GOOD State with Auto-Negotiation Enabled

7. Enable Auto-Negotiation.
8. Send a Base Page to the DUT so it enters the FLP LINK GOOD CHECK state followed by link signaling in order to establish a link.
9. Read bit 7.1.5.

Part d: Setting Bit 7.1.5 to 0 in the TRANSMIT DISABLE State

10. Repeat steps 7 and 8.
11. Break the link and allow the DUT to enter the TRANSMIT DISABLE State.
12. Read bit 7.1.5.

Part e: Establishing a Link through Parallel Detection

13. Enable Auto-Negotiation.
14. Transmit link signaling to the DUT to establish a link through Parallel Detection.
15. Read bit 7.1.5.

Observable Results:

a. When Auto-Negotiation is disabled, the value of bit 7.1.5 should never be set to one.
b. When Auto-Negotiation is enabled, the value of bit 7.1.5 should never be set to one before the DUT enters the FLP LINK GOOD state. The value of bit 7.1.5 should be zero.
c. When Auto-Negotiation is enabled, the DUT should set bit 7.1.5 once it has entered the FLP LINK GOOD state. The value of bit 7.1.5 should be one.
d. When the DUT enters the TRANSMIT DISABLE State bit 7.1.5 should be set to 0.
e. When Auto-Negotiation is enabled, the DUT should set bit 7.1.5 once it has entered the FLP LINK GOOD state. The value of bit 7.1.5 should be one.

Possible Problems: If the DUT does not allow Auto-Negotiation to be disabled, part a cannot be performed. If a link cannot be established through parallel detection, part e cannot be performed.

Test #MDIO.3.2: Link Status

Purpose: To verify that bit 7.1.2 of the Status Register is set when a link has been established.

References:

[1] IEEE Std 802.3-2012, subclause 28.3.1 – State diagram variables
[2] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram
[3] IEEE Std 802.3-2012, subclause 45.2.7.2.7 – Link status
[4] IEEE Std 802.3-2012, Table 45-182 – AN status register

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: Bit 7.1.2 of the AN Status Register indicates to management that a link has been established. When this bit is set, it indicates that the DUT has entered the FLP LINK GOOD state, regardless of whether Auto-Negotiation is enabled or disabled.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Establish a Link through Auto-Negotiation

1. Establish a link with the DUT using the Auto-Negotiation process.
2. Read bit 7.1.2.

Part b: Establish a Link through Parallel Detection

3. Restart Auto-Negotiation.
4. Send link signaling to establish link through Parallel Detection.
5. Read bit 7.1.2.

Part c: Establish a Link with Auto-Negotiation Disabled

6. Disable Auto-Negotiation.
7. Send the DUT link signaling to manually force a link.
8. Read bit 7.1.2.

Part d: Setting Bit 7.1.2 to 0

9. Establish a link with the DUT using the Auto-Negotiation process
10. Break the link with the DUT.
11. Read bit 7.1.2.

Observable Results:

a. Bit 7.1.2 should be set to 1 after entering the FLP LINK GOOD state.
b. Bit 7.1.2 should be set to 1 after entering the FLP LINK GOOD state.
c. Bit 7.1.2 should be set to 0 when Auto-Negotiation is disabled.

d. Bit 7.1.2 should be set to 0 once the link has been broken.

Possible Problems: If the device does not support 10BASE-T half duplex or 100BASE-TX half duplex, then part b cannot be performed. If Auto-Negotiation cannot be disabled, then part c cannot be performed.

Test #MDIO.3.3: Auto-Negotiation Ability

Purpose: To verify that the DUT maintains the value of one in bit 7.1.3.

References:

[1] IEEE Std 802.3-2012, Table 28-8 – State diagram variable to MII register mapping
[2] IEEE Std 802.3-2012, subclause 45.2.7.2.6 – Auto-Negotiation ability

Resource Requirements:

- None

Last Modification: March 18, 2015

Discussion: Management is made aware that an Auto-Negotiation capable PHY is attached using the AN Status Register bit 7.1.3, regardless of the management's desire to enable or disable Auto-Negotiation. It allows for a DUT with an exposed MII to discover the Auto-Negotiation ability of an attached PHY.

Test Setup: Access the DUT's Management Registers.

Procedure:

Part a: Status of Bit 7.1.3

1. Disable Auto-Negotiation.
2. Read bit 7.1.3.
3. Enable Auto-Negotiation.
4. Read bit 7.1.3.

Observable Results:

a. Bit 7.1.3 should be set to one, regardless of whether Auto-Negotiation is enabled or not.

Possible Problems: None.

Test #MDIO.3.4: Link Partner Auto-Negotiation Able

Purpose: To verify that the DUT sets bit 7.1.0 to one after detection of an Auto-Negotiation capable Link Partner.

References:

[1] IEEE Std 802.3-2012, subclause 28.3.1 – State diagram variables
[2] IEEE Std 802.3-2012, subclause 45.2.7.2.8 – Link partner Auto-Negotiation ability
[3] IEEE Std 802.3-2012, Table 28-8 – State diagram variable to MII register mapping
[4] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: A DUT's management is made aware that its Link Partner is capable of Auto-Negotiation by bit 7.1.0. When the DUT enters the ACKNOWLEDGE DETECT state, it sets bit 7.1.0 to 1. Whenever the DUT re-enters the ABILITY DETECT state bit 7.1.0 is set to 0.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Default Value of Bit 7.1.0

1. Initialize the DUT.
2. Read Bit 7.1.0.

Part b: Value Bit 7.1.0 in the ACKNOWLEDGE DETECT State

3. Send a Base Page with the Acknowledge bit set to 0 to the DUT to put it in the ACKNOWLEDGE DETECT state.
4. Read Bit 7.1.0.

Part c: Setting Bit 7.1.0 to 0

5. Repeat steps 3 and 4.
6. Cease transmissions to the DUT and wait until the DUT passes through the TRANSMIT DISABLE state.
7. Read Bit 7.1.0.

Part d: Value of Bit 7.1.0 when Receiving Alternating FLP Bursts

8. Send the DUT a constant stream of FLP Bursts alternating in content and without the Acknowledge bit set, to keep the DUT in the ABILITY DETECT state.
9. Read Bit 7.1.0.

Observable Results:

a. The default value of bit 7.1.0 should be 0.
b. The DUT should set bit 7.1.0 to 1 in the ACKNOWLEDGE DETECT state.
c. The DUT should set bit 7.1.0 to 0 in the ABILITY DETECT state.
d. When the DUT is in the ABILITY DETECT state, bit 7.1.0 should be set to 0.

Possible Problems: None.

Test #MDIO.3.5: Report PHY Capabilities

Purpose: To verify that the PHY sets bits 1.4.9:4, and 1.11.10:0 appropriately for the PHY's abilities.

References:

[1] IEEE Std 802.3-2012, subclause 45.2.1.4.1 – 100G capable
[2] IEEE Std 802.3-2012, subclause 45.2.1.4.2 – 40G capable
[3] IEEE Std 802.3-2012, subclause 45.2.1.4.3 – 10/1G capable
[4] IEEE Std 802.3-2012, subclause 45.2.1.4.4 – 10M capable
[5] IEEE Std 802.3-2012, subclause 45.2.1.4.5 – 100M capable
[6] IEEE Std 802.3-2012, subclause 45.2.1.4.6 – 1000M capable
[7] IEEE Std 802.3-2012, subclause 45.2.1.4.9 – 10G capable
[8] IEEE Std 802.3-2012, subclause 45.2.1.10 – PMA/PMD extended ability register
[9] IEEE Std 802.3-2012, Table 45-6 – PMA/PMD speed ability register bit definitions
[10] IEEE Std 802.3-2012, Table 45-13 – PMA /PMD Extended Ability register bit definitions

Resource Requirements:

- None

Last Modification: March 18, 2015

Discussion: Management is made aware that a PHY's signaling abilities using the PMA/PMD Speed Ability Register bits 1.4.9:4, 1.4.0, and the PMA/PMD Extended Ability register bits 1.11.10:0.

Test Setup: Access the DUT's Management Registers.

Part a: PHY Abilities

1. Read bits 1.4.9:4, 1.4.0, and 1.11.10:0.
2. Verify the DUT supports all indicated abilities.

Observable Results:

a. Bits 1.4.9:4, 1.4.0, and 1.11.10:0 should only be set if the DUT supports the ability.

Possible Problems: None.

Test #MDIO.3.6: Remote Fault

Purpose: To verify that the DUT sets bit 7.1.4 upon reception of a link codeword with the Remote Fault bit set.

References:

[1] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.2.5 – Remote Fault
[2] IEEE Std 802.3, 2012 Edition, subclause 28.2.3.5 – Remote Fault Sensing
[3] IEEE Std 802.3, 2012 Edition, Table 45-182 – AN Status Register

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: Bit 7.1.4 is used to indicate that a Base Page with the Remote Fault bit set has been received. Once set, this bit should remain set until after management reads the AN Status Register or until successful negotiation of a link. The default value of bit 7.1.4 is zero.

Test Setup: See **Appendix 22.B**

Part a: Default Value of Bit 7.1.4

1. Perform an AN Reset.
2. Read bit 7.1.4.

Part b: Value of 7.1.4 Prior to the FLP LINK GOOD State

3. Send a Base Page with the Remote Fault bit set to 1 to put the DUT into the COMPLETE ACKNOWLEDGE state.
4. Cease transmissions to the DUT and wait until the DUT passes through the TRANSMIT DISABLE state.
5. Read bit 7.1.4.

Part c: Setting Bit 7.1.4 to 0 After a Read

6. Repeat steps 3 and 4.
7. Read bit 7.1.4 twice.

Observable Results:

a. The default value of bit 7.1.4 is 0.
b. Bit 7.1.4 should be set to 1 once the DUT has entered the COMPLETE ACKNOWLEDGE state.
c. Bit 7.1.4 should be set to 0 after it has been read.

Possible Problems: None.

Test #MDIO.3.7: Page Received Setting/Resetting

Purpose: To verify that mr_page_rx is set when a new page is received and cleared when the Auto-Negotiation Expansion Register is read.

References:
[1] IEEE Std 802.3-2012, subclause 28.3.1 – State diagram variables
[2] IEEE Std 802.3-2012, subclause 45.2.7.2.3 – Page received
[3] IEEE Std 802.3-2012, Table 28-8 – State diagram variable to MII register mapping
[4] IEEE Std 802.3-2012, Figure 28-18 – Arbitration state diagram

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: Management is made aware of the reception of a new page by reading bit 7.1.6 in the AN Status register. If bit 7.1.6 is set, then management can look at the contents of the received page and act accordingly. Bit 7.1.6 should be reset after a read to the AN Status Register.

Test Setup: See **Appendix 22.B**

Procedure:
Part a: Value of Bit 7.1.6 in the ACKNOWLEDGE DETECT State
1. Send a Base Page with the Acknowledge bit set to zero to the DUT to put it into the ACKNOWLEDGE DETECT state.
2. Read Bit 7.1.6.

Part b: Value of Bit 7.1.6 in the COMPLETE ACKNOWLEDGE State
3. Send a Base Page with the Acknowledge bit set to one to the DUT put it into the COMPLETE ACKNOWLEDGE state.
4. Read Bit 7.1.6.

Part c: Value of Bit 6.1 with Extended Next Pages
5. Send a Base Page with the Next Page and Extended Next Page bits set to one to the DUT to put it into the COMPLETE ACKNOWLEDGE state.
6. Read bit 7.1.6 while the DUT is in the COMPLETE ACKNOWLEDGE state.
7. While the DUT is in the COMPLETE ACKNOWLEDGE state, send an Extended Next Page with Acknowledge bit set to zero to the DUT to cause it to re-enter the ACKNOWLEDGE DETECT state.
8. Read bit 7.1.6 while the DUT is in the ACKNOWLEDGE DETECT state.
9. While the DUT is in the ACKNOWLEDGE DETECT state, send a page identical to the ones sent in step 7 with the Acknowledge bit set to put the DUT into the COMPLETE ACKNOWLEDGE state again.
10. Read Bit 7.1.6.

Part d: Setting Bit 7.1.6 to 0

11. Repeat step 3.
12. Read Bit 7.1.6 twice.

Observable Results:

a. Bit 7.1.6 should never be set in the ACKNOWLEDGE DETECT state.
b. Bit 7.1.6 should be set to 1 in the COMPLETE ACKNOWLEDGE state.
c. Bit 7.1.6 should be set to 1 in the COMPLETE ACKNOWLEDGE state and set to 0 in the ACKNOWLEDGE DETECT state.
d. Bit 7.1.6 should be set to 1 in the COMPLETE ACKNOWLEDGE state and set to 0 after Register 7.1 has been read.

Possible Problems: None

Test #MDIO.3.8: Extended Next Page Status

Purpose: To verify that the DUT sets bit 7.1.7 (Extended Next Page Status) to indicate both the device and its link partner support an Extended Next Page exchange.

References:

[4] IEEE Std 802.3, 2012 Edition, subclause 28.2.1.2.3 – Extended Next Page
[5] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.1.2 – Extended Next Page control
[6] IEEE Std 802.3, 2012 Edition, subclause 45.2.7.2.2 – Extended Next Page status
[7] IEEE Std 802.3, 2012 Edition, Table 45-182 – AN Status Register

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: Bit 7.1.7 is used to indicate to the management that both the device and its link partner support an Extended Next Page exchange. If either bit 7.0.13 or 7.16.12 is set to zero, this bit should never be set to one.

Test Setup: See **Appendix 22.B**

Part a: Value of bit 7.1.7 when Both Link Partner Support an Extended Next Page Exchange

1. Configure the DUT to desire an Extended Next Page exchange.
2. Send a Base Page with the Extended Next Page bit set 1 to the DUT.
3. Read bit 7.1.7.

Part b: Value of Bit 7.1.7 when only the DUT or Link Partner Supports an Extended Next Page Exchange

4. Repeat steps 1-3 configuring the DUT to not desire an Extended Next Page exchange.
5. Repeat steps 1-3 sending a Base Page with the Extended Next Page bit set to 0 to the DUT.

Observable Results:

a. Bit 7.1.7 should be set to 1 when both the DUT and its link partner desire an Extended Next Page exchange.
b. Bit 7.1.7 should be set to 0 when only the DUT or its link partner desire an Extended Next Page exchange.

Possible Problems: None.

Test #MDIO.3.9: 10GBASE-T AN Status Register

Purpose: To verify that the 10GBASE-T AN Status Register conforms to the definition in Table 45-188.

References:

[1] IEEE Std 802.3-2012, subclause 45.2.7.11 – 10GBASE-T AN status register
[2] IEEE Std 802.3, 2012 Edition, Table 45-188 – 10GBASE-T AN status register
[3] IEEE Std 802.3, 2012 Edition, Table 55-15 – 10GBASE-T Base and Next Pages Bit Assignments

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: Once a 10GBASE-T device completes Auto-Negotiation, status information specific to the 10GBASE-T link must be properly represented in the 10GBASE-T AN Status Register.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Read/Write Ability

1. Read Register 7.33.
2. Set Register 7.33 to 0xFFFF.
3. Read Register 7.33.
4. Set Register 7.33 to 0x0000.
5. Read Register 7.33.

Part b: Value of Bit 7.33.11

6. Send a Base Page and 10GBASE-T Extended Next Page Sequence, advertising 10GBASE-T support, to the DUT.
7. Read bit 7.33.11.
8. Repeat steps 6 and 7, without advertising 10GBASE-T abilities.

Part c: Value of Bit 7.33.10

9. Send a Base Page and 10GBASE-T Extended Next Page Sequence, advertising LD Loop Timing support, to the DUT.
10. Read bit 7.33.10.
11. Repeat steps 9 and 10, without advertising 10GBASE-T abilities.

Part d: Value of Bit 7.33.14

12. Send a Base Page and a 10GBASE-T Extended Next Page Sequence to the DUT so that the DUT will resolve to MASTER.
13. Read bit 7.33.14.

14. Repeat steps 12 and 13, changing the Extended Next Page Sequence so that the DUT should resolve to SLAVE.

Part e: MASTER/SLAVE Configuration Fault with Manual Configuration

15. Configure the DUT to be manual_MASTER.
16. Send a Base Page and 10GBASE-T Extended Next Page Sequence, advertising manual_MASTER to the DUT.
17. Read bit 7.33.15.
18. Repeat steps 15-17 configuring the DUT and the Link Partner to be manual_SLAVE.

Part f: MASTER/SLAVE Configuration Fault with LD Loop Timing

19. Configure the DUT to advertise manual_MASTER and LD Loop timing.
20. Send a Base Page and 10GBASE-T Extended Next Page Sequence, advertising manual_SLAVE to the DUT.
21. Read bit 7.33.15.
22. Configure the DUT to advertise manual_SLAVE.
23. Send a Base Page and 10GBASE-T Extended Next Page Sequence, advertising manual_MASTER and LD Loop timing to the DUT.
24. Read bit 7.33.15.

Part g: MASTER/SLAVE Configuration Fault with Seed Values

25. Configure the DUT to be neither manual_MASTER nor manual_SLAVE.
26. Send a Base Page and 10GBASE-T Extended Next Page Sequence to the DUT, transmitting the same value for bit U10:0 that the DUT transmits.
27. Repeat steps 17 and 18 six more times.
28. Read bit 7.33.15.

Part h: Setting Bit 7.33.15 to 0 when Read

29. Configure the DUT to be manual_MASTER.
30. Send a Base Page and 10GBASE-T Extended Next Page sequence advertising manual_MASTER to the DUT.
31. Read bit 7.33.15 twice.

Part i: Self-Clearing Function of Bit 7.33.15 after Auto-Negotiation has been Restarted

32. Repeat steps 15 and 16.
33. Restart Auto-Negotiation.
34. Read bit 7.33.15.

Part j: Value of Bits 7.33.13:12

35. Establish a 10GBASE-T link with the DUT.
36. Read bits 7.33.13 and 7.33.12

Observable Results:

a. The DUT should not allow Register 7.33 to be written.

b. The reported Link Partner 10GBASE-T ability should match the ability indicated in the received 10GBASE-T Extended Next Page.
c. The reported Link Partner LD Loop timing ability should match the ability indicated in the received 10GBASE-T Extended Next Page.
d. Bit 7.33.14 should be set to one when the DUT resolves to MASTER. Bit 7.33.14 should be set to 0 when the DUT resolves to SLAVE.
e. Bit 7.33.15 should be set to one when a configuration fault occurs.
f. Bit 7.33.15 should be set to one when a configuration fault occurs.
g. After 7 failed attempts, the DUT should set bit 7.33.15.
h. Bit 7.33.15 should be set to 0 after Register 7.33 has been read.
i. After Auto-Negotiation has been restarted, bits 7.33.15 should be set to 0.
j. Once a link is established, bits 7.33.13 and 7.33.12 should both be set to 1.

Possible Problems: None.

GROUP 4: Link Partner Advertisement Registers

Scope: The following tests cover Auto-Negotiation operation specific to Link Partner advertisement registers in the management register set.

Overview: These tests are designed to verify that the device under test properly implements the Management Data Input Output (MDIO) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 45 of IEEE 802.3.

NOTE: These tests are performed for the Ethernet Consortia. These tests cannot be performed if MDIO management register access is not provided.

Test #MDIO.4.1: AN Link Partner Ability Register

Purpose: To verify that the AN LP Base Page Ability Register is set based on the link codewords received by the DUT.

References:

[1] IEEE Std 802.3-2012, subclause 28.2.1.2 – Link codeword encoding
[2] IEEE Std 802.3-2012, subclause 45.2.7.7 – AN LP Base Page ability register
[3] IEEE Std 802.3-2012, Table 45-184 – AN LP Base Page ability register bit definitions
[4] IEEE Std 802.3-2012, Table 28-8 – State diagram variable to MII register mapping
[5] IEEE Std 802.3-2012, Annex 28A – Selector Field definitions
[6] IEEE Std 802.3-2012, Annex 28B – 802.3 Selector Base Page definition
[7] IEEE Std 802.3-2012, Annex 28D – Description of extensions to Clause 28 and associated annexes

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: For a device to resolve a proper link configuration, it must accurately receive its Link Partner's abilities and relay them to management. Register 7.19 of the MDIO interface is defined to contain these abilities. The contents of this register are not guaranteed to be valid until the DUT enters the COMPLETE ACKNOWLEDGE state.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Storage of Received Link Codewords

1. Send a Base Page advertising 41E1 to the DUT so it enters the COMPLETE ACKNOWLEDGE state.
2. Read Register 7.19.
3. Repeat steps 1 and 2 sending Base Pages advertising (but not limited to) FFFF and 4101.

Part b: Read Only Status of Register 7.19

4. Read Register 7.19.
5. Set Register 7.19 to 0xFFFF.
6. Read Register 7.19.

Observable Results:

a. The value of Register 7.19 should exactly match the received link codewords once the DUT has set bit 7.1.6 in the COMPLETE ACKNOWLEDGE State.
b. The DUT should not allow Register 7.19 to be written.

Possible Problems: None

Test #MDIO.4.2: AN LP XNP Ability Register

Purpose: To verify that the DUT properly stores received Extended Next Pages in the AN LP XNP ability registers (7.25, 7.26, and 7.27).

References:

[1] IEEE Std 802.3-2012, subclause 28.2.3.4 – Next Page function
[2] IEEE Std 802.3-2012, subclause 45.2.7.9 – AN LP XNP ability register
[3] IEEE Std 802.3-2012, Table 45-186 – AN LP XNP ability register bit definitions

Resource Requirements: See **Appendix 22.A**

Last Modification: March 18, 2015

Discussion: For a device to resolve a proper link configuration, it must accurately receive its Link Partner's Extended Next Page abilities and relate them to management. The AN LP XNP ability registers are defined to contain these abilities and are read only.

Test Setup: See **Appendix 22.B**

Procedure:

Part a: Read Only Status of the AN LP XNP Ability Registers

1. Set registers 7.25, 7.26, and 7.27 to 0xFFFF.
2. Read registers 7.25, 7.26, and 7.27.

Part b: Storage of Received Extended Next Pages

3. Send a Base Page with the Next Page, Extended Next Page, and Acknowledge bits set to one to the DUT so it enters the COMPLETE ACKNOWLEDGE state, followed by an Extended Next Page with a value of 0xFFFF-FFFF-FFFF.
4. Read registers 7.25, 7.26, and 7.27.
5. Repeat steps 3 and 4 with Extended Next Pages containing the following values 0x6001-0000-0000, 0x4000-0000-0000, and 0x6801-0000-0000.

Observable Results:

a. The DUT should not allow registers 7.25, 7.26, and 7.27 to be written.
b. The DUT should store the Extended Next Pages exactly as received from its Link Partner.

Possible Problems: If the DUT does not support an Extended Next Page exchange, then this test cannot be performed.

Appendices

Scope: Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Overview: Test suite appendices are intended to provide additional low-level technical details pertinent to specific tests in this test suite. These appendices are outside the scope of the standard and are specific to the methodologies used for performing the measurements in this test suite.

Appendix A - Resource Requirements

Purpose: To specify the necessary resources to complete the testing in this test suite

Last Modification: March 18, 2015

Discussion:

The reader will need the following in order to perform testing.

1. Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
2. Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs), fast link pulses (FLPs) and link signaling appropriate to the PHY abilities of the DUT.

Appendix B - Test Setup

Purpose: To specify the test setup used to complete the testing in this test suite

Last Modification: March 18, 2015

Discussion:

The reader will need the following setup to perform the testing in this test suite

1. Using appropriate category cabling patch cords, connect the DUT and the Traffic Generator to the Line Monitor such that the DUT's receiver will see the traffic generator's signaling. Terminate the DUT's transmit channel with a 100Ω line termination.