UNH IOL 10 GIGABIT ETHERNET CONSORTIUM

SFF-8431 SFP+ Module Conformance Test Suite
Version 1.1

Technical Document

Last Updated: March 6, 2018

10 Gigabit Ethernet Consortium

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MODIFICATION RECORD

August 21, 2013 Version 0.1

Christopher Bridges: Initial preliminary draft.

April 8, 2014 Version 0.1

Michael Klempa: Major edits.

May 19, 2014 Version 1.0

Michael Klempa: Initial version

March 6, 2018 Version 1.1

Paul Willis: Add Linear Module Receiver requirements. Clarify Limiting Module Receiver requirements name.

ACKNOWLEDGMENTS

The University of New Hampshire would like to acknowledge the efforts of the following individuals in the development of this test suite:

Christopher Bridges	UNH InterOperability Laboratory
Michael Klempa	UNH InterOperability Laboratory
AJ McQuade	UNH InterOperability Laboratory
Jeff Lapak	UNH InterOperability Laboratory
Curtis Donahue	UNH InterOperability Laboratory
Paul Willis	UNH InterOperability Laboratory

INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the standards conformance of SFP+ modules to the SFF-8431 Standard.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent test

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross-references to the SFF-8431 standards and other documentation that might be helpful in understanding and evaluating the test and results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the configuration of the test environment. Small changes in the configuration should not be included here, but rather included in the procedure section below.

Procedure

The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

The observable results section lists observations that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

GROUP 1: ELECTRICAL SIGNALING REQUIREMENTS

Overview:

The tests defined in this section verify the electrical signaling characteristics of the SFP+ modules defined in Chapter 3 of SFF-8431.

Test 1.1 – Output AC Common-Mode Voltage

Purpose: To verify that the AC common-mode voltage is within the conformance limits

References:

[1] SFF-8431 Rev. 4.1 Table 18 – Module Receiver Output Electrical Specifications at C'
[2] SFF-8431 Rev. 4.1 Appendix D.15 – AC Common Mode Voltage
[3] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ modules. This specification includes conformance requirements for the maximum Output AC Common-Mode Voltage defined in [2].

In this test, the differential amplitude is measured while the DUT is connected to the DSO. The common mode voltage can be found by averaging the signal+ and signal- at any time. RMS AC common-mode voltage may be calculated by applying the histogram function over 1 UI to the common mode signal.

Test Setup: See Appendix I

Test Procedure:

1. Configure the BERT to send test pattern 3 (PRBS31).
2. Connect the DUT's transmitter to the DSO.
3. Measure the common mode amplitude.
4. Apply a histogram function over 1 UI of the signal.

Observable Results:

a. The maximum output AC common-mode voltage should be no more than 7.5 mV RMS

Possible Problems: None.

Test 1.2 – Output Rise and Fall Times

Purpose: To verify that the output rise and fall times are within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 19 – Limiting Module Receiver Output Jitter and Eye Mask Specifications at C'

[2] SFF-8431 Rev. 4.1 Appendix D.6 – Rise and Fall Times

Resource Requirements: See Appendix I

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ modules. This specification includes conformance requirements for the rising and falling edge transition times defined in [2].

For the purpose of this testing the rise and fall times are defined as the time between the 20% and 80% or 80% and 20% times respectively of isolated edges. The rise/fall time measurements are observed through a 12GHz low pass filter response. For optical signals, the rise and fall times may be defined either without a filter response or through the standard 7.5 GHz Bessel-Thomson response; one or the other option is specified in each case.

Test Setup: See Appendix I

Procedure:

1. Configure the pattern generator to transmit an eight ones eight zeroes pattern.
2. Capture the rise time and fall times between the 20% and 80% values.

Observable Results:

a. The rising and falling edge transition times should be greater than or equal to 28ps.

Possible Problems: None.

Group 2: IMPEDANCE REQUIREMENTS

Overview:

The tests defined in this section verify the impedance characteristics of the SFP+ modules defined in Chapter 3 of SFF-8431.

Test 2.1 – Termination Mismatch

Purpose: To verify that the termination mismatch is within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 18 – Module Receiver Output Electrical Specifications at C'

[2] SFF-8431 Rev. 4.1 Appendix D.16 – Termination Mismatch

Resource Requirements: See Appendix II

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ modules. This specification includes conformance requirements for termination mismatch defined in [2].

For the purpose of this test, the termination mismatch is defined as the percentage difference between the two low-frequency impedances to common of a differential electrical port.

$$\Delta Z_m = 2 * \frac{Z_p - Z_n}{Z_p - Z_n} * 100$$

Test Setup: See Appendix II

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing low frequency signal.
3. Connect the DUT's positive transmitter to the VNA.
4. Observe the Impedance for the positive channel.
5. Repeat steps 3 and 4 for the negative channel.
6. Using the values from the positive and negative impedances compute the termination mismatch.

Observable Results:

a. The termination mismatch at 1MHz should not exceed 5%.

Possible Problems: None.

Test 2.2 – Differential Output/Input Return Loss

Purpose: To verify the differential output and input return loss are within conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 16 – Module Transmitter Input Electrical Specifications at B'
[2] SFF-8431 Rev. 4.1 Table 18 – Module Receiver Output Electrical Specifications at C'

Resource Requirements: See Appendix II

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ modules. This specification includes conformance requirements for the differential output/input return loss.

For frequencies from 10 MHz to 11.1 GHz, both the differential input and output return loss of the driver should not exceed the limit given in the equation below:

$$\begin{Bmatrix} -12 + 2\sqrt{f} & 0.01 \le f < 4.1GHz \\ -6.3 + 13log_{10}\left(\frac{f}{5.5}\right) & 4.1GHz < f \le 11.1GHz \end{Bmatrix} (dB)$$

Test Setup: See Appendix II

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's transmitter to the VNA.
3. Measure the differential output/input return loss at the DUT transmitter from 10 MHz to 11.1 GHz.

Observable Results:

a. The differential input return loss should exceed the limits described by [1].
b. The differential output return loss should exceed the limits described by [2].

Possible Problems: None.

Test 2.3 – Reflected Input Differential to Common Mode Conversion

Purpose: To verify the reflected differential to common mode conversion is within conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 16 – Module Transmitter Input Electrical Specifications at B'

Resource Requirements: See Appendix II.

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ modules. This specification includes conformance requirements for the reflected differential to common mode conversion.

For frequencies from 10 MHz to 11.1 GHz, both the reflected differential to common mode conversion of the receiver should not exceed the limit given in the equation below:

$$\{-10 \qquad 0.01 \leq f < 11.1GHz\} \ (dB)$$

Test Setup: See Appendix II

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's receiver to the VNA.
3. Measure the reflection coefficient at the DUT receiver from 10 MHz to 11.1 GHz.
4. Compute the mode conversion from the reflection coefficient values.

Observable Results:

a. Differential to common mode return loss should exceed the limit line as specified in [1].

Possible Problems: None.

Test 2.4 – Common Mode Output Reflection Coefficient

Purpose: To verify the common mode output reflection coefficient is within conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 18 – Module Receiver Output Electrical Specifications at C'

Resource Requirements: See Appendix II.

Last Modification: April 8, 2014

Discussion:

Reference [1] specifies the receiver characteristics for SFP+ modules. This specification includes conformance requirements for the common mode output reflection coefficient.

For frequencies from 10 MHz to 11.1 GHz, both the reflected differential to common mode conversion of the transmitter should not exceed the limit given in the equation below:

$$\begin{Bmatrix} -7 + 1.6 * f & 0.01 \leq f < 2.5GHz \\ -3 & 2.5 \leq f < 11.1GHz \end{Bmatrix} \ (dB)$$

Test Setup: See Appendix II.

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's transmitter to the VNA.
3. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
4. Compute the common mode return loss from the reflection coefficient values.

Observable Results:

a. The common mode return loss should exceed the limit line as specified in [1].

Possible Problems: None.

Group 3: LIMITING MODULE REQUIREMENTS

Overview:

The tests defined in this section verify the characteristics of the SFP+ limiting modules defined in Chapter 3 of SFF-8431.

Test 3.1 – Receiver Bit Error Rate Test for Limiting Modules

Purpose: To verify the TJ and J2 values as well as the eye-mask failure probability.

References:

[1] SFF-8431 Rev. 4.1 Table 19 – Limiting Module Receiver Output Jitter and Eye Mask Specifications at C'
[2] SFF-8431 Rev. 4.1 Appendix D.5 – 99% Jitter (J2) and Total Jitter (TJ)
[3] SFF-8431 Rev. 4.1 Appendix D.2 – Eye Mask Compliance
[4] SFF-8431 Rev. 4.1 Appendix D.12 – Limiting Module Receiver Compliance Test
[5] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition
[6] SFF-8431 Rev. 4.1 Table 17 – Module Transmitter Input Tolerance Signal Calibrated at B"

Resource Requirements: See Appendix V

Last Modification: March 6, 2018

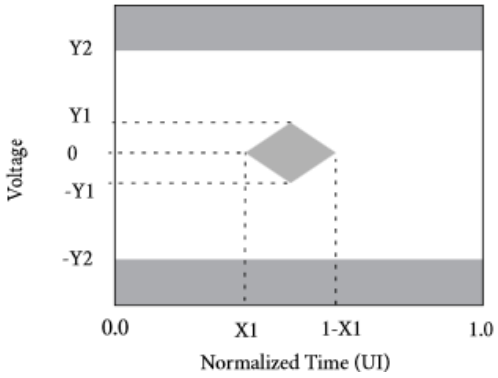
Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ modules. This specification includes conformance requirements for the peak-to-peak transmit jitter defined in [2] as well as eye mask hit ratio defined in [3]. Reference [4] specifies the crosstalk characteristics required for this test.

J2 or 99% jitter is defined as the jitter that lies between the 0.5 and 99.5 percentile of the jitter distribution in a histogram. Total jitter is defined as the sum of the deterministic jitter and random jitter multiplied by some constant based on the desired bit error rate (BER).

Reference [4] specifies the conformance requirements for the receiver tolerance. A major problem for multi-channel transceivers is interference. The interfering signal can come from a variety of sources including: a) Crosstalk from other data channels running the same kind of signals as the channel of interest. This type of interference is usually subdivided into: 1) Far-end crosstalk (FEXT) coming from data traveling in the same general direction as the channel of interest. 2) Near-end crosstalk (NEXT) originating from a channel with a transmitter near the receiver of the channel of interest. b) Self interference caused by reflections due to impedance discontinuities, stubs, etc. This is a form of intersymbol interference (ISI) that is beyond what a reasonable equalizer can compensate. c) Alien crosstalk which is defined to be interference from unrelated sources such as clocks, other kinds of data, power supply noise, etc. For the channel to work, the receiver must be able to extract correct data from the lossy channel in the presences of interference. The ability of the receiver to extract data in the presence of interference is an important characteristic of the receiver and needs to be measured. This ability is called interference tolerance.

In this test, BER is measured while the DUT is subjected to a compliant input signal with interference as specified in [4] and [6]. The jitter tolerance test setup in Figure 50 or its equivalent shall meet the receiver eye mask defined in [1]. Random jitter is added to the test signal using an interference generator which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask defined in [3]. The compliance test pattern will be used. For this test, the maximum allowable hit ratio is 10^{-12}. The failure probability for the eye masks or eye mask hit ratio is defined as the rate at which the signal will cross the eye mask.



X1=0.35 UI Y1=150 mV Y2=425 mV

Test Setup: See Appendix I

Procedure:

1. Set the BERT to transmit test pattern 3 (PRBS31) which meets the requirements of [6] for the sensitivity vertical eye parameter condition.
2. Use the DSO to find TJ and J2.
3. Use the DSO to capture the eye diagram
4. Repeat this test for the overload vertical eye parameter condition.

Observable Results:

a. The Total Jitter should not exceed 0.70 UI(p-p) for both conditions
b. The J2 should not exceed 0.42 UI(p-p) for both conditions
c. The eye mask hit ratio should not exceed 10^{-12} for both conditions

Possible Problems: None.

Group 4: LINEAR MODULE REQUIREMENTS

Overview:

The tests defined in this section verify the characteristics of the SFP+ linear modules defined in Chapter 3 of SFF-8431.

Test 4.1 – Difference Waveform Distortion Penalty

Purpose: To verify the waveform distortion penalty (dWDP).

References:

[1] SFF-8431 Rev. 4.1 Table 20 – Linear Module Receiver Specifications at C'
[2] SFF-8431 Rev. 4.1 Appendix D.14 – Linear Module Compliance Tests
[3] SFF-8431 Rev. 4.1 Appendix D.9 – Waveform Distortion Penalty
[4] IEEE Std. 802.3-2012, subclause 68.6.1 – Test-Pattern Definition

Resource Requirements: See Appendix III

Last Modification: September 19, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ modules. This specification includes conformance requirements for the maximum dWDP defined in [2] and [3].

WDP is the simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device. WDP is a waveshape metric for waveform filtering and/or nonlinear distortion. Conceptually the WDP measurement is an example of what the DUT's transmitted signaling would 'look like' to a receiver device, after passing through an interconnect (i.e., channel, backplane, cable, etc), and being received and processed by an equalizer circuit inside the receiver device.

Because it is not typically possible to observe the signal at this point (as it is conceptually located inside the actual receiver IC, post-equalization) it is not possible to practically measure this signal, however it can be mathematically computed, based on a reference model of an interconnect, and a reference receive equalizer. This mathematical modeling is performed by a set of MATLAB code that is included as part of the Standard [3].

For this test the dWDP is defined as:

$$dWDP = WDP_o - WDP_i$$

Where WDP_i is the signal of a compliance waveform generator measured at the output of a mated module compliance (MCB) board and host compliance board (HCB). WDP_o is the signal measured at the output of the module (DUT).

It is important to carefully calibrate the input compliance signal. The target WDP_i can be achieved by adjusting DDJ and/or DDPWS through use of a pre-emphasis generator and through a fourth order Bessel Thomson filter as defined in [2].

Test Setup: See Appendix III

Procedure:

1. Configure the compliance signal generator to send a PRBS9 test pattern and such that it meets the target requirements found in [1].
2. Connect the host compliance board to the module compliance board and measure WDP_i
3. Connect the DUT between the MCBs and measure WDP_o
4. Calculate dWDP

Observable Results:

a. dWDP should fall below 2.7dB for SR and LR modules.
b. dWDP should fall below 1.5 dB for LRM modules.

Possible Problems: None.

Test 4.2 – Voltage Modulation Amplitude

Purpose: To verify the voltage modulation amplitude (VMA).

References:

[1] SFF-8431 Rev. 4.1 Table 20 – Linear Module Receiver Specifications at C'
[2] SFF-8431 Rev. 4.1 Appendix D.7 – Voltage Modulation Amplitude (VMA)

Resource Requirements: See Appendix I

Last Modification: September 19, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for linear SFP+ devices. This specification includes conformance requirements for the VMA defined in [2].

For the purpose of this test, VMA is defined as the difference between the nominal one and zero levels of an electrical signal.

Test Setup: See Appendix I

Procedure:

1. Set the BERT to transmit an eight ones eight zeroes pattern.
2. Use the DSO to find the value of a time interval 8 UI long centered on the average level of the high and low section of the resulting square wave.
3. Measure the average voltage level in the central 20% of each of these time intervals.
4. Find the VMA by taking the difference of these two levels.

Observable Results:

a. The VMA should fall between 150 and 600mV for SR and LR modules.
b. The VMA should fall between 180 and 600mV for LRM modules.

Possible Problems: None.

Test 4.3 – Relative Noise

Purpose: To verify the relative noise (RN).

References:

[1] SFF-8431 Rev. 4.1 Table 20 – Linear Module Receiver Specifications at C'
[2] SFF-8431 Rev. 4.1 Appendix D.14 – Linear Module Compliance Tests
[3] SFF-8431 Rev. 4.1 Appendix D.8 – Relative Noise (RN)
[4] SFF-8431 Rev. 4.1 Table 31 – Target RN_i Values

Resource Requirements: See Appendix IV

Last Modification: September 19, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for linear SFP+ devices. This specification includes conformance requirements for the RN defined in [2]. Reference [3] defines relative noise for the purpose of this test.

For this test, the RN is found by the equation:

$$RN = \sqrt{RN_{measured}^2 - 1.24 * RN_i(target) * \left(RN_i - RN_i(target)\right)} \qquad (1)$$

[2] defines $RN_{measured}$ as the effect of TP3 tester noise at the module output. RN_i is defined as the actual TP3 tester noise. RN_i(target) is the target tester noise defined in table 31 in [2].

[1] defines the upper limit of the RN by the equation:

$$RN \leq \min[(m1 * dWDP + b1), (mw * dWDP + b2), RNmax] \qquad (2)$$

Where dWDP is the value found in test #3.1. m1, b1, m2, b2, and RNmax are defined in [1].

Test Setup: See Appendix IV

Procedure:

1. Configure the TP3 tester to the eight ones eight zeroes pattern and the RN_i to the appropriate level as defined in reference [4]
2. Connect the TP3 tester to the DUT
3. Connect the DUT to the MCB which is connected to the DSO
4. Use [3] to measure $RN_{measured}$ and RN_i.
5. Calculate RN.

Observable Results:

a. The RN should be less than 0.078 for SR modules.
b. The RN should be less than 0.083 for LR modules.
c. The RN should be less than 0.0475 for LRM modules under all pre/post cursor conditions.

Possible Problems: None.

Test 4.4 – Differential Peak to Peak Voltage

Purpose: To verify the differential peak to peak voltage.

References:

[1] SFF-8431 Rev. 4.1 Table 20 – Linear Module Receiver Specifications at C'
[2] SFF-8431 Rev. 4.1 Appendix D.14 – Linear Module Compliance Tests

Resource Requirements:

- TP3 Tester
- SFP+ Module Compliance Board
- DSO

Last Modification: September 19, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for linear SFP+ devices. This specification includes conformance requirements for the differential peak to peak voltage defined in [2].

For the purpose of this test the differential peak to peak voltage is defined as the difference between the minimum and maximum value of the differential output of the DUT taken with a measurement bandwidth of 12GHz.

Test Setup:

1. Connect the TP3 tester to the module receiver input.
2. Connect the module to the MCB.
3. Connect the output of the MCB to the DSO.

Procedure:

1. Set the TP3 tester to transmit an eight ones eight zeroes test pattern with a rise/fall time of 47ps 20-80% with no overshoot or ripple when observed though an O/E converter.
2. Use the DSO to find the minimum and maximum differential voltage levels at the output of the MCB.

Observable Results:

a. The differential peak to peak voltage should not exceed 600mV

Possible Problems: None.

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Appendix I – Setup for Electrical signaling measurements

Purpose: To specify the setup for electrical based tests in this test suite.

References:

[1] SFF-8431 Rev. 4.1 Subclause 3.6.1 - Module Input Electrical Specifications at B' and B"
[2] SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C'

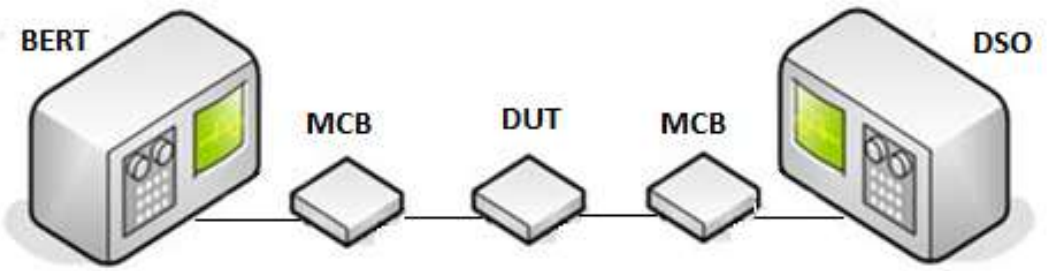
Resource Requirements:

- DSO
- BERT
- De-emphasis Signal Converter
- Two SFP+ Module Compliance Boards

Last Modification: August 21, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The BERT is setup to transmit a valid signal and jittered clock into the emphasis signal converter. The output of the de-emphasis signal converter is attached to the TX lane of the SFP+ module compliance board (MCB). The RX lane of the second MCB is attached to the DSO positive and negative inputs.

The BERT and De-emphasis signal converter should be configured so that the jitter values as read by the DSO are in reference [2].

Appendix II – Setup for VNA measurements

Purpose: To specify the setup for VNA based tests in this test suite.

References:

[1] SFF-8431 Rev. 4.1 Table 17 – Module Input Electrical Specifications at B' and B"

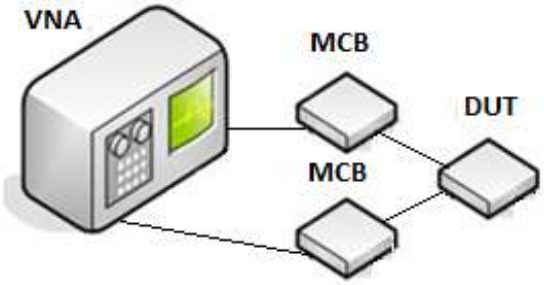
Resource Requirements:

- Vector Network Analyzer
- Two SFP+ Module Compliance Boards

Last Modification: August 21, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The VNA is setup so that channels 1 and 2 are connected to the RX side of one card while channels 3 and 4 are attached to the TX side on the other card.

The VNA should be properly calibrated before use.

Appendix III – Difference Waveform Distortion Penalty Test Setup

Purpose: To specify the setup and calibration of the TP3 tester and DSO used in this test suite.

References:

[1] SFF-8431 Rev. 4.1 Appendix D.14 – Linear Module Compliance Tests

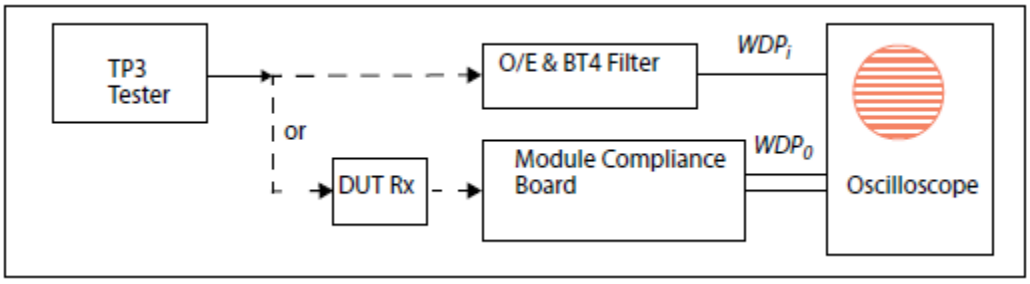
Resource Requirements:

- TP3 Tester
- SFP+ Module Compliance Boards
- DSO

Last Modification: September 19, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



To measure WDP_i, the TP3 tester is connected to the DSO through an optical to electrical converter and a fourth order Bessel-Thomson filter. To measure WDP_o, the TP3 tester is connected to the receive end of the DUT which is then connected to the DSO through a MCB.

Appendix IV – Relative Noise Test Setup

Purpose: To specify the setup and calibration of the TP3 tester and DSO used in this test suite.

References:

[1] SFF-8431 Rev. 4.1 Appendix D.14 – Linear Module Compliance Tests

[2] SFF-8431 Rev. 4.1 Table 18 – Module Receiver Output Electrical Specifications at C'

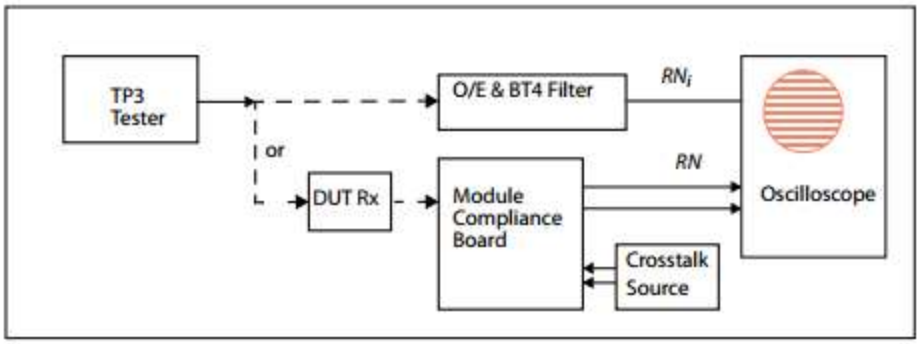
Resource Requirements:

- TP3 Tester
- Two SFP+ Module Compliance Boards
- DSO
- Crosstalk Source

Last Modification: September 19, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The Crosstalk source should be set to transmit a valid PRBS31 test pattern with a rise/fall time (20-80%) of 34ps and a p-p amplitude of 700mV. The TP3 tester should be configured to transmit an eight ones eight zeroes test pattern with waveform shaping enabled and jitter disabled.

Appendix V – Setup for receiver tests

References:

[1] SFF-8431 Rev. 4.1 Subclause 3.3.2 – Module Compliance Points
[2] SFF-8431 Rev. 4.1 Table 16 – Module Transmitter Input Electrical Specifications at B'
[3] SFF-8431 Rev. 4.1 Table 17 – Module Transmitter Input Tolerance Signal Calibrated at B"
[4] SFF-8431 Rev. 4.1 Table 35 – 10GSFP+ Host receiver input stress Generator at C"

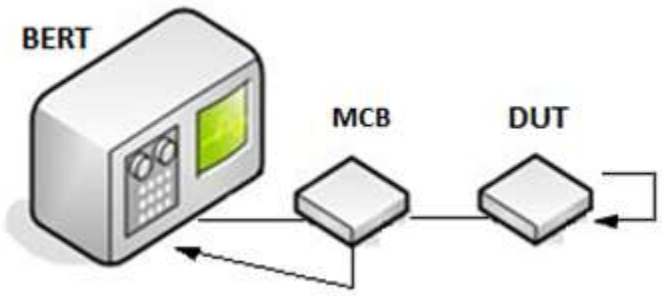
Resource Requirements:

- DSO
- BERT
- De-emphasis Signal Converter
- SFP+ Module Compliance Boards

Last Modification: September 23, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The BERT sends traffic through the de-emphasis signal converter to the DUT connected to a SFP+ host compliance board. This traffic is then looped back through the host compliance board into a DSO. The test setup should be configured to create the following stress values:

For test 3.1 use reference [2] to calibrate the crosstalk source. For test 3.2 use reference [3] to calibrate the crosstalk source. For devices supporting Cu the additional requirements in reference [4] must also be met.