

10GEC

THE 10 GIGABIT ETHERNET CONSORTIUM

10GBASE-T Clause 55 PMA Electrical Test Suite

Version 1.1

Technical Document



Last Updated: July7, 2008, 2:00 PM

*10 Gigabit Ethernet Consortium
University of New Hampshire
InterOperability Laboratory*

*121 Technology Drive, Suite 2
Durham, NH 03824
Phone: (603) 862-0205
Fax: (603) 862-4181*

<http://www.ioi.unh.edu/consortiums/10gec>

© 2008 University of New Hampshire InterOperability Laboratory

The University of New Hampshire
InterOperability Laboratory
TABLE OF CONTENTS

TABLE OF CONTENTS	2
MODIFICATION RECORD	3
ACKNOWLEDGMENTS	4
INTRODUCTION	5
GROUP 1: PMA ELECTRICAL SPECIFICATIONS	7
TEST 55.5.3.1 – MAXIMUM OUTPUT DROOP.....	8
TEST 55.5.3.2 – TRANSMITTER LINEARITY	9
TEST 55.5.3.3 – TRANSMITTER TIMING JITTER	10
TEST 55.5.3.4 – TRANSMITTER POWER SPECTRAL DENSITY AND POWER LEVEL	11
TEST 55.5.3.5 – TRANSMIT CLOCK FREQUENCY.....	12
TEST 55.8.3.1 – MDI RETURN LOSS.....	13
TEST SUITE APPENDICES	15
APPENDIX 55.5.A – TRANSMITTER TEST SETUPS	16

The University of New Hampshire
InterOperability Laboratory
MODIFICATION RECORD

- **The Future (Version 1.1)**
David Schwarzenberg Added Appendix A
- **September 6, 2006 (Version 1.0)**
Jon Beckwith Initial Release

The University of New Hampshire
InterOperability Laboratory
ACKNOWLEDGMENTS

The University of New Hampshire would like to acknowledge the efforts of the following individuals in the development of this test suite.

Jon Beckwith	University of New Hampshire
Zach Clifton	University of New Hampshire
Eric Lynskey	University of New Hampshire
David Schwarzenberg	University of New Hampshire

The University of New Hampshire
InterOperability Laboratory

INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the functionality of the Physical Medium Attachment (PMA) sublayer of their 10GBASE-T products.

These tests are designed to determine if a product conforms to specifications defined in the IEEE 802.3 standard. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 10GBASE-T environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

*The University of New Hampshire
InterOperability Laboratory*

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

*The University of New Hampshire
InterOperability Laboratory*

GROUP 1: PMA ELECTRICAL SPECIFICATIONS

Overview:

This group of tests verifies several of the electrical specifications of the 10GBASE-T Physical Medium Attachment sublayer outlined in Clause 55 of the IEEE 802.3-2005TM standard.

Scope:

All of the tests described in this section are currently under development at the University of New Hampshire InterOperability Laboratory.

*The University of New Hampshire
InterOperability Laboratory*

Test 55.5.3.1 – Maximum Output Droop

Purpose: To verify that the transmitter output level does not droop more than the maximum specified amount.

References:

- [1] IEEE standard 802.3an, subclause 55.5.2, Test modes
- [2] IEEE standard 802.3an, subclause 55.5.2.1, Test Fixtures
- [3] IEEE standard 802.3an, subclause 55.5.3.1, Maximum output droop
- [4] Test suite appendix 55.5.A – Transmitter Test Setups
- [5] IEEE standard 802.3an, subclause 55.12.6, Item PME19

Resource Requirements:

- Refer to test suite appendix 55.5.A.

Last Modification: September 6, 2006 (version 1.0)

Discussion:

Reference [1] states that a 10GBASE-T device shall implement 7 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] defines the test fixture to be used to perform the test. Reference [1] defines the operation of a device while in test mode 4, while reference [3] provides a specification for the maximum allowable droop for the transmitter.

This test requires the device under test (DUT) to operate in transmitter test mode 6. While in test mode 6, the DUT shall generate a sequence of 128 +16 symbols followed by 128 –16 symbols continually from all four transmitters with the THP turned off.

Test Setup: Refer to test suite appendix 55.5.A.

Test Procedure:

1. Configure the DUT so that it is operating in transmitter test mode 6.
2. Connect pair BI_DA from the MDI to test fixture 1.
3. Find a rising-edge zero-crossing in the waveform (the reference).
4. Measure the amplitude of the waveform at 10 ns after the reference zero-crossing (V_{10}).
5. Measure the amplitude of the waveform at 90 ns after the reference zero-crossing (V_{90}).
6. Compute the droop between V_{10} and V_{90} .
7. For enhanced accuracy, repeat steps 3-6 multiple times and average the results.
8. Repeat using a falling edge reference.
9. Repeat steps 2 through 8 for pairs BI_DB, BI_DC, and BI_DD.

Observable Results:

- a. The magnitude of both the positive and negative droop shall be less than 10%.

Possible Problems: None.

*The University of New Hampshire
InterOperability Laboratory*

Test 55.5.3.2 – Transmitter Linearity

Purpose: To verify that the output of the transmitter conforms to the transmitter linearity mask.

References:

- [1] IEEE standard 802.3an, subclause 55.5.2, Test Modes
- [2] IEEE standard 802.3an, subclause 55.5.2.1, Test Fixtures
- [3] IEEE standard 802.3an, subclause 55.5.3.2, Transmitter linearity
- [4] Test suite appendix 55.5.A – Transmitter Test Setups
- [5] IEEE standard 802.3an, subclause 55.12.6, Item PME20

Resource Requirements:

- Refer to test suite appendix 55.5.A

Last Modification: September 6, 2006 (version 1.0)

Discussion:

Reference [1] states that a 10GBASE-T device shall implement 7 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] defines the test fixture to be used to perform the test. Reference [1] defines the operation of the device while in test mode 4, while reference [3] provides a specification for the Spurious Free Dynamic Range of the transmitter.

While in test mode 4, the PHY shall transmit, with THP turned off, symbols defined by bits 7.9.12:10 and table 55-4.

Test Setup: Refer to test suite appendix 55.5.A.

Test Procedure:

1. Configure the DUT so that it is operating in transmitter test mode 4.
2. Connect pair BI_DA from the MDI to test fixture 2.
3. Capture the output from the transmitter.
4. For enhanced accuracy, repeat step 3 multiple times and average the voltages measured at each point.
5. Compute the SFDR of the waveform.
6. Repeat steps 3 through 5 for the remainder of the test tones as specified in reference [1].
7. Repeat steps 2 through 6 for pairs BI_DB, BI_DC, and BI_DD.

Observable Results:

- a. While in Test Mode 4, the SFDR of the transmitter when subject to single tone inputs producing output peak-to-peak transmit amplitude shall meet the requirement that:

$$SFDR \geq 2.5 + \min\{52, 58 - 20 * \log_{10}(f / 25)\}$$

where f is the maximum frequency of the two test tones in MHz and SFDR is the ratio in dB of the minimum RMS value of either input tone to the RMS value of the worst intermodulation product in the frequency range of 1 to 400 MHz.

Possible Problems: None.

*The University of New Hampshire
InterOperability Laboratory*

Test 55.5.3.3 – Transmitter Timing Jitter

Purpose: To verify that the transmitter timing jitter of the PMA is within the conformance limits.

References:

- [1] IEEE standard 802.3an, subclause 55.5.2, Test modes
- [2] IEEE standard 802.3an, subclause 55.5.2.1, Test Fixtures
- [3] IEEE standard 802.3an, figure 55-30
- [4] IEEE standard 802.3an, subclause 55.3.3, Transmit timing jitter
- [5] Test suite appendix 55.5.A – Transmitter Test Setups
- [6] IEEE standard 802.3an, subclause 55.12.6, Item PME21 (Master)
- [7] IEEE standard 802.3an, subclause 55.12.6, Item PME22 (Slave)

Resource Requirements:

- Refer to test suite appendix 55.5.A

Last Modification: September 6, 2006 (version 1.0)

Discussion:

Reference [1] states that a 10GBASE-T device shall implement 7 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] and [3] define the test fixture to be used to perform the test. Reference [4] provides a specification for the transmitter timing jitter.

Case 1 – MASTER transmitter timing jitter

When in test mode 2, the PHY transmits 2 +16 symbols followed by 2 –16 symbols continually with the THP turned off and with no power backoff. In this mode, the transmitter output should be a 200 MHz signal and the RMS period jitter measured at the PHY MDI output shall be less than 5.5 ps. The RMS period jitter is measured as per the test configuration shown in Figure 55-30 over an integration time interval of 1 ms +/- 10%.

Case 2 – SLAVE transmitter timing jitter

For a PHY supporting loop timing mode, the MASTER PHY is set to test mode 1 and the SLAVE PHY is in test mode 3. The MASTER PHY transmits the PMA training pattern (PRBS 33) to the SLAVE PHY on pairs A, B and C, and the SLAVE must synchronize its transmit clock to the signals received from the MASTER PHY. The RMS period jitter measured at the SLAVE PHY MDI output shall be less than 5.5 ps.

Test Setup: Refer to test suite appendix 55.5.A.

Test Procedure:

1. Configure the DUT so that it is operating in transmitter test mode 2.
2. Connect pair BI_DA from the MDI to test fixture 3.
3. Capture 1ms±10% using a sample size of 200,000±20,000. Process the capture with a PC to determine the RMS period jitter according to equation 55-8 in reference [4].
4. For enhanced accuracy, repeat step 3 multiple times.
5. Repeat steps 2 through 4 for pairs BI_DB, BI_DC, and BI_DD.
6. If PHY supports loop timing, configure the DUT so that the MASTER PHY is operating in transmitter test mode 1, SLAVE PHY is operating in transmitter test mode 3, and repeat steps 2 through 5.

Observable Results:

- a. The RMS period jitter measured at the MDI output should not exceed 5.5 ps for all cases.

Possible Problems: None.

*The University of New Hampshire
InterOperability Laboratory*

Test 55.5.3.4 – Transmitter Power Spectral Density and Power Level

Purpose: To verify the transmitter power level and power spectral density are within the conformance limits.

References:

- [1] IEEE standard 802.3an, subclause 55.5.2, Test modes
- [2] IEEE standard 802.3an, subclause 55.5.2.1, Test Fixtures
- [3] IEEE standard 802.3an, subclause 55.5.3.4, Transmitter PSD and power level
- [4] IEEE standard 802.3an, figure 55-31, Transmitter PSD mask
- [5] Test suite appendix 55.5.A – Transmitter Test Setups
- [6] IEEE standard 802.3an, subclause 55.12.6, Item PME23 (transmit power level)
- [7] IEEE standard 802.3an, subclause 55.12.6, Item PME24 (PSD)

Resource Requirements:

- Refer to test suite appendix 55.5.A

Last Modification: September 6, 2006 (version 1.0)

Discussion:

Reference [1] states that a 10GBASE-T PHY shall implement 7 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] discusses the operation of a device while in test mode 5. Reference [1] defines the operation of a device while in test mode 5, while reference [3] provides a specification for the transmitter power spectral density and power level. Reference [4] provides the transmitter power spectral density mask.

In test mode 5, the device shall transmit as in normal operation with power backoff disabled. The transmit power shall be between 3.2dBm and 5.2dBm and the power spectral density, measured into 100Ω, shall fit within the upper and lower masks of figure 55-31.

Test Setup: Refer to test suite appendix 55.5.A.

Test Procedure:

1. Configure the DUT so that it is operating in transmitter test mode 5.
2. Connect pair BI-DA to transmitter test fixture 2.
3. Capture the spectrum of the transmitted test mode waveform using a spectrum analyzer.
4. For enhanced accuracy, repeat step 3 multiple times and average the voltages measured at each point.
5. Compute the transmit power and power spectral density.
6. Repeat steps 2 through 5 for pairs BI_DB, BI_DC, and BI_DD.

Observable Results:

- a. The transmit power shall be between 3.2dBm and 5.2dBm.
- b. The power spectral density of the transmitter output while operating in test mode 5 shall fit within the transmitter power spectral density mask shown in figure 55-31.

Possible Problems: None.

*The University of New Hampshire
InterOperability Laboratory*

Test 55.5.3.5 – Transmit Clock Frequency

Purpose: To verify that the frequency of the Transmit Clock is within the conformance limits

References:

- [1] IEEE Std 802.3an, clause 55.5.3.5
- [2] IEEE standard 802.3an, subclause 55.12.6, Item PME25
- [3] Test suite appendix 55.5.A – Transmitter Test Setups

Resource Requirements:

- Refer to appendix 55.5.A

Last Modification: September 6, 2006 (version 1.0)

Discussion:

Reference [1] states that all 10GBASE-T devices must have a quinary symbol transmission rate of 800.00 MHz \pm 50ppm while operating in Master timing mode.

The reference clock used in this test is the one obtained in test 55.5.3.3, Transmitter Timing Jitter. The frequency of this clock extracted from the transmitted waveform shall have a base frequency of 800 MHz \pm 50ppm.

Test Setup: Refer to test suite appendix 55.5.A

Procedure:

1. Configure the DUT for test mode 2 operation.
2. Using a narrow-bandwidth PLL, extract the clock frequency from the transmitted symbols.
3. For enhanced accuracy, repeat step 2 multiple times.
4. Measure the frequency of the transmit clock.

Observable Results:

- a. The transmit clock generated by the DUT shall have a frequency of 800MHz \pm 50ppm.

Possible Problems: None.

*The University of New Hampshire
InterOperability Laboratory*

Test 55.8.3.1 – MDI Return Loss

Purpose: To measure the return loss at the MDI for all four channels

References:

- [1] IEEE Std 802.3an, subclause 55.8.2.1 – MDI return loss.
- [2] IEEE Std 802.3an, subclause 55.5.3 – Test modes
- [3] IEEE Std 802.3an, subclause 55.12.8, Item MDI7 (Return Loss)

Resource Requirements:

- RF Vector Network analyzer (VNA)
- Return loss test jig
- Post-processing PC

Last Modification: September 6, 2006 (version 1.0)

Discussion:

The MDI on a 10GBASE-T device compliant with the IEEE 802.3an standard shall ideally have a differential impedance of 100Ω. Any difference between the impedance of the MDI and the impedance of the connector and cable results in reflections of the transmitted signals. Because the impedances can never be precisely 100Ω, and because the termination impedance varies with frequency, some limited amount of reflections must be allowed.

Return loss is a measure of the signal power that is reflected due to the impedance mismatch. 802.3an specifies that the reflected power at the MDI must be at least 16 dB less than the incident power over the range of 1.0 to 40MHz. The return loss must be at least $16 - 10 \cdot \log_{10}(f / 40)$ dB from 40 to 500MHz (f in MHz). This return loss must be maintained when connected to cabling with a characteristic impedance of 100Ω, and while transmitting data or control symbols.

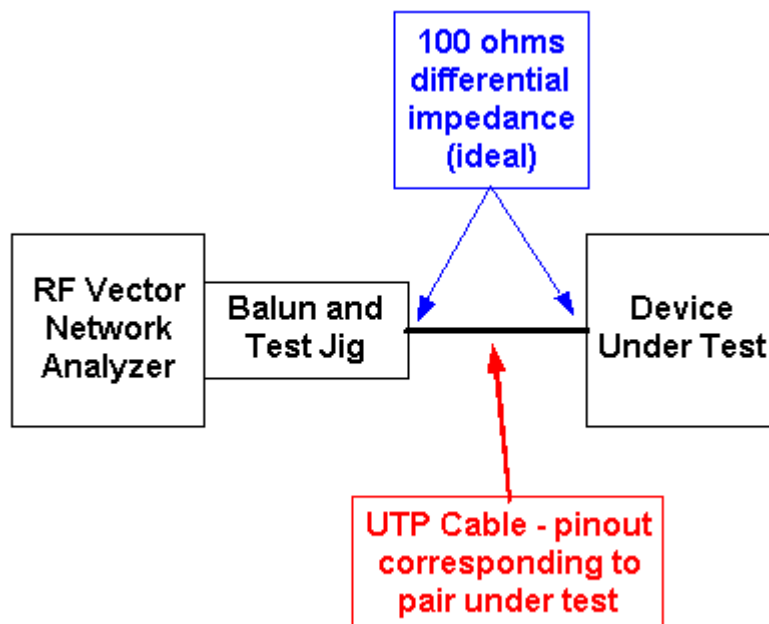


Figure 55.8.3.1-1: Return Loss Test Setup

*The University of New Hampshire
InterOperability Laboratory*

Test Setup:

Connect the devices as shown in figure 55.8.3.1-1.

Procedure:

1. Configure the DUT for test mode 5 operation.
2. Connect pair BI_DA to the reflection port of a network analyzer.
3. Measure the reflection coefficient at the transmitter in the frequency range of 1.0 MHz to 500 MHz.
4. Compute the Return Loss for a Z_S of 85Ω and a Z_S of 115Ω . Assume Z_S to be completely resistive.
5. Repeat above steps for the BI_DB, BI_DC, and BI_DD pairs.

Observable Results:

- a. The return loss measured at each MDI shall be at least 16 dB from 1.0 to 40 MHz, at least $16 - 10 * \log_{10}(f/40)$ dB from 40 to 400 MHz, and at least $6 - 30 * \log_{10}(f/400)$ from 400 to 500 MHz.

The University of New Hampshire
InterOperability Laboratory
TEST SUITE APPENDICES

Overview:

The appendices contained in this section are intended to provide additional low-level technical details pertinent to specific tests defined in this test suite. Test suite appendices often cover topics that are beyond the scope of the standard, but are specific to the methodologies used for performing the measurements covered in this test suite. This may also include details regarding a specific interpretation of the standard (for the purposes of this test suite), in cases where a specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative, and pertain only to tests contained in this test suite.

*The University of New Hampshire
InterOperability Laboratory*

Appendix 55.5.A – Transmitter Test Setups

Purpose: To present an example of the test setups and connecting hardware that may be used to implement the 10GBASE-T PMA test suite.

References:

- [1] IEEE Std 802.3-2005, clause 25
- [2] ANSI X3.263-1995, section 9.1

Resource Requirements:

- Digital Storage Oscilloscope, Agilent Infinium DSO81204A or equivalent
- Vector Network Analyzer, HP 8712B or equivalent
- Spectrum Analyzer, HP E4404B or equivalent
- Balun, ETS PI-102 or equivalent
- Test Jigs #1, #2
- Transceiver in test Mode 1
- Controlling software (MATLAB)

Last Modification: July 7, 2008 (Version 1.1)

Discussion:

55.5.A.1 – Introduction

This appendix describes of the implementation of the 10GBASE-T PMA test suite used by the University of New Hampshire. This description is intended to be an example for those that wish to implement the test suite in their own lab.

Note that in the cases where specific equipment models are specified, any piece of equipment with similar capabilities may be substituted. Also note that the length of the unshielded twisted pair (UTP) cable used to connect the device under test (DUT) to the test jig should be kept as short as possible (less than a foot). If longer lengths are necessary, the impact of the cable on the measurement must be evaluated and steps taken to remove its effect.

55.5.A.2 – Example Test Setups

Test Setup #1

- Test 55.5.3.1 – Maximum Output Droop
- Test 55.5.3.3 – Transmit Timing Jitter – Master Jitter
- Test 55.5.3.5 – Transmit Clock Frequency

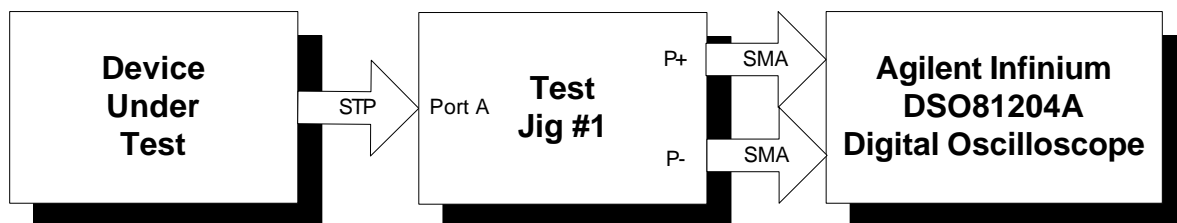


Figure 55.5.A-1: Test Setup #1

*The University of New Hampshire
InterOperability Laboratory*

Test Setup #2

- Test 55.5.3.2 – Transmitter Linearity
- Test 55.5.3.4 – Transmitter Power Spectral Density
-

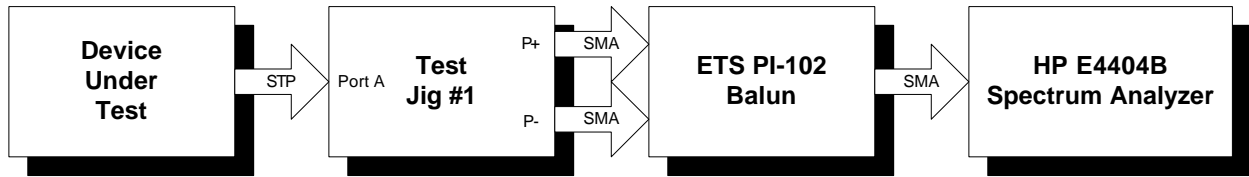


Figure 55.5.A-2: Test Setup #2

Test Setup #3

- Test 55.5.3.3 – Transmit Timing Jitter – Slave Jitter

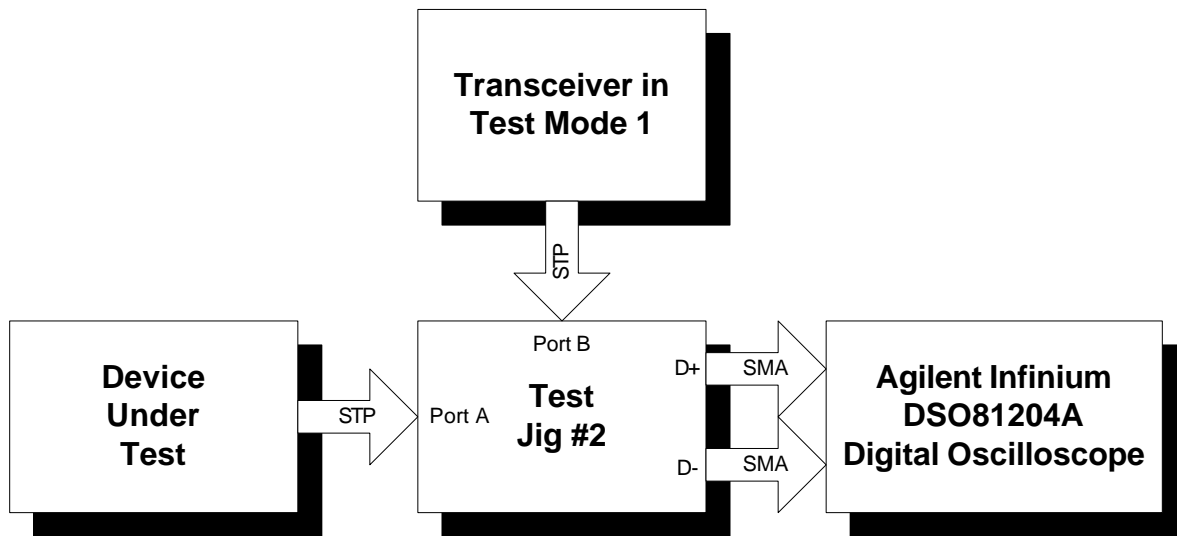


Figure 55.5.A-3: Test Setup #3

Test Setup #4

- Test 55.5.8.1 – MDI Return Loss

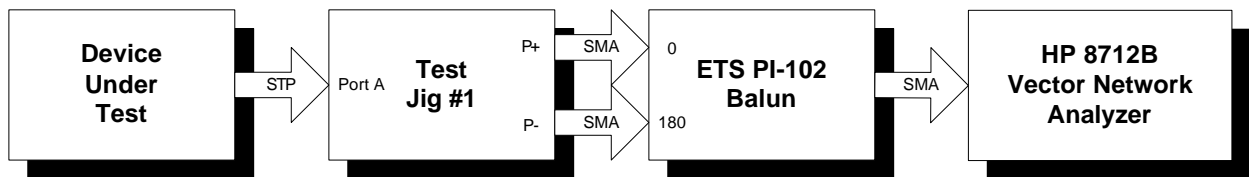


Figure 55.5.A-4: Test Setup #4

55.5.A.3 – Test Jigs

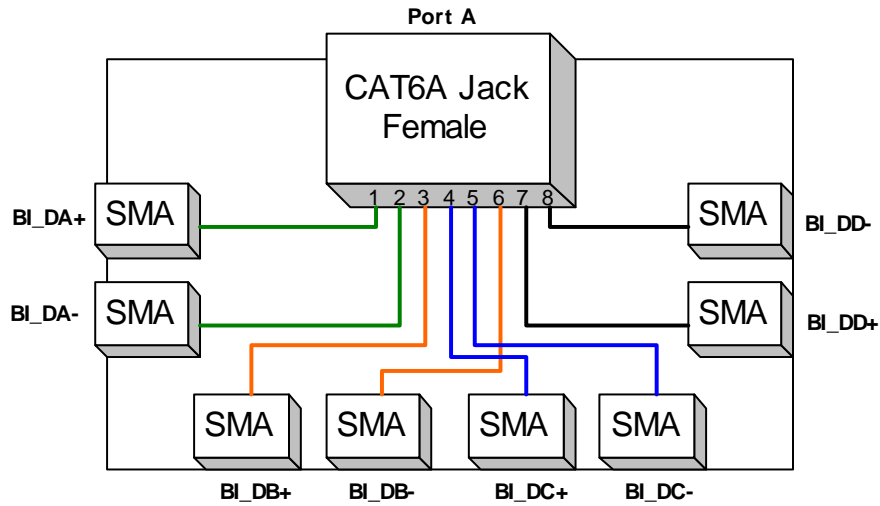


Figure 55.5.A-5: Test Jig #1

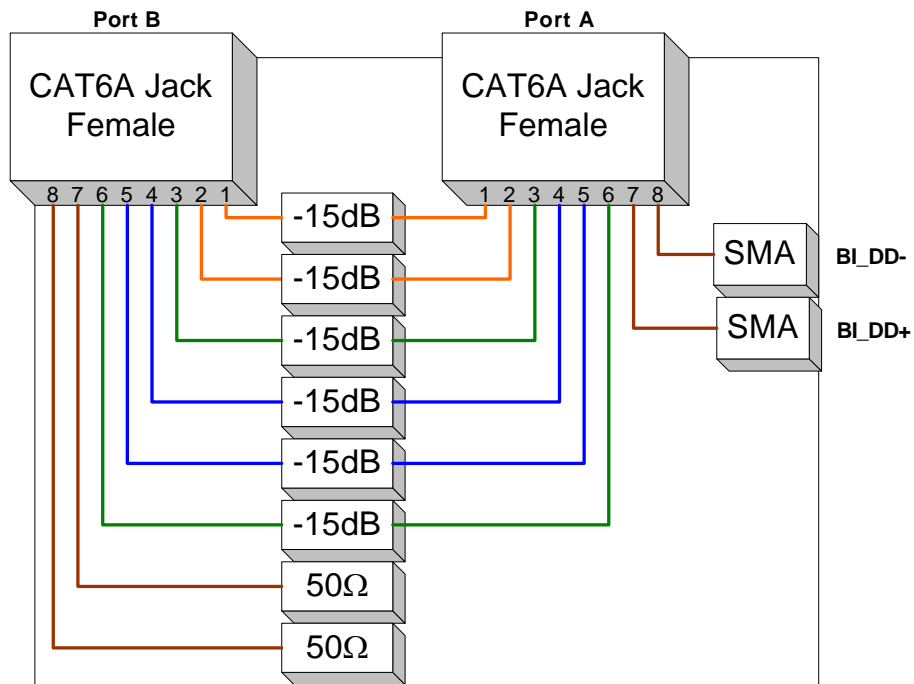


Figure 55.5.A-6: Test Jig #2