UNH IOL SATA Consortium
SATA Physical Layer Test Report

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XXCreateDateXX

XXVendorNameXX
XXVendorCompanyXX
XXVendorAddressXX

Mr. XXVendorLastNameXX:

Enclosed are the test results from the SATA Physical Layer testing performed on the:

XXDUTDescXX

The testing was performed according to Revision 1.4.3 of the *Serial ATA Interoperability Program Unified Test Document*, which may be viewed online at:

http://www.sata-io.org/developers/interop_14.asp

Note that these tests are based on the SATA specification, *Serial ATA International Organization: Serial ATA Revision 3.2*. The tests covered by this report include those which are defined in the *Serial ATA Interoperability Program Revision 1.4.3 Unified Test Document.*

Note that at the time of this testing, the SATA-IO Integrator's List does not support Port Multiplier devices, thus the DUT is not eligible for inclusion on the Integrator's List. However, the results in this report can informatively be treated as if the DUT were an HDD device, for informational purposes. Given this assumption, any failures specific to the v1.4.3 SATA-IO Integrator's List test specifications are listed as follows:

Note also for convenience, any failures specifically impacting r1.4.3 SATA-IO Integrator's List eligibility are listed as follows:

- **The DUT passed all applicable r1.4.3 SATA-IO Integrator's List Physical Layer tests**

Please feel free to contact me via email at XXEmailXX with any questions you may have regarding this report.

Sincerely,

XXTesterNameXX

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Table 1: Test Setup and DUT Configuration Information

DUT Details	
Manufacturer	XXManufacturerXX
Description	XXModelNameXX
Mfr. Serial Number	XXSerialNumberXX
Firmware Version	XXFWVersionXX
UNH-IOL ID Number	XXUNHnumberXX
Test System Hardware	
Real-time DSO	Agilent Infiniium DSA91304A, 13GHz, 40GS/s Real-time DSO Agilent N5411B SATA6G Test App v1.70.9015 Tektronix DSA72004, 20GHz, 50GS/s Real-time DSO
Pattern Generator	Agilent 81134A 3.35GHz Pulse Pattern Generator Tektronix AWG7122B 12GS/s with Option 6
MDI-to-SMA Adapter	Crescent Heart Software TF-SATA-NE/XP, Rev 0B Wilder Technologies SATA-TPA-R 600-101-4000
Time Domain Reflectometer	Agilent DCA-X 86100D, with S-parameter Option 201 and 54754A module Agilent DCA-J 86100C, with S-parameter Option 201 and 54754A module Tektronix CSA8000B, with 80E04 module
RSG Setup	Agilent J-BERT N4903A 12.5Gb/s Serial BERT (FW: 4.94) Tektronix AWG7122B 12GS/s with Option 6 Tektronix MSO7200C Mixed Signal Oscilloscope (Frame Error Counter)
Additional Comments/Notes	

As this device is Gen1 SATA (1.5G) only, only the applicable 1.5G tests were run on the device. As a result, not all of the fields in this report contain result information, as this report uses a generic template that covers all 1.5G, 3.0G, and 6.0G SATA tests. Tests that do not apply to this device are marked 'N/A' in the results, and may be ignored.

In this report, SATA v3.2 spec conformance failures are indicated in red text, enclosed by parentheses. Conformant (i.e., passing) results are indicated in green text. Informative (i.e., non-applicable) results appear in gray text. Informative results that fall outside of their respective conformance ranges are additionally enclosed by parentheses. Note these are not considered conformance failures because the tests are informative, but were performed anyway. (e.g., Gen2/3 Return Loss performed on Gen1 devices.)

This device was tested in BIST-L mode for the PHY/TSG tests, and BIST-TAS (MFTP) for the TX/RX tests. Normal operating mode was used for the OOB tests. The device was observed to support disconnect in both the BIST-TAS and BIST-L modes.

This device was tested in BIST-L mode for the PHY/TSG tests, and BIST-TAS (MFTP) for the TX/RX tests. Normal operating mode was used for the OOB tests. The device was observed to support disconnect in both the BIST-TAS and BIST-L modes, however a power cycle was required in order to cause the device to exit BIST, because the DUT was observed not to exit BIST upon reception of COMRESET.

Note also that this failure is outside of the scope of the SATA-IO Interoperability Program and thus does not impact Integrator's List eligibility, however it is a legitimate conformance issue per the SATA spec.

The DUT was observed to track the frequency of the incoming signal while in BIST-L. This behavior was also observed in normal operation mode. This implies that the DUT mirrors the SSC behavior of its link partner. Since the DUT was tested using a fixed frequency pattern generator the DUT was tested as SSC OFF.

Also, see the Test Notes section following Table 6 for more detailed information regarding the scope and relevance of various tests, particularly with respect to the SATA Interoperability Program, as well as the SATA v3.2 Standard.

Table 2: Summary of PHY/TSG test results for the DUT

Test/Parameter	Range	Measured	Units	Fig.
PHY-01: Unit Interval				
(1.5G rate): Mean UI value	666.4333/670.2333	<g1ui>	ps	-
(3.0G rate): Mean UI value	333.2167/335.1167	<g2ui>	ps	-
(6.0G rate): Mean UI value	166.6083/167.5583	<g3ui>	ps	-
PHY-02: Frequency Long Term Stability(1)				
(1.5G rate): Long term frequency offset from nominal	-350/+350	<g1flts>	ppm	-
(3.0G rate): Long term frequency offset from nominal	-350/+350	<g2flts>	ppm	-
(6.0G rate): Long term frequency offset from nominal	-350/+350	<g3flts>	ppm	-
PHY-03: Spread Spectrum Modulation Frequency(1)				
(1.5G rate) Frequency of SSC modulation (1/period)	30/33	<g1sscf>	kHz	1
(3.0G rate) Frequency of SSC modulation (1/period)	30/33	<g2sscf>	kHz	2
(6.0G rate) Frequency of SSC modulation (1/period)	30/33	<g3sscf>	kHz	3
PHY-04: Spread Spectrum Modulation Deviation(1)				
(1.5G rate) Max SSC frequency deviation	-5350/+350	<g1sscmx>	ppm	1
(1.5G rate) Min SSC frequency deviation	-5350/+350	<g1sscmn>	ppm	1
(3.0G rate) Max SSC frequency deviation	-5350/+350	<g2sscmx>	ppm	2
(3.0G rate) Min SSC frequency deviation	-5350/+350	<g2sscmn>	ppm	2
(6.0G rate) Max SSC frequency deviation	-5350/+350	<g3sscmx>	ppm	3
(6.0G rate) Min SSC frequency deviation	-5350/+350	<g3sscmn>	ppm	3
TSG-01: Differential Output Voltage(2)				
(1.5G rate): VdiffTX(min), for HFTP/MFTP/LBP	>400	<g1dov>	mVpp	4 5 7
(1.5G rate): MFTP pu	<5	<g1mpu>	%	5
(1.5G rate): MFTP pl	<5	<g1mpl>	%	5
(1.5G rate): LFTP pu	<5	<g1lpu>	%	6
(1.5G rate): LFTP pl	<5	<g1lpl>	%	6
(3.0G rate): VdiffTX(min), for HFTP/MFTP/LBP	>400	<g2dov>	mVpp	8 9 11
(3.0G rate): MFTP pu	<5	<g2mpu>	%	9
(3.0G rate): MFTP pl	<5	<g2mpl>	%	9
(3.0G rate): LFTP pu	<5	<g2lpu>	%	10
(3.0G rate): LFTP pl	<5	<g2lpl>	%	10
TSG-02: Rise/Fall Time(3)				
(1.5G rate): LFTP: Rise time	50/273	<g1lrise>	ps	-
(1.5G rate): LFTP: Fall time	50/273	<g1lfall>	ps	-
(3.0G rate): LFTP: Rise time	50/136	<g2lrise>	ps	-
(3.0G rate): LFTP: Fall time	50/136	<g2lfall>	ps	-
(6.0G rate): LFTP: Rise time	33/80	<g3lrise>	ps	-
(6.0G rate): LFTP: Fall time	33/80	<g3lfall>	ps	-

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Table 2: (continued)

Test/Parameter	Range	Measured	Units	Fig.
TSG-03: Differential Skew[10]				
(1.5G rate): HFTP: Skew	<20	<g1hsk>	ps	-
(1.5G rate): MFTP: Skew	<20	<g1msk>	ps	
(3.0G rate): HFTP: Skew	<20	<g2hsk>	ps	-
(3.0G rate): MFTP: Skew	<20	<g2msk>	ps	
(6.0G rate): HFTP: Skew	<20	<g3hsk>	ps	-
(6.0G rate): MFTP: Skew	<20	<g3msk>	ps	
TSG-04: AC Common Mode Voltage[4]				
(3.0G rate) Pk-pk Amplitude of AC CM voltage	<50	<g2cmv>	mV	-
TSG-05: Rise/Fall Imbalance (OBSOLETE)[5]				
(3.0G rate): TX+ rise / TX- fall (max) HFTP	<20	<g2hrf>	%	-
(3.0G rate): TX+ fall / TX- rise (max) HFTP	<20	<g2hfr>	%	-
(3.0G rate): TX+ rise / TX- fall (max) MFTP	<20	<g2mrf>	%	-
(3.0G rate): TX+ fall / TX- rise (max) MFTP	<20	<g2mfr>	%	-
TSG-06: Amplitude Imbalance (OBSOLETE) [5]				
(3.0G rate): HFTP Imbalance	<10	<g2hbal>	%	-
(3.0G rate): MFTP Imbalance	<10	<g2mbal>	%	-
TSG-07: Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, $f_{BAUD}/10$ (OBSOLETE)[5]				
(This test is considered obsolete for SATA-IO Logo Program revisions r1.3 and above.)	-	-	-	-
TSG-08: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, $f_{BAUD}/10$ (OBSOLETE)[5]				
(This test is considered obsolete for SATA-IO Logo Program revisions r1.3 and above.)	-	-	-	-
TSG-09: Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, $f_{BAUD}/500$ [6]				
(1.5G rate): TJ with HFTP	<370	<g1htj>	mUI	-
(1.5G rate): TJ with LBP	<370	<g1btj>	mUI	-
TSG-10: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, $f_{BAUD}/500$ [6]				
(1.5G rate): DJ with HFTP	<190	<g1hdj>	mUI	-
(1.5G rate): DJ with LBP	<190	<g1bdj>	mUI	-

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Table 2: (continued)

Test/Parameter	Range	Measured	Units	Fig.
TSG-11: Gen2 (3.0Gb/s) TJ at Connector, Clock to Data, $f_{BAUD}/500$[6]				
(3.0G rate): TJ with HFTP	<370	<g2htj>	mUI	-
(3.0G rate): TJ with LBP	<370	<g2btj>	mUI	-
TSG-12: Gen2 (3.0Gb/s) DJ at Connector, Clock to Data, $f_{BAUD}/500$[6]				
(3.0G rate): DJ with HFTP	<190	<g2hdj>	mUI	-
(3.0G rate): DJ with LBP	<190	<g2bdj>	mUI	-
TSG-13: Gen3 (6Gb/s) Transmit Jitter[12]				
(6.0G rate): RJ before CIC (MFTP)	<180	<tsg13a>	mUI	-
(6.0G rate): TJ before CIC (LBP), *minus* measured RJ	<<XXtsg13b_limitXX>340	<tsg13b>	mUI	
(6.0G rate): TJ after CIC (LBP), *minus* measured RJ	<<XXtsg13c_limitXX>340	<tsg13c>	mUI	
(6.0G rate): TJ after CIC (LBP), ECN39, BER = 1E-6	<460	<tsg13d>	mUI	
(6.0G rate): TJ after CIC (LBP), ECN39, BER = 1E-12	<520	<tsg13e>	mUI	
TSG-14: Gen3 (6Gb/s) TX Maximum Differential Voltage Amplitude				
(6.0G rate): Pk-pk amplitude of averaged MFTP waveform	<900	<tsg14a>	mVppd	-
TSG-15: Gen3 (6Gb/s) TX Minimum Differential Voltage Amplitude				
(6.0G rate): Minimum eye opening after CIC (LBP pattern)	>240	<tsg15a>	mVppd	-
TSG-16: Gen3 (6Gb/s) TX AC Common Mode Voltage				
(6.0G rate): HFTP spectral magnitude @ 3GHz	<26	<tsg16a>	dBmV(pk)	-
(6.0G rate): HFTP spectral magnitude @ 6GHz	<30	<tsg16b>	dBmV(pk)	-

Table 3: Summary of TX/RX test results for the DUT

Test/Parameter	Range	Measured	Units	Fig.
TX-01: TX Pair Differential Impedance[7][11]				
Maximum differential impedance of TX Pair (TDD22)	85 to 115	<tx01a>	Ohms	12
Minimum differential impedance of TX Pair (TDD22)	85 to 115	<tx01b>	Ohms	12
Final termination impedance value (2ns post-dip)	85 to 115	<tx01c>	Ohms	12
TX-02: TX Single-Ended Impedance (Obsolete)[8]				
Minimum value of TX+ single-ended impedance (T11)	>40	<tx02a>	Ohms	13
Minimum value of TX- single-ended impedance (T33)	>40	<tx02b>	Ohms	13
TX-03: Gen2 (3Gb/s) TX Differential Mode Return Loss[9] [11]				
Minimum return loss (SDD22) from 150 to 300 MHz	>14	<tx03a>	dB	14
Minimum return loss (SDD22) from 300 to 600 MHz	>8	<tx03b>	dB	14
Minimum return loss (SDD22) from 600 to 1200 MHz	>6	<tx03c>	dB	14
Minimum return loss (SDD22) from 1200 to 2400 MHz	>6	<tx03d>	dB	14
Minimum return loss (SDD22) from 2400 to 3000 MHz	>3	<tx03e>	dB	14
Minimum return loss (SDD22) from 3000 to 5000 MHz	>1	<tx03f>	dB	14
TX-04: Gen2 (3Gb/s) TX Common Mode Return Loss[9] [11]				
Minimum return loss (SCC22) from 150 to 300 MHz	>8	<tx04a>	dB	15
Minimum return loss (SCC22) from 300 to 600 MHz	>5	<tx04b>	dB	15
Minimum return loss (SCC22) from 600 to 1200 MHz	>2	<tx04c>	dB	15
Minimum return loss (SCC22) from 1200 to 2400 MHz	>2	<tx04d>	dB	15
Minimum return loss (SCC22) from 2400 to 3000 MHz	>2	<tx04e>	dB	15
Minimum return loss (SCC22) from 3000 to 5000 MHz	>1	<tx04f>	dB	15
TX-05: Gen2 (3Gb/s) TX Impedance Balance[9] [11]				
Minimum return loss (SDC22) from 150 to 300 MHz	>30	<tx05a>	dB	16
Minimum return loss (SDC22) from 300 to 600 MHz	>20	<tx05b>	dB	16
Minimum return loss (SDC22) from 600 to 1200 MHz	>10	<tx05c>	dB	16
Minimum return loss (SDC22) from 1200 to 2400 MHz	>10	<tx05d>	dB	16
Minimum return loss (SDC22) from 2400 to 3000 MHz	>4	<tx05e>	dB	16
Minimum return loss (SDC22) from 3000 to 5000 MHz	>4	<tx05f>	dB	16
TX-06: Gen1 (1.5Gb/s) TX Differential Mode Return Loss[7] [11]				
Minimum return loss (SDD22) from 75 to 150 MHz	>14	<tx06a>	dB	17
Minimum return loss (SDD22) from 150 to 300 MHz	>8	<tx06b>	dB	17
Minimum return loss (SDD22) from 300 to 600 MHz	>6	<tx06c>	dB	17
Minimum return loss (SDD22) from 600 to 1200 MHz	>6	<tx06d>	dB	17
Minimum return loss (SDD22) from 1200 to 2400 MHz	>3	<tx06e>	dB	17
Minimum return loss (SDD22) from 2400 to 3000 MHz	>1	<tx06f>	dB	17
TX-07: Gen3 (6Gb/s) TX Differential Mode Return Loss[9] [11]				
Minimum return loss margin (SDD22) from 300 to 3000 MHz	>0	<tx07a>	dB	18
TX-08: Gen3 (6Gb/s) TX Impedance Balance[9] [11]				
Minimum return loss (SDC22) from 150 to 300 MHz	>30	<tx08a>	dB	19
Minimum return loss (SDC22) from 300 to 600 MHz	>30	<tx08b>	dB	19
Minimum return loss (SDC22) from 600 to 1200 MHz	>20	<tx08c>	dB	19
Minimum return loss (SDC22) from 1200 to 2400 MHz	>10	<tx08d>	dB	19
Minimum return loss (SDC22) from 2400 to 3000 MHz	>10	<tx08e>	dB	19
Minimum return loss (SDC22) from 3000 to 5000 MHz	>4	<tx08f>	dB	19
Minimum return loss (SDC22) from 5000 to 6500 MHz	>4	<tx08g>	dB	19

Table 4: Summary of TX/RX test results for the DUT

Test/Parameter	Range	Measured	Units	Fig.
RX-01: RX Pair Differential Impedance[7][11]				
Maximum differential impedance of RX pair (TDD11)	85 to 115	<rx01a>	Ohms	20
Minimum differential impedance of RX pair (TDD11)	85 to 115	<rx01b>	Ohms	20
Final termination impedance value (2ns post-dip)	85 to 115	<rx01c>	Ohms	20
RX-02: RX Single-Ended Impedance (Obsolete)[8]				
Minimum value of RX+ single-ended impedance (T11)	>40	<rx02a>	Ohms	21
Minimum value of RX- single-ended impedance (T33)	>40	<rx02b>	Ohms	21
RX-03: Gen2 (3Gb/s) RX Differential Mode Return Loss[9] [11]				
Minimum return loss (SDD11) from 150 to 300 MHz	>18	<rx03a>	dB	22
Minimum return loss (SDD11) from 300 to 600 MHz	>14	<rx03b>	dB	22
Minimum return loss (SDD11) from 600 to 1200 MHz	>10	<rx03c>	dB	22
Minimum return loss (SDD11) from 1200 to 2400 MHz	>8	<rx03d>	dB	22
Minimum return loss (SDD11) from 2400 to 3000 MHz	>3	<rx03e>	dB	22
Minimum return loss (SDD11) from 3000 to 5000 MHz	>1	<rx03f>	dB	22
RX-04: Gen2 (3Gb/s) RX Common Mode Return Loss[9] [11]				
Minimum return loss (SCC11) from 150 to 300 MHz	>5	<rx04a>	dB	23
Minimum return loss (SCC11) from 300 to 600 MHz	>5	<rx04b>	dB	23
Minimum return loss (SCC11) from 600 to 1200 MHz	>2	<rx04c>	dB	23
Minimum return loss (SCC11) from 1200 to 2400 MHz	>2	<rx04d>	dB	23
Minimum return loss (SCC11) from 2400 to 3000 MHz	>2	<rx04e>	dB	23
Minimum return loss (SCC11) from 3000 to 5000 MHz	>1	<rx04f>	dB	23
RX-05: Gen2 (3Gb/s) RX Impedance Balance[9] [12]				
Minimum return loss (SDC11) from 150 to 300 MHz	>30	<rx05a>	dB	24
Minimum return loss (SDC11) from 300 to 600 MHz	>30	<rx05b>	dB	24
Minimum return loss (SDC11) from 600 to 1200 MHz	>20	<rx05c>	dB	24
Minimum return loss (SDC11) from 1200 to 2400 MHz	>10	<rx05d>	dB	24
Minimum return loss (SDC11) from 2400 to 3000 MHz	>4	<rx05e>	dB	24
Minimum return loss (SDC11) from 3000 to 5000 MHz	>4	<rx05f>	dB	24
RX-06: Gen1 (1.5Gb/s) RX Differential Mode Return Loss[7] [11]				
Minimum return loss (SDD11) from 75 to 150 MHz	>18	<rx06a>	dB	25
Minimum return loss (SDD11) from 150 to 300 MHz	>14	<rx06b>	dB	25
Minimum return loss (SDD11) from 300 to 600 MHz	>10	<rx06c>	dB	25
Minimum return loss (SDD11) from 600 to 1200 MHz	>8	<rx06d>	dB	25
Minimum return loss (SDD11) from 1200 to 2400 MHz	>3	<rx06e>	dB	25
Minimum return loss (SDD11) from 2400 to 3000 MHz	>1	<rx06f>	dB	25
RX-07: Gen3 (6Gb/s) RX Differential Mode Return Loss[9] [11]				
Minimum return loss margin (SDD11) from 300 to 6000 MHz	>0	<rx07a>	dB	26
RX-08: Gen3 (6Gb/s) RX Impedance Balance[9] [11]				
Minimum return loss (SDC11) from 150 to 300 MHz	>30	<rx08a>	dB	27
Minimum return loss (SDC11) from 300 to 600 MHz	>30	<rx08b>	dB	27
Minimum return loss (SDC11) from 600 to 1200 MHz	>20	<rx08c>	dB	27
Minimum return loss (SDC11) from 1200 to 2400 MHz	>10	<rx08d>	dB	27
Minimum return loss (SDC11) from 2400 to 3000 MHz	>10	<rx08e>	dB	27
Minimum return loss (SDC11) from 3000 to 5000 MHz	>4	<rx08f>	dB	27
Minimum return loss (SDC11) from 5000 to 6500 MHz	>4	<rx08g>	dB	27

Table 5: Summary of OOB test results for the DUT

Test/Parameter	Range	Measured	Units
OOB-01: OOB Signal Detection Threshold			
Verify that DUT rejects bursts with amplitude of xx40xxmVppd	Should Reject	<oob01a>	-
Verify that DUT detects bursts with amplitude of 210mVppd	Should Detect	<oob01b>	-
Measured minimum COMINIT detection level	xx50xx/200	<oob01e>	mVppd
OOB-02: UI During OOB Signaling			
Mean UI during OOB burst signaling	646.67/686.67	<oob02>	ps
OOB-03: COMINIT/RESET/WAKE Transmit Burst Length			
Mean length of OOB signaling bursts	103.5/110.9	<oob03>	ns
OOB-04: COMINIT/RESET Transmit Gap Length			
Mean length of COMINIT/RESET signaling gaps	310.4/329.6	<oob04>	ns
OOB-05: COMWAKE Transmit Gap Length			
Mean length of COMWAKE signaling gaps	102.4/109.9	<oob05>	ns
OOB-06: COMWAKE Gap Detection Windows			
Verify that DUT rejects bursts gapped at $45UI_{OOB}$ (30ns)	Should Reject	<oob06c>	-
Verify that DUT detects bursts gapped at $155UI_{OOB}$ (103.33ns)	Should Detect	<oob06a>	-
Verify that DUT detects bursts gapped at $165UI_{OOB}$ (110ns)	Should Detect	<oob06b>	-
Verify that DUT rejects bursts gapped at $266UI_{OOB}$ (177.33ns)	Should Reject	<oob06d>	-
Minimum detected COMWAKE burst spacing	52.5/151.95	<oob06e>	UI_{OOB}
Maximum detected COMWAKE burst spacing	168/262.5	<oob06f>	UI_{OOB}
OOB-07: COMINIT/RESET Gap Detection Windows			
Verify that DUT rejects bursts gapped at $259UI_{OOB}$ (172.66ns)	Should Reject	<oob07c>	-
Verify that DUT detects bursts gapped at $459UI_{OOB}$ (306ns)	Should Detect	<oob07a>	-
Verify that DUT detects bursts gapped at $501UI_{OOB}$ (334ns)	Should Detect	<oob07b>	-
Verify that DUT rejects bursts gapped at $791UI_{OOB}$ (527.33ns)	Should Reject	<oob07d>	-
Minimum detected COMINIT/RESET burst spacing	262.5/456	<oob07e>	UI_{OOB}
Maximum detected COMINIT/RESET burst spacing	504/787.5	<oob07f>	UI_{OOB}

Table 6: Summary of RSG test results for the DUT

Test/Parameter	Frames Sent	CRC Errors Observed
RSG-01: Gen1 (1.5Gb/s) RX Jitter Tolerance Test (TJ=0.501UI, RJ=0.180UI, Amplitude=325mV)		
Deterministic Jitter Frequency: 5 MHz	10,000,000	<rsg01d>
Deterministic Jitter Frequency: 10 MHz	10,000,000	<rsg01a>
Deterministic Jitter Frequency: 33 MHz	10,000,000	<rsg01b>
Deterministic Jitter Frequency: 62 MHz	10,000,000	<rsg01c>
RSG-02: Gen2 (3.0Gb/s) RX Jitter Tolerance Test (TJ=0.552UI, RJ=0.180UI, Amplitude=275mV)		
Deterministic Jitter Frequency: 5 MHz	10,000,000	<rsg02d>
Deterministic Jitter Frequency: 10 MHz	10,000,000	<rsg02a>
Deterministic Jitter Frequency: 33 MHz	10,000,000	<rsg02b>
Deterministic Jitter Frequency: 62 MHz	10,000,000	<rsg02c>
RSG-03: Gen3 (6.0Gb/s) RX Jitter Tolerance Test (TJ=0.498UI, RJ=0.180UI, Amplitude=240mV)		
Deterministic Jitter Frequency: 5 MHz	10,000,000	<rsg03d>
Deterministic Jitter Frequency: 10 MHz	10,000,000	<rsg03a>
Deterministic Jitter Frequency: 33 MHz	10,000,000	<rsg03b>
Deterministic Jitter Frequency: 62 MHz	10,000,000	<rsg03c>
RSG-04: (Reserved Place Holder)		
(Test name/number reserved for future development)	-	-
RSG-05: Gen1 (1.5Gb/s) Receiver Stress Test at +350ppm (TJ=0.501UI, RJ=0.180UI, Amplitude=325mV)		
Deterministic Jitter Frequency: 62 MHz	100,000	<rsg05a>
RSG-06: Gen1 (1.5Gb/s) Receiver Stress Test with SSC (TJ=0.501UI, RJ=0.180UI, Amplitude=325mV)		
Deterministic Jitter Frequency: 62 MHz	100,000	<rsg06a>

Test Notes

(1): While the SATA v3.2 Standard specifies this requirement for all supported speeds, the SATA r1.4.3 Logo Program only requires verification of this parameter at the highest supported speed. For the purposes of the SATA r1.4.3 Logo Program, the lower speed results can be considered informative. However, verification at all supported speeds is required if demonstration of full conformance to the SATA v3.2 Standard is desired.

(2): The SATA r1.4.3 Logo Program requires the measurement of VdiffTX(min) at 1.5 and 3.0Gbps for products that support these operating speeds, and considers the pu/pl results for Maximum Amplitude to be informative for these products. However, verification of pu/pl for Maximum Amplitude is still required if full conformance to the SATA v3.2 Standard is desired. (Also note that these tests are not applicable to devices supporting 6.0G operation. See tests TSG-14/15 instead.)

(3): The obsolete SATA v2.6 Standard specified that the rise/fall measurements be performed on HFTP, LFTP, and LBP patterns, at all supported speeds. However, this requirement was changed in the SATA 3.0 Standard, such that the measurements are now performed using only the LFTP pattern. Also, the *SATA-IO Interoperability Program Revision 1.4.3 Unified Test Document* states that "Failures at minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for Interop testing." Thus, any failures below the minimum limits (e.g., 50, 50, and 33ps for 1.5G, 3.0G, and 6.0G products, respectively) should be considered informative by the definition of TSG-02 in the *SATA-IO Interoperability Program Revision 1.4.3*. TSG-02 was reclassified as informative as of the SATA r1.4.3 Logo Program. However, conformance to both the maximum and minimum limits is required if full conformance to the SATA v3.2 Standard is desired.

(4): This requirement applies only to products that support an operating speed of 3.0G, as per the SATA v3.2 Standard.

(5): Tests TSG-05 and TSG-06 were reclassified as obsolete as of the SATA r1.4 Logo Program. however, the requirements for TSG-06 are still included in the SATA 3.2 Standard. Test TSG-05 was reclassified as obsolete as of the SATA v3.2 Standard. Tests TSG-07 and TSG-08 were reclassified as obsolete as of the SATA r1.3 Logo Program, and the requirements were removed entirely from the specification for the SATA 3.0 Standard.

(6): While the SATA v3.2 Standard specifies that all jitter requirements shall be verified at 1.5G and 3.0G rates using all of the data patterns defined in section 7.2.4.3 (LTDP, HTDP, LFSCP, SSOP, LBP, and COMP), verification using all specified patterns is not practical, due to the time required. To simplify this issue, the SATA-IO Logo Program requires verification using only the HFTP and LBP patterns for the 1.5G and 3.0G operating speeds.

(7): The SATA v2.5 Standard originally defined a conformance range of 85 to 115 ohms for the differential TDR impedance profile of products that supported operation at 1.5G. Through testing performed at multiple SATA-IO events, it was discovered that nearly all products were incapable of meeting this requirement, due to a capacitive dip caused by the ESD protection diodes found in nearly all IC's, which causes the impedance to fall below the 85-ohm minimum for some duration. In order to define a practical specification that was capable of being met by many products, the SATA r1.0 Logo Program introduced a new test, which effectively verified a subset of the original spec requirement, by measuring only the final termination impedance value, occurring at the time point located 2ns after the last major capacitive dip in the impedance profile. The SATA r1.0 Logo Program required only that this final termination impedance value be between 85 and 115 ohms in order to pass TX/RX-01.

Following the creation the '2ns' Final Termination Impedance Value test, the SATA-IO PHY Working Group took measures to address the issue formally in the standard, and released a Technical Errata to the SATA v2.5 Standard, referred to as *ECN-021*, which defines a new impedance specification for 1.5G

operation, specified as Differential Return Loss, similar to the specifications defined for 3.0G. The Errata specifies that 1.5G products must pass *either* the existing TDR specification **OR** the new return loss requirement in order to demonstrate conformance to the Standard. These changes were incorporated into the SATA r1.1 Logo Program documentation, in the form of new tests TX/RX-06. According to the SATA r1.1 Logo Program requirements, all results for TX/RX-01 will be rendered informative if a product passes the TX/RX-06 return loss requirements. These requirements remained unchanged for the SATA r1.4 Logo Program.

Additionally, on March 1, 2007, the SATA-IO initiated a formal waiver to the r1.1 Program, pertaining to the TX/RX-01/06 tests for Gen1 products. The waiver states, *"In evaluation of the pass/fail criteria for Transmit Pair Differential Impedance (TX-01), if the existing min/max results criteria result in a failure, then the 2ns measured result shall be taken into consideration. If the 2ns result is measured between 85 ohms and 115 ohms, then the assessment of TX-01 shall be 'PASS'".* This implies that if a product fails TX-06 and the min/max impedance tests of TX-01, but the '2ns' Final Termination Impedance value is between 85 and 115 ohms, TX-01 is considered passing, and hence the results for TX-06 are considered informative.

Note that a similar waiver was also specified for RX-01. Documentation regarding the waivers for TX/RX-01 can be found at http://www.sata-io.org/documents/Interop_Waiver_Rev1_1_v10.pdf.

Note also that these waivers for TX/RX-01 only apply to the r1.1 Logo Program, and do not apply to the r1.0, r1.2, r1.3, r1.4, or r1.4.3 Logo Programs.

(8): The SATA v3.2 Standard defines a specification for Single-Ended Impedance for products supporting operation at 1.5G. The SATA r1.0 Logo Program included this requirement, defined as tests TX/RX-02. These tests were since reclassified as informative for the SATA r1.1 and r1.2 Logo Programs and SATA r1.3 reclassified as obsolete, however they are still required if full conformance to the SATA v3.2 Standard is to be claimed.

(9): The *SATA-IO Interoperability Program Revision 1.4.3 Unified Test Document* only defines the relevant TX/RX measurements that apply to the highest supported DUT rate. Because the automated tools used by UNH IOL for performing the TX/RX tests perform all of the TX/RX 01-08 measurements on a particular interface at a given speed, any TX/RX results appearing for speeds lower than the maximum supported speed are provided purely for informational purposes only, are considered informative, as the measurements were performed while the product was operating at the highest supported speed.

(10): Test TSG-03 was reclassified as informative as of the SATA r1.4.3 Logo Program. However, verification of TX Differential Skew is still required if full conformance to the SATA v3.2 standard is desired.

(11): All transmitter and receiver impedance and return loss tests (Tests TX-01 through -08 and RX-01 through -08) were reclassified as informative as of the SATA r1.4.3 Logo Program. However, verification of these requirements is still required if full conformance to the SATA v3.2 standard is desired.

(12): Test TSG-13: (6.0G rate): RJ before CIC (MFTP) was reclassified as informative as of the SATA r1.4.3 Logo Program. However, TSG-13: (6.0G rate): TJ after CIC (LBP), ECN39, BER = 1E-6 and TSG-13: (6.0G rate): TJ after CIC (LBP), ECN39, BER = 1E-12 must still pass for SATA r1.4.3.

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