UNH IOL PCIe Consortium PCIe Gen 3 CEM Transmitter Testing

InterOperability Lab — 121 Technology Drive, Suite 2 — Durham, NH 03824 — (603) 862-0701

January 24, 2014

Mr. Vendor Company Name Address

Mr. Vendor:

Enclosed are the results from the PCIe Gen 3 CEM Receiver testing performed on the:

20140106 UNHID Company DUT PCIe Gen 3 Platform/AIC

The testing was performed according to Version 0.91 of the PCI Sig, PCI Express 3.0 CEM RX Physical Layer Test Method of Implementation for Agilent J-BERT N4903B High Performance Serial BERT, which is available online at:

http://www.pcisig.com/members/downloads/specifications/Agilent PCIe 3.0 8G RX MOI v0 91.pdf

Note that the tests defined in this test suite are based on:

PCI Express Base Specification Revision 3.0, version 1.0 PCI Express Card Electromechanical Specification Revision 3.0, version 0.9 PCI Express® Architecture PHY Test Specification Revision 3.0, Ver. 0.9

Please feel free to contact me at <u>jbeaudet@iol.unh.edu</u> if you have any questions regarding the test suite, or the results contained in this report.

Sincerely,

Joshua Beaudet

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Table 1: Test Equipment and DUT	Configuration/Feature Information
DUT Details	
Manufacturer	
Model	
Device Type (Platform/AIC)	
Mfr. Serial Number	
BIOS Version	
Hardware Version	
Software Version	
UNH-IOL ID Number	
Processor Details (If applicable)	
Spec	
Lot Information	
Manufacture Location	
Lot Numbers	
Test System Hardware	
Real-time DSO	Agilent Infiniium DSO91304A, 13GHz, 40GS/s Real-time
	DSO
Test Fixture	PCI Sig PCIe x16 Compliance Base Board
Additional Comments/Notes	
Table 3 and 4 results are gathered usi	ing the waveforms with the least amount of equalization. For Gen 1 this
1. 1	Con 2 this is the 2.5 dD and by Con 2 this is asset 4

is the only one supported is used. For Gen 2 this is the -3.5 dB mode. For Gen 3 this is preset 4.

All Eye Mask tests are done with at least 1E6 bits.



Figure 1: Test Setup

Note: This setup was used for capturing the waveforms.

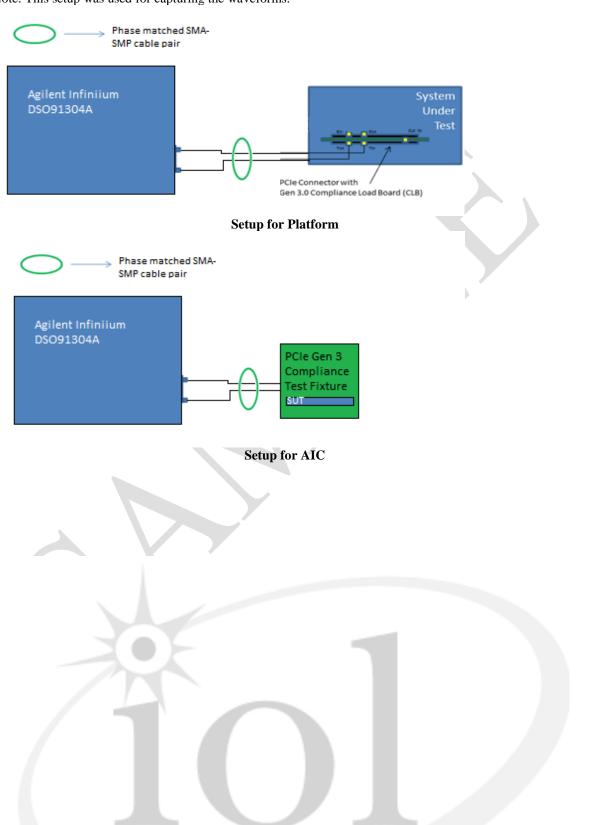


Table 2: TX Jitter and Eye Requirements

Slot x, Lane y				
Test/Parameter	Valid Range	Measured	Units	Figure
Test 1.1: TX Jitter - Gen 1				
Median to Mean	-	23.29	ps	
Median to Maximum	125	122.23	mUI	
Median to Minimum	=	14.54	ps	
Test 1.2: TX Jitter - Gen 2				
Gen 2 (-3.5 dB)				
Deterministic jitter > 1.5MHz (DD)	<=150	59.5	mUI	
Random jitter < 1.5MHz (RMS)	<=3.00	1.56	ps	
Total jitter	-	33.84	ps	
•				
Gen 2 (-6.0 dB)				
Deterministic jitter > 1.5MHz (DD)	<=150	65	mUI	
Random jitter < 1.5MHz (RMS)	<=3.00	2.10	ps	
Total jitter	-	38.49	ps	
10001		00113	P	
Test 1.3: TX Jitter – Gen 3				
Gen 3 (P0)				
Uncorrelated deterministic jitter	<=12	8.7	ps	
Data dependent jitter	<=18	12	ps	
Total uncorrelated Jitter	<=31.25	28.2	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	7.6	ps	
Total uncorrelated PWJ	<=24	23.5	ps	
Total uncorrelated I W3	<u></u>	23.3	ps	
Gen 3 (P1)				
Uncorrelated deterministic jitter	<=12	7.3	ps	
Data dependent jitter	<=18	11	ps	
Total uncorrelated Jitter	<=31.25	27.9	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	6.7	*	
Total uncorrelated PWJ	<=24	23.9	ps	
Total uncorrelated F w J	<-24	23.9	ps	
Gen 3 (P2)				
Uncorrelated deterministic jitter	<=12	0.6	no	
	<=18	9.6	ps	
Data dependent jitter Total uncorrelated Jitter			ps	
Deterministic (DjDD) uncorrelated PWJ	<=31.25	28.6	ps	
	<=10	8.7	ps	
Total uncorrelated PWJ	<=24	21.3	ps	
C 2 (N2)				
Gen 3 (P3)	. 12	0.2		
Uncorrelated deterministic jitter	<=12	8.3	ps	
Data dependent jitter	<=18	15	ps	
Total uncorrelated Jitter	<=31.25	30.5	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	8.8	ps	
Total uncorrelated PWJ	<=24	22.2	ps	
G 3 (P4)		-		
Gen 3 (P4)				
Uncorrelated deterministic jitter	<=12	6.9	ps	
Data dependent jitter	<=18	9.0	ps	
Total uncorrelated Jitter	<=31.25	26.2	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	5.3	ps	
Total uncorrelated PWJ	<=24	20.6	ps	

Test/Parameter	Valid Range	Measured	Units	Figure
Test 1.3: TX Jitter – Gen 3 (Continued)				
Gen 3 (P5)				
Uncorrelated deterministic jitter	<=12	9.3	ps	
Data dependent jitter	<=18	13	ps	
Total uncorrelated Jitter	<=31.25	27.6	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	9.7	ps	
Total uncorrelated PWJ	<=24	23.6	ps	
		2010	F~	
Gen 3 (P6)				
Uncorrelated deterministic jitter	<=12	8.3	ps	
Data dependent jitter	<=18	13	ps	
Total uncorrelated Jitter	<=31.25	26.9	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	7.7	ps	
Total uncorrelated PWJ	<=24	21.9	ps	
Town discretified I we			Po	
Gen 3 (P7)				
Uncorrelated deterministic jitter	<=12	8.2	ps	
Data dependent jitter	<=18	15	ps	
Total uncorrelated Jitter	<=31.25	24.9	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	5.7	ps	
Total uncorrelated PWJ	<=24	20.9	ps	
			F~	
Gen 3 (P8)				
Uncorrelated deterministic jitter	<=12	(12.1)	ps	
Data dependent jitter	<=18	14	ps	
Total uncorrelated Jitter	<=31.25	29.3	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	9.8	ps	
Total uncorrelated PWJ	<=24	24	ps	
			Γ	
Gen 3 (P9)	7			
Uncorrelated deterministic jitter	<=12	6.3	ps	
Data dependent jitter	<=18	10.5	ps	
Total uncorrelated Jitter	<=31.25	25.9	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	6.6	ps	
Total uncorrelated PWJ	<=24	22.9	ps	
			_	
Gen 3 (P10)		1		
Uncorrelated deterministic jitter	<=12	9.3	ps	
Data dependent jitter	<=18	17	ps	
Total uncorrelated Jitter	<=31.25	30.2	ps	
Deterministic (DjDD) uncorrelated PWJ	<=10	9.4	ps	
Total uncorrelated PWJ	<=24	23.9	ps	
			1	

Test/Parameter	Valid Range	Measured	Units	Figure
Test 1.5: Eye Width (Gen 2 and 3 only)				
Gen 2 (-3.5 dB)	>=750	802	mUI	
Gen 2 (-6.0 dB)	>=750	795	mUI	
Gen 3 (P0)	>=41.25	50.2	ps	
Gen 3 (P1)	>=41.25	49.6	ps	
Gen 3 (P2)	>=41.25	43.4	ps	
Gen 3 (P3)	>=41.25	42.3	ps	
Gen 3 (P4)	>=41.25	40.7	ps	
Gen 3 (P5)	>=41.25	41.75	ps	
Gen 3 (P6)	>=41.25	44.9	ps	
Gen 3 (P7)	>=41.25	48.6	ps	
Gen 3 (P8)	>=41.25	51.2	*	
Gen 3 (P9)	>=41.25	53.8	ps	
Gen 3 (P10)	>=41.25		ps	
Gell 3 (P10)	>=41.23	47.6	ps	
Test 1.6: Eye Height (Gen 2 and 3 only)	A	200.4	X7	
Gen 2 (-3.5 dB)	-	200.4	mV	
Gen 2 (-6.0 dB)	-	198.6	mV	
Gen 3 (P0)	-	194.3	mV	
Gen 3 (P1)	-	195.2	mV	
Gen 3 (P2)	-	197.8	mV	
Gen 3 (P3)	-	194.9	mV	
Gen 3 (P4)	-	188.7	mV	
Gen 3 (P5)	-	190.2	mV	
Gen 3 (P6)	-	193.8	mV	
Gen 3 (P7)	-	194.8	mV	
Gen 3 (P8)	-	197.6	mV	
Gen 3 (P9)	-	199.9	mV	
Gen 3 (P10)	-	202.3	mV	
Test 1.6 Eye Mask				
Gen 1	-	Pass		2
Gen 2 (-3.5 dB)	-	Pass		3
Gen 2 (-6.0 dB)	-	Pass		4
Gen 3 (P0)	-	Pass		5
Gen 3 (P1)	-	Pass		6
Gen 3 (P2)	-	Pass		7
Gen 3 (P3)	_	Pass		8
Gen 3 (P4)	_	Pass		9
Gen 3 (P5)	-	Pass		10
Gen 3 (P6)	-	Pass		11
Gen 3 (P7)	-	Pass		12
Gen 3 (P8)	-	Pass		13
Gen 3 (P9)	-	Pass		14
Gen 3 (P10)	_	Pass		15
(110)		1 433		13

Table 3: Clocking and SSC Test Results

Slot x, Lane y

Slot x, Lane y	V-11 D	Manageria	TT Mar	TO!
Test/Parameter	Valid Range	Measured	Units	Figure
Test 2.1: TX UI Period				
UI Period at 2.5 GT/s	399.88/400.12	400	ps	
UI Period at 5.0 GT/s	199.94/200.06	200	ps	
UI Period at 8.0 GT/s	124.9625/	125	ps	
	125.0375			
Test 2.2: Reference Clock Frequency (Platform only)				
Reference Clock Frequency (No SSC)	99.97/100.03	100.02	MHz	
			•	
Test 2.3: TX SSC Modulation Frequency				
Frequency of SSC modulation at 5 GT/s	30/33	31.2	kHz	16
Frequency of SSC modulation at 8 GT/s	30/33	31.3	kHz	17
Test 2.4: TX SSC Modulation Deviation and Balance				
5GT/s				
Average upper SSC peak value:	< 0	(34.8)	ppm	16
Average lower SSC peak value:	> -5000	-1931.6	ppm	16
8GT/s				
Average upper SSC peak value:	< 0	(25.1)	ppm	17
Average lower SSC peak value:	> -5000	-1930.5	ppm	17
Test 2.5: TX SSC dF/dt (Informative)				
Peak dF/dt at 5 GT/s	1250	194	ppm/us	18
Peak dF/dt at 8 GT/s	1250	186	ppm/us	19



Table 4: TX NRZ Data Signaling Test Results

Slot x, Lane v

Slot X, Lane y				
Test/Parameter	Valid Range	Measured	Units	Figure
Test 2.1: TX Differential Voltage (p-p) (Informative)				
Differential Swing at 2.5 GT/s	800/1200	1154	mV_{PP}	2
Differential Swing at 5.0 GT/s	800/1200	1194	mV_{PP}	3
Differential Swing at 8.0 GT/s	800/1300	1202	mV_{PP}	9
Test 2.2: TX AC Common Mode Voltage (p-p)				
(Informative)				
AC Common Mode Voltage at 2.5 GT/s	0/20*	7.9	mV_{PP}	
AC Common Mode Voltage at 5.0 GT/s	0/150	5.3	mV_{PP}	
AC Common Mode Voltage at 8.0 GT/s	0/150	6.9	mV_{PP}	
Test 2.3: TX DC Common Mode Voltage				
DC Common Mode Voltage at 2.5 GT/s	0/3.6	1.2E-6	V	
DC Common Mode Voltage at 5.0 GT/s	0/3.6	0.2E-6	V	
DC Common Mode Voltage at 8.0 GT/s	0/3.6	1.3E-6	V	
_		\		
Test 2.4: TX Intra Pair Skew (Informative)				
Skew at 2.5 GT/s	-	3	ps	
Skew at 5.0 GT/s	-	3.1	ps	
Skew at 8.0 GT/s	7	2.9	ps	

^{*}This test is defined to the peak, not peak to peak (p-p)



Table 5: Gen 3 Equalization Results

Slot x, Lane y

Preset	Vb (mV)	De-emphasis (dB)	Preshoot (dB)	CP
P0	414.09	0.00	-6.73	0
P1	593.33	0.00	-3.60	1
P2	514.21	0.00	-4.85	2
Р3	671.25	0.00	-2.53	3
P4	898.56	0.00	0.00	4
P5	748.32	1.59	0.00	5
P6	703.16	2.13	0.00	6
P7	333.10	3.77	-7.03	7
P8	448.79	3.50	-3.90	8
P9	625.61	3.14	0.00	9
P10	273.90	0.00	-10.32	10

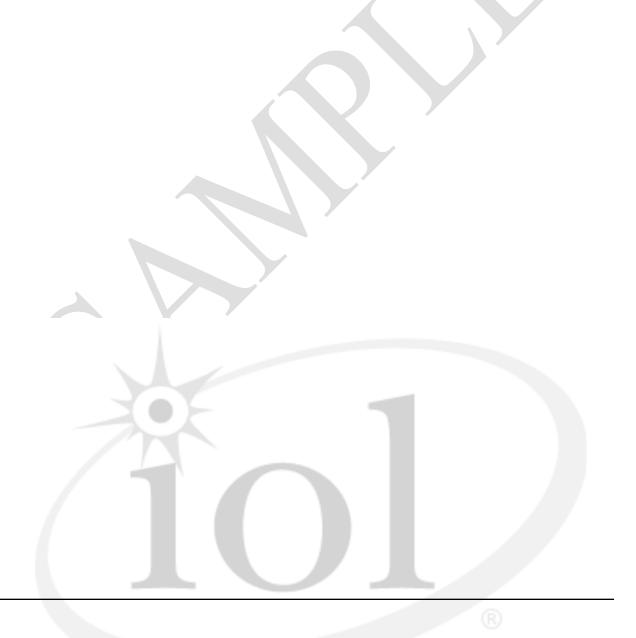
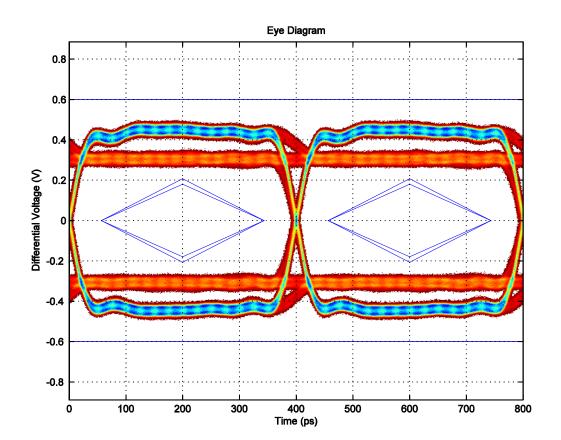


Figure 2: Gen 1 Eye Diagram





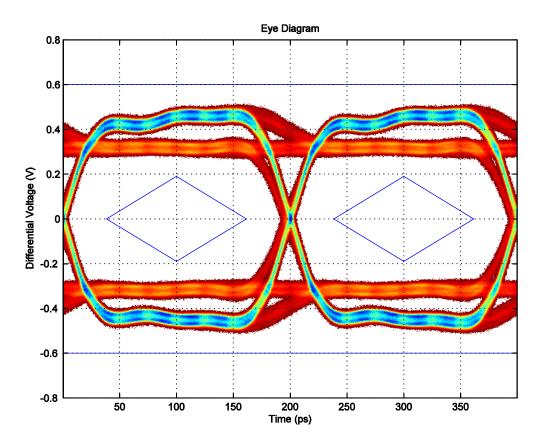


Figure 3: Gen 2 (-3.5 dB) Eye Diagram



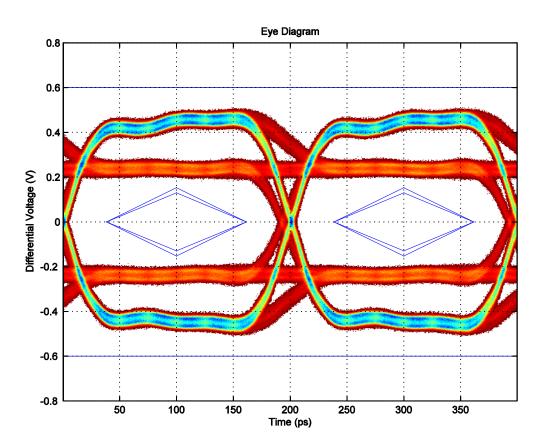


Figure 4: Gen 2 (-5 dB) Eye Diagram



Figure 5: Gen 3 P0 Eye Diagram

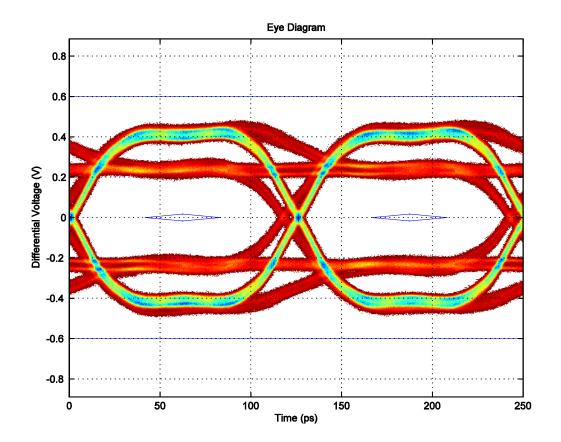




Figure 6: Gen 3 P1 Eye Diagram

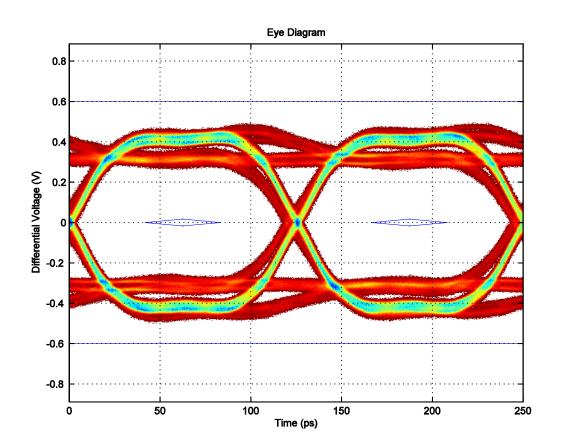




Figure 7: Gen 3 P2 Eye Diagram

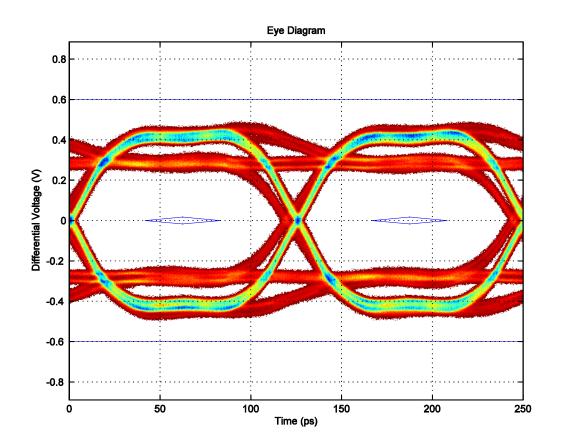




Figure 8: Gen 3 P3 Eye Diagram

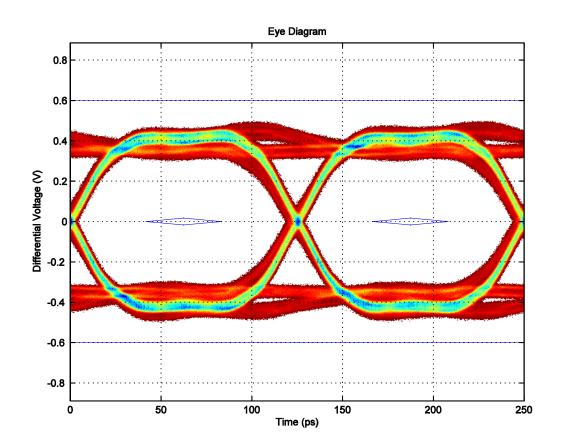




Figure 9: Gen 3 P4 Eye Diagram

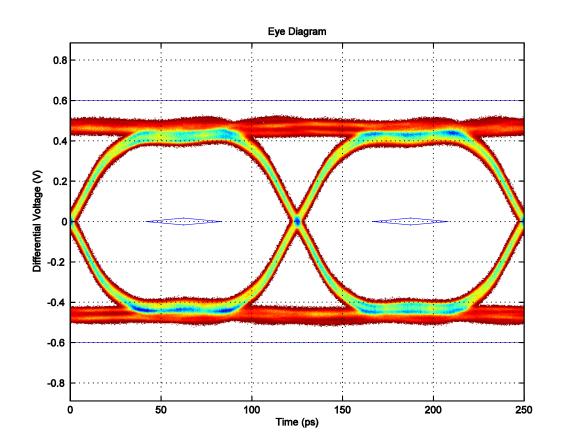




Figure 10: Gen 3 P5 Eye Diagram

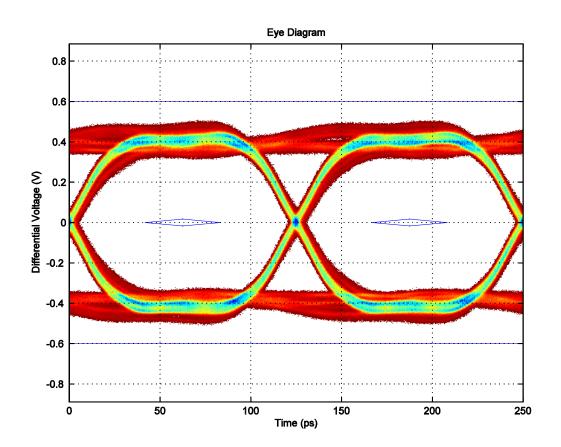




Figure 11: Gen 3 P6 Eye Diagram

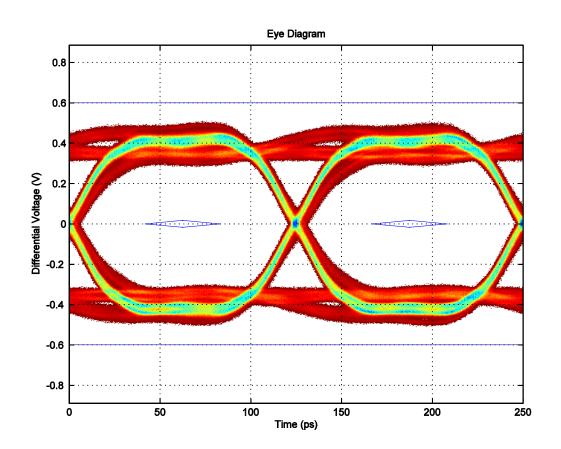


Figure 12: Gen 3 P7 Eye Diagram

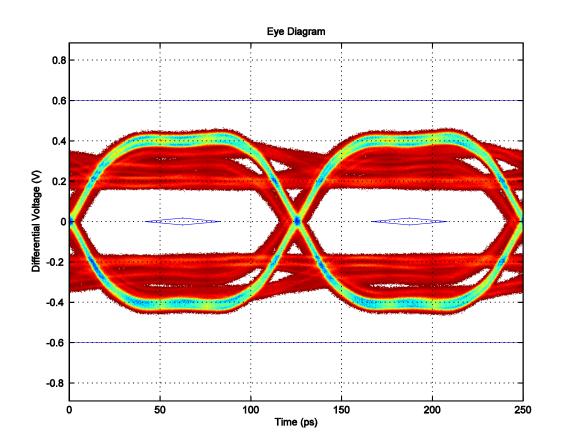
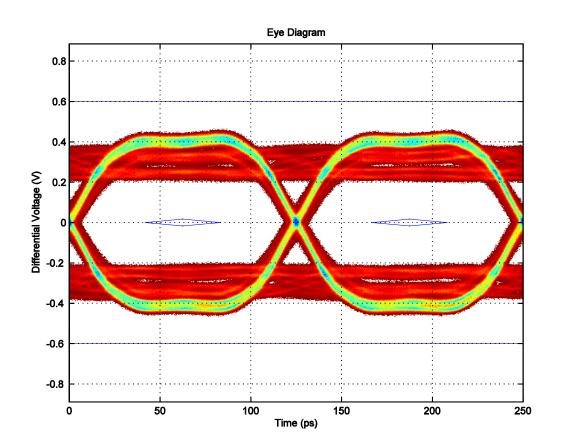


Figure 13: Gen 3 P8 Eye Diagram





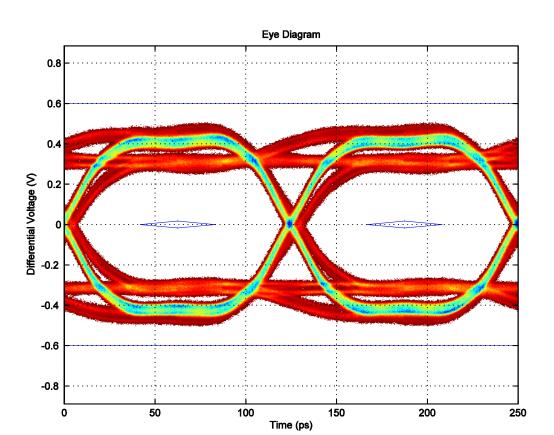


Figure 14: Gen 3 P9 Eye Diagram



Figure 15: Gen 3 P10 Eye Diagram

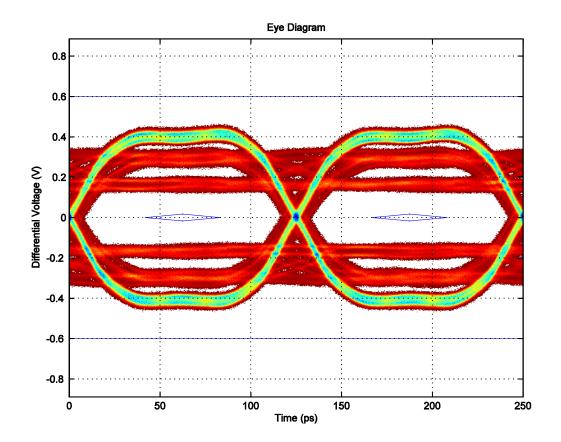
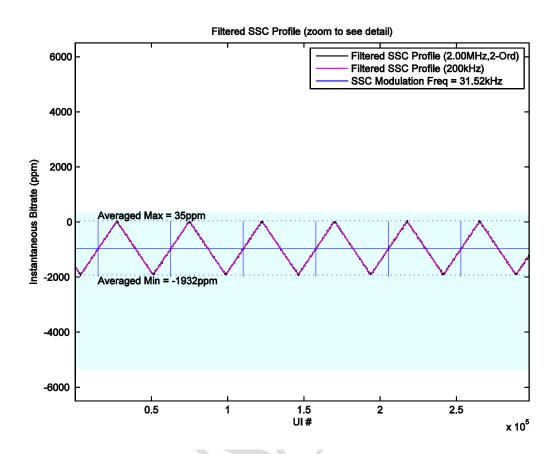




Figure 16: Gen 2 SSC Profile





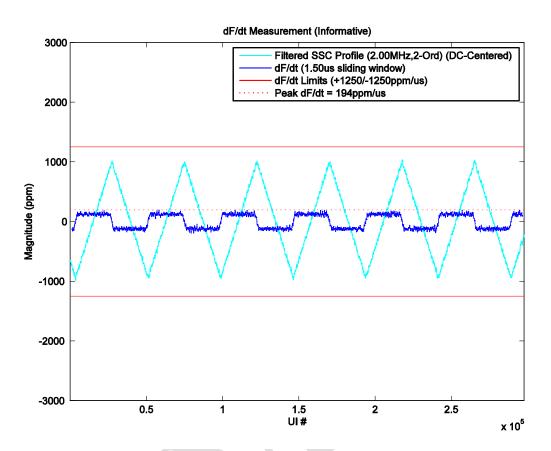


Figure 17: Gen 2 SSC dF/dt



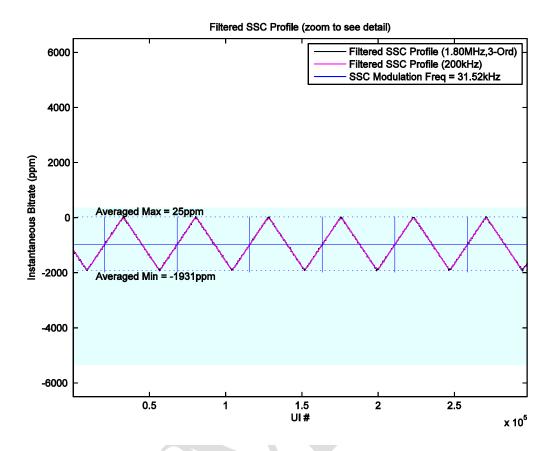


Figure 18: Gen 3 SSC Profile



Figure 19: Gen 3 SSC dF/dt

