UNH IOL PCIe Consortium

PCIe Gen 3 CEM Receiver Testing

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January 24, 2014

Mr. Vendor
Company Name
Address

Mr. Vendor:

Enclosed are the results from the PCIe Gen 3 CEM Receiver testing performed on the:

20140106 UNHID Company DUT PCIe Gen 3 Platform/AIC

The testing was performed according to Version 0.91 of the PCI Sig, PCI Express 3.0 CEM RX Physical Layer Test Method of Implementation for Agilent J-BERT N4903B High Performance Serial BERT, which is available online at:

http://www.pcisig.com/members/downloads/specifications/Agilent_PCIe_3.0_8G_RX_MOI_v0_91.pdf

Note that the tests defined in this test suite are based on:
PCI Express Base Specification Revision 3.0, version 1.0
PCI Express Card Electromechanical Specification Revision 3.0, version 0.9
PCI Express® Architecture PHY Test Specification Revision 3.0, Ver. 0.9

Please feel free to contact me at jbeaudet@iol.unh.edu if you have any questions regarding the test suite, or the results contained in this report.

Sincerely,

Joshua E. Beaudet

Joshua Beaudet

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Table 1: Test Equipment and DUT Configuration/Feature Information

DUT Details	
Manufacturer	
Model	
Device Type (Platform/AIC)	
Mfr. Serial Number	
BIOS Version	
Hardware Version	
Software Version	
UNH-IOL ID Number	
Processor Details (If applicable)	
Spec	
Lot Information	
Manufacture Location	
Lot Numbers	
Test System Hardware	
Real-time DSO (for Calibration)	Agilent Infiniium DSO91304A, 13GHz, 40GS/s Real-time DSO
Bit Error Tester/ Pattern Generator	Agilent J-BERT N4903B, 12.5Gb/s, High Performance Serial BERT
De-Emphasis Box	Agilent N4916B De-Emphasis Signal Converter
Clock Multiplier	Agilent N4880A Reference Clock Multiplier
Repeater	National Semiconductor/TI DS80PCIEVK REV.1
Test Fixture	PCI Sig PCIe x16 Compliance Load Board
Additional Comments/Notes	
The testing was performed without the Repeater as it was not needed.	

Figure 1: Test Setup
Note: The Reference Clock Multiplier is not pictured. That box takes the clock from the CLB and puts out a reference clock that feeds the clock in on the Error Detector of the J-BERT.

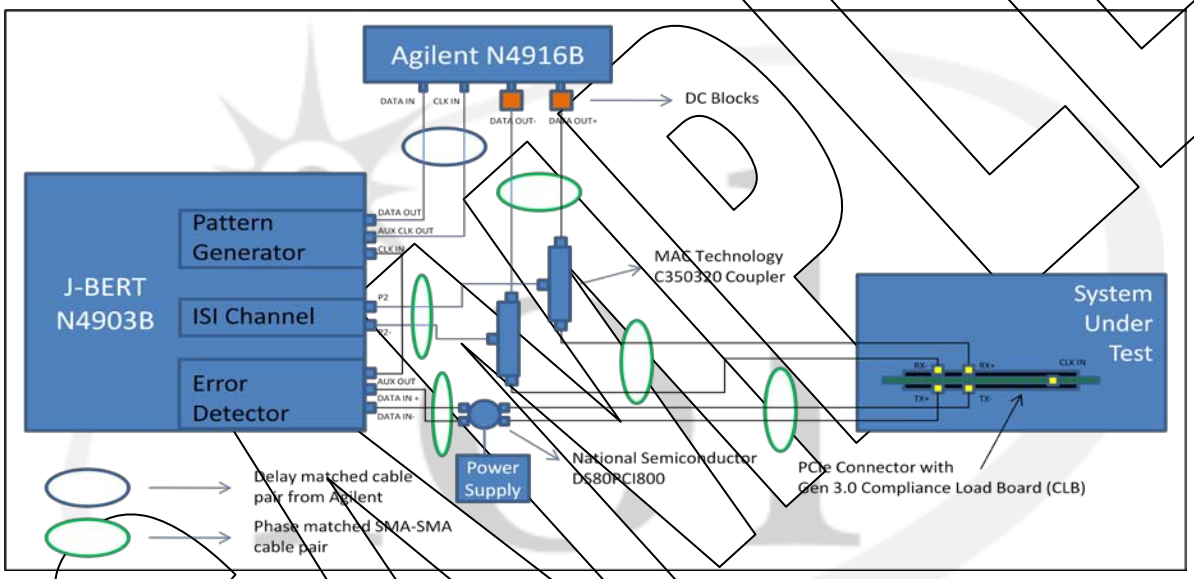

Table 2: Test Results

Slot	Lane	Errors	Bit Count	BER	Result
1	0	0	3.01681692E12	0	Pass
1	7	0	3.01649533E12	0	Pass
1	15	0	3.01631390E12	0	Pass
2	0	0	3.01679100E12	0	Pass
2	7	0	3.01725552E12	0	Pass
2	15	0	3.01705414E12	0	Pass
3	0	0	3.01382083E12	0	Pass
3	7	0	3.01422731E12	0	Pass
3	15	0	3.01409973E12	0	Pass
4	0	0	3.01335704E12	0	Pass
4	7	0	3.01332195E12	0	Pass
4	15	0	3.01333870E12	0	Pass
5	0	0	3.01644679E12	0	Pass
5	7	0	3.01644679E12	0	Pass
5	15	0	3.01421346E12	0	Pass
6	0	0	3.01372464E12	0	Pass
6	7	2	3.01357117E12	6.6366E-13	Pass
6	15	0	3.01369993E12	0	Pass
7	0	0	3.01103704E12	0	Pass
7	7	0	3.01402182E12	0	Pass
7	15	0	3.01409973E12	0	Pass
8	0	0	3.01304817E12	0	Pass
8	7	0	3.01304918E12	0	Pass
8	15	4	3.01304727E12	1.3276E-6	Fail