UNH-IOL MIPI Alliance Test Program
D-PHY TX Conformance Test Report

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September 27, 2010

Engineer Name
Sample Company, Inc.
1010 Mobile Way
San Jose, CA 95101

Mr. Engineer:

Enclosed are the test results from the D-PHY TX Physical Layer Conformance testing performed on the:

Sample Company 1234 Camera Sensor 1-Lane CSI-2 Transmitter

The testing was performed according to v0.98 of the MIPI Alliance D-PHY Conformance Test Suite, which is available to MIPI Alliance Members at:

https://members.mipi.org/mipi-testing/workspace/StartPage

Also note that most of the measurements in this report were performed on captured DSO waveform data using the freely available DPHYGUI physical layer conformance software tool, which is available to all MIPI members, and may be downloaded at the URL above. The raw waveform data files used for this report may be obtained upon request, if duplication of results or further analysis of the data is desired. (Contact UNH IOL for assistance.)

Any conformance failures observed during testing are listed below:

- **NO CONFORMANCE ISSUES WERE OBSERVED DURING TESTING**

Please feel free to contact me via email at aab@iol.unh.edu with any questions you may have regarding this report.

Sincerely,

Andy Baldman

Digitally signed by UNH-IOL
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Table 1-0: Test Setup and DUT Configuration Information

DUT Details	
Week testing was performed	20100927
Manufacturer	Sample Company
Model	1234 Camera Sensor
Max. Supported HS Bit Rate	800 Mbps
Mfr. Serial Number	9876543210
Firmware Version	v1.0
Hardware Version	v0.10
Software Version	3.15
UNH-IOL ID Number	99999
Test System Hardware	
Real-time DSO	Agilent Infiniium DSA91304A, 13GHz, 40GS/s Real-time DSO, with four Agilent 1169A InfiniiMax 12GHz Differential Probes
Termination Fixture	UNH-IOL D-PHY Reference Termination Board (RTB) v2.0
Additional Comments/Notes	
Testing was performed on Clock Lane and Data Lane 0. (Results for Data Lanes 1, 2, and 3 are reported as Not Applicable (N/A), as the DUT does not implement these Lanes.)	

Table 1-1: (Section 1, Group 1): Data Lane LP-TX Signaling Requirements:

Test/Parameter	Conformance Range	Lane 0 Measured	Lane 1 Measured	Lane 2 Measured	Lane 3 Measured	Units	Fig.
Test 1.1.1: Data Lane LP-TX Thevenin Output High Level Voltages (V_{OH})							
Measured V_{OH} for V_{DP} (50pF C_{LOAD}):	1100 / 1300	**1178.2**	N/A	N/A	N/A	mV	1
Measured V_{OH} for V_{DN} (50pF C_{LOAD}):	1100 / 1300	**1185.4**	N/A	N/A	N/A	mV	2
Measured V_{OH} for V_{DP} (No C_{LOAD}):	1100 / 1300	**1177.1**	N/A	N/A	N/A	mV	3
Measured V_{OH} for V_{DN} (No C_{LOAD}):	1100 / 1300	**1180.3**	N/A	N/A	N/A	mV	4
Test 1.1.2: Data Lane LP TX Thevenin Output Low Level Voltages (V_{OL})							
Measured V_{OL} for V_{DP} (50pF C_{LOAD}):	-50 / +50	**-5.0**	N/A	N/A	N/A	mV	1
Measured V_{OL} for V_{DN} (50pF C_{LOAD}):	-50 / +50	**-5.1**	N/A	N/A	N/A	mV	2
Measured V_{OL} for V_{DP} (No C_{LOAD}):	-50 / +50	**-6.3**	N/A	N/A	N/A	mV	3
Measured V_{OL} for V_{DN} (No C_{LOAD}):	-50 / +50	**-5.7**	N/A	N/A	N/A	mV	4
Test 1.1.3: Data Lane LP TX 15%-85% Rise Time (T_{RLP})							
Measured T_{RLP} for V_{DP} (50pF C_{LOAD}):	< 25	**13.5**	N/A	N/A	N/A	ns	5
Measured T_{RLP} for V_{DN} (50pF C_{LOAD}):	< 25	**13.8**	N/A	N/A	N/A	ns	6
Measured T_{RLP} for V_{DP} (No C_{LOAD}):	< 25	**10.3**	N/A	N/A	N/A	ns	7
Measured T_{RLP} for V_{DN} (No C_{LOAD}):	< 25	**10.3**	N/A	N/A	N/A	ns	8
Test 1.1.4: Data Lane LP TX 15%-85% Fall Time (T_{FLP})							
Measured T_{FLP} for V_{DP} (50pF C_{LOAD}):	< 25	**11.7**	N/A	N/A	N/A	ns	9
Measured T_{FLP} for V_{DN} (50pF C_{LOAD}):	< 25	**11.6**	N/A	N/A	N/A	ns	10
Measured T_{FLP} for V_{DP} (No C_{LOAD}):	< 25	**11.1**	N/A	N/A	N/A	ns	11
Measured T_{FLP} for V_{DN} (No C_{LOAD}):	< 25	**10.8**	N/A	N/A	N/A	ns	12
Test 1.1.5: Data Lane LP TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)							
V_{DP} (Falling Edges, C_{LOAD} = 50pF):							
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**121.9**	N/A	N/A	N/A	mV/ns	9
MIN $\delta V/\delta t_{SR}$ (400-930mV):	> 30	**60.0**	N/A	N/A	N/A	mV/ns	9
V_{DN} (Falling Edges, C_{LOAD} = 50pF):							
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**113.8**	N/A	N/A	N/A	mV/ns	10
MIN $\delta V/\delta t_{SR}$ (400-930mV):	> 30	**61.1**	N/A	N/A	N/A	mV/ns	10
V_{DP} (Rising Edges, C_{LOAD} = 50pF):							
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**104.8**	N/A	N/A	N/A	mV/ns	5
MIN $\delta V/\delta t_{SR}$ (400-700mV):	> 30	**55.6**	N/A	N/A	N/A	mV/ns	5
MIN $\delta V/\delta t_{SR}$ margin (700-930mV):	> 0	**29.8**	N/A	N/A	N/A	mV/ns	5
V_{DN} (Rising Edges, C_{LOAD} = 50pF):							
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**106.1**	N/A	N/A	N/A	mV/ns	6
MIN $\delta V/\delta t_{SR}$ (400-700mV):	> 30	**57.5**	N/A	N/A	N/A	mV/ns	6
MIN $\delta V/\delta t_{SR}$ margin (700-930mV):	> 0	**31.7**	N/A	N/A	N/A	mV/ns	6

Table 1-1: (Continued)

Test/Parameter	Conformance Range	Lane 0 Measured	Lane 1 Measured	Lane 2 Measured	Lane 3 Measured	Units	Fig.
Test 1.1.6: Data Lane LP TX Pulse Width of Exclusive-OR Clock ($T_{LP-PULSE-TX}$)							
50pF C_{LOAD}, 930mV Trip Level:							
Width of first XOR Clock pulse	> 40	**54.2**	N/A	N/A	N/A	ns	14
Width of last XOR Clock pulse	> 40	**43.0**	N/A	N/A	N/A	ns	14
Min width of all other pulses	> 20	**42.5**	N/A	N/A	N/A	ns	14
50pF C_{LOAD}, 500mV Trip Level:							
Width of first XOR Clock pulse	> 40	**54.8**	N/A	N/A	N/A	ns	15
Width of last XOR Clock pulse	> 40	**55.7**	N/A	N/A	N/A	ns	15
Min width of all other pulses	> 20	**55.4**	N/A	N/A	N/A	ns	15
No C_{LOAD}, 930mV Trip Level:							
Width of first XOR Clock pulse	> 40	**54.3**	N/A	N/A	N/A	ns	17
Width of last XOR Clock pulse	> 40	**45.8**	N/A	N/A	N/A	ns	17
Min width of all other pulses	> 20	**45.6**	N/A	N/A	N/A	ns	17
No C_{LOAD}, 500mV Trip Level:							
Width of first XOR Clock pulse	> 40	**55.1**	N/A	N/A	N/A	ns	18
Width of last XOR Clock pulse	> 40	**56.2**	N/A	N/A	N/A	ns	18
Min width of all other pulses	> 20	**56.1**	N/A	N/A	N/A	ns	18
Test 1.1.7: Data Lane LP TX Period of Exclusive-OR Clock ($T_{LP-PER-TX}$)							
50pF C_{LOAD}, 930mV Trip Level:							
Minimum LP XOR Clock period	> 90	**106.6**	N/A	N/A	N/A	ns	14
50pF C_{LOAD}, 500mV Trip Level:							
Minimum LP XOR Clock period	> 90	**104.8**	N/A	N/A	N/A	ns	15
No C_{LOAD}, 930mV Trip Level:							
Minimum LP XOR Clock period	> 90	**106.8**	N/A	N/A	N/A	ns	17
No C_{LOAD}, 500mV Trip Level:							
Minimum LP XOR Clock period	> 90	**104.3**	N/A	N/A	N/A	ns	18

Table 1-2: (Section 1, Group 2): Clock Lane LP-TX Signaling Requirements:

Test/Parameter	Conformance Range	Clock Lane Measured	Units	Fig.
Test 1.2.1: Clock Lane LP-TX Thevenin Output High Level Voltages (V_{OH})				
Measured V_{OH} for V_{DP} (50pF C_{LOAD}):	1100 / 1300	**1250.5**	mV	-
Measured V_{OH} for V_{DN} (50pF C_{LOAD}):	1100 / 1300	**1254.8**	mV	-
Measured V_{OH} for V_{DP} (No C_{LOAD}):	1100 / 1300	**1198.8**	mV	-
Measured V_{OH} for V_{DN} (No C_{LOAD}):	1100 / 1300	**1240.6**	mV	-
Test 1.2.2: Clock Lane LP TX Thevenin Output Low Level Voltages (V_{OL})				
Measured V_{OL} for V_{DP} (50pF C_{LOAD}):	-50 / +50	**-3.1**	mV	-
Measured V_{OL} for V_{DN} (50pF C_{LOAD}):	-50 / +50	**-5.3**	mV	-
Measured V_{OL} for V_{DP} (No C_{LOAD}):	-50 / +50	**1.4**	mV	-
Measured V_{OL} for V_{DN} (No C_{LOAD}):	-50 / +50	**2.5**	mV	-
Test 1.2.3: Clock Lane LP TX 15%-85% Rise Time (T_{RLP})				
Measured T_{RLP} for V_{DP} (50pF C_{LOAD}):	< 25	**18.7**	ns	-
Measured T_{RLP} for V_{DN} (50pF C_{LOAD}):	< 25	**14.5**	ns	-
Measured T_{RLP} for V_{DP} (No C_{LOAD}):	< 25	**12.7**	ns	-
Measured T_{RLP} for V_{DN} (No C_{LOAD}):	< 25	**12.3**	ns	-
Test 1.2.4: Clock Lane LP TX 15%-85% Fall Time (T_{FLP})				
Measured T_{FLP} for V_{DP} (50pF C_{LOAD}):	< 25	**13.2**	ns	-
Measured T_{FLP} for V_{DN} (50pF C_{LOAD}):	< 25	**11.6**	ns	-
Measured T_{FLP} for V_{DP} (No C_{LOAD}):	< 25	**14.7**	ns	-
Measured T_{FLP} for V_{DN} (No C_{LOAD}):	< 25	**12.8**	ns	-
Test 1.2.5: Clock Lane LP TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)				
V_{DP} (Falling Edges, C_{LOAD} = 50pF):				-
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**135.4**	mV/ns	-
MIN $\delta V/\delta t_{SR}$ (400-930mV):	> 30	**51.2**	mV/ns	-
V_{DN} (Falling Edges, C_{LOAD} = 50pF):				-
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**134.6**	mV/ns	-
MIN $\delta V/\delta t_{SR}$ (400-930mV):	> 30	**63.4**	mV/ns	-
V_{DP} (Rising Edges, C_{LOAD} = 50pF):				-
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**135.4**	mV/ns	-
MIN $\delta V/\delta t_{SR}$ (400-700mV):	> 30	**51.2**	mV/ns	-
MIN $\delta V/\delta t_{SR}$ margin (700-930mV):	> 0	**1.2**	mV/ns	-
V_{DN} (Rising Edges, C_{LOAD} = 50pF):				-
MAX $\delta V/\delta t_{SR}$ (entire edge):	< 150	**134.6**	mV/ns	-
MIN $\delta V/\delta t_{SR}$ (400-700mV):	> 30	**63.4**	mV/ns	-
MIN $\delta V/\delta t_{SR}$ margin (700-930mV):	> 0	**5.6**	mV/ns	-

Table 1-3: (Section 1, Group 3): Data Lane HS-TX Burst Signaling Requirements:

Test/Parameter	Conformance Range (Formula)	Conformance Range (Numeric)	Lane 0 Measured	Lane 1 Measured	Lane 2 Measured	Lane 3 Measured	Units	Fig.
Test 1.3.1: Data Lane HS Entry: T_{LPX} Value								
Measured T_{LPX}	N/A	> 50	**50.81**	N/A	N/A	N/A	ns	19
Test 1.3.2: Data Lane HS Entry: $T_{HS-PREPARE}$ Value								
Measured $T_{HS-PREPARE}$	40ns+4*UI/ 85ns+6*UI	45.00/ 92.50	**64.25**	N/A	N/A	N/A	ns	19
Test 1.3.3: Data Lane HS Entry: $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ Value								
Measured $T_{HS-PREP+ ZERO}$	> 145ns+10*UI	> 157.50	**474.74**	N/A	N/A	N/A	ns	19
Test 1.3.4: Data Lane HS-TX Differential Voltages ($V_{OD(1)}$, $V_{OD(0)}$)								
(Z_{ID}=100): $V_{OD(1)}$	N/A	140 / 270	**202.3**	N/A	N/A	N/A	mV	20
(Z_{ID}=100): $V_{OD(0)}$	N/A	-140 / -270	**-200.0**	N/A	N/A	N/A	mV	21
(Z_{ID}=125): $V_{OD(1)}$	N/A	140 / 270	**222.0**	N/A	N/A	N/A	mV	22
(Z_{ID}=125): $V_{OD(0)}$	N/A	-140 / -270	**-220.5**	N/A	N/A	N/A	mV	23
(Z_{ID}=80): $V_{OD(1)}$	N/A	140 / 270	**182.0**	N/A	N/A	N/A	mV	24
(Z_{ID}=80): $V_{OD(0)}$	N/A	-140 / -270	**-180.4**	N/A	N/A	N/A	mV	25
Test 1.3.5: Data Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})								
(Z_{ID}=100): ΔV_{OD}	N/A	< 10	**2.2**	N/A	N/A	N/A	mV	-
(Z_{ID}=125): ΔV_{OD}	N/A	< 10	**1.5**	N/A	N/A	N/A	mV	-
(Z_{ID}=80): ΔV_{OD}	N/A	< 10	**1.6**	N/A	N/A	N/A	mV	-
Test 1.3.6: Data Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$, $V_{OHHS(DN)}$)								
(Z_{ID}=100): $V_{OHHS(DP)}$	N/A	< 360	**298.3**	N/A	N/A	N/A	mV	26
(Z_{ID}=100): $V_{OHHS(DN)}$	N/A	< 360	**304.7**	N/A	N/A	N/A	mV	27
(Z_{ID}=125): $V_{OHHS(DP)}$	N/A	< 360	**306.4**	N/A	N/A	N/A	mV	28
(Z_{ID}=125): $V_{OHHS(DN)}$	N/A	< 360	**313.3**	N/A	N/A	N/A	mV	29
(Z_{ID}=80): $V_{OHHS(DP)}$	N/A	< 360	**289.0**	N/A	N/A	N/A	mV	30
(Z_{ID}=80): $V_{OHHS(DN)}$	N/A	< 360	**296.3**	N/A	N/A	N/A	mV	31
Test 1.3.7: Data Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)								
(Z_{ID}=100): $V_{CMTX(1)}$	N/A	150 / 250	**203.1**	N/A	N/A	N/A	mV	32
(Z_{ID}=100): $V_{CMTX(0)}$	N/A	150 / 250	**203.4**	N/A	N/A	N/A	mV	32
(Z_{ID}=125): $V_{CMTX(1)}$	N/A	150 / 250	**201.5**	N/A	N/A	N/A	mV	33
(Z_{ID}=125): $V_{CMTX(0)}$	N/A	150 / 250	**202.3**	N/A	N/A	N/A	mV	33
(Z_{ID}=80): $V_{CMTX(1)}$	N/A	150 / 250	**203.0**	N/A	N/A	N/A	mV	34
(Z_{ID}=80): $V_{CMTX(0)}$	N/A	150 / 250	**202.7**	N/A	N/A	N/A	mV	34
Test 1.3.8: Data Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)								
(Z_{ID}=100): $\Delta V_{CMTX(1,0)}$	N/A	< 5	**-0.2**	N/A	N/A	N/A	mV	-
(Z_{ID}=125): $\Delta V_{CMTX(1,0)}$	N/A	< 5	**-0.4**	N/A	N/A	N/A	mV	-
(Z_{ID}=80): $\Delta V_{CMTX(1,0)}$	N/A	< 5	**0.1**	N/A	N/A	N/A	mV	-
Test 1.3.9: Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($V_{CMTX(LF)}$)								
(Z_{ID}=100): $V_{CMTX(LF)}$	N/A	< 25	**8.8**	N/A	N/A	N/A	mVpk	35
Test 1.3.10: Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($V_{CMTX(HF)}$)								
(Z_{ID}=100): $V_{CMTX(HF)}$	N/A	< 15	**4.8**	N/A	N/A	N/A	mV_{RMS}	35
Test 1.3.11: Data Lane HS-TX 20%-80% Rise Time (t_R)								
(Z_{ID}=100): t_R	150 / 0.3*UI	150 / 375.04	**309.4**	N/A	N/A	N/A	ps	36
(Z_{ID}=125): t_R	150 / 0.3*UI	150 / 375.04	**353.3**	N/A	N/A	N/A	ps	37
(Z_{ID}=80): t_R	150 / 0.3*UI	150 / 375.04	**273.2**	N/A	N/A	N/A	ps	38

Test 1.3.12: Data Lane HS-TX 80%-20% Fall Time (t_F)								
(Z_{ID}=100): t_F	150 / 0.3*UI	150 / 375.04	**304.1**	N/A	N/A	N/A	ps	39
(Z_{ID}=125): t_F	150 / 0.3*UI	150 / 375.04	**349.0**	N/A	N/A	N/A	ps	40
(Z_{ID}=80): t_F	150 / 0.3*UI	150 / 375.04	**268.0**	N/A	N/A	N/A	ps	41
Test 1.3.13: Data Lane HS Exit: $T_{HS-TRAIL}$ Value								
(Z_{ID}=100): $T_{HS-TRAIL}$	> 60+4*UI	> 65.00	**65.12**	N/A	N/A	N/A	ns	42
Test 1.3.14: Data Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})								
(Z_{ID}=100): T_{REOT}	N/A	< 35	**16.85**	N/A	N/A	N/A	ns	42
Test 1.3.15: Data Lane HS Exit: T_{EOT} Value								
(Z_{ID}=100): T_{EOT}	< 105+12*UI	< 120.00	**81.97**	N/A	N/A	N/A	ns	42
Test 1.3.16: Data Lane HS Exit: $T_{HS-EXIT}$ Value								
(Z_{ID}=100): $T_{HS-EXIT}$	N/A	> 100	**834**	N/A	N/A	N/A	ns	-

Table 1-4: (Section 1, Group 4): Clock Lane HS-TX Burst Signaling Requirements:

Test/Parameter	Conformance Range (Formula)	Conformance Range (Numeric)	Clock Lane Measured	Units	Fig.
Test 1.4.1: Clock Lane HS Entry: T_{LPX} Value					
Measured T_{LPX}	N/A	> 50	**50.84**	ns	46
Test 1.4.2: Clock Lane HS Entry: $T_{CLK-PREPARE}$ Value					
Measured $T_{CLK-PREPARE}$	N/A	38 / 95	**53.98**	ns	46
Test 1.4.3: Clock Lane HS Entry: $T_{CLK-PREPARE}$+$T_{CLK-ZERO}$ Value					
Measured $T_{CLK-PREP+ ZERO}$	N/A	> 300	**332.61**	ns	46
Test 1.4.4: Clock Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$)					
(Z_{ID}=100): $V_{OD(1)}$	N/A	140/270	**197.3**	mV	47
(Z_{ID}=100): $V_{OD(0)}$	N/A	-140/-270	**-205.3**	mV	48
(Z_{ID}=125): $V_{OD(1)}$	N/A	140/270	**205.1**	mV	49
(Z_{ID}=125): $V_{OD(0)}$	N/A	-140/-270	**-209.6**	mV	50
(Z_{ID}=80): $V_{OD(1)}$	N/A	140/270	**190.1**	mV	51
(Z_{ID}=80): $V_{OD(0)}$	N/A	-140/-270	**-194.9**	mV	52
Test 1.4.5: Clock Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})					
(Z_{ID}=100): ΔV_{OD}	N/A	< 10	**8.0**	mV	-
(Z_{ID}=125): ΔV_{OD}	N/A	< 10	**4.5**	mV	-
(Z_{ID}=80): ΔV_{OD}	N/A	< 10	**4.8**	mV	-
Test 1.4.6: Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$, $V_{OHHS(DN)}$)					
(Z_{ID}=100): $V_{OHHS(DP)}$	N/A	< 360	**315.6**	mV	53
(Z_{ID}=100): $V_{OHHS(DN)}$	N/A	< 360	**318.3**	mV	54
(Z_{ID}=125): $V_{OHHS(DP)}$	N/A	< 360	**313.8**	mV	55
(Z_{ID}=125): $V_{OHHS(DN)}$	N/A	< 360	**316.0**	mV	56
(Z_{ID}=80): $V_{OHHS(DP)}$	N/A	< 360	**306.9**	mV	57
(Z_{ID}=80): $V_{OHHS(DN)}$	N/A	< 360	**309.8**	mV	58
Test 1.4.7: Clock Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)					
(Z_{ID}=100): $V_{CMTX(1)}$	N/A	150/250	**213.9**	mV	59
(Z_{ID}=100): $V_{CMTX(0)}$	N/A	150/250	**213.8**	mV	59
(Z_{ID}=125): $V_{CMTX(1)}$	N/A	150/250	**207.2**	mV	60
(Z_{ID}=125): $V_{CMTX(0)}$	N/A	150/250	**207.9**	mV	60
(Z_{ID}=80): $V_{CMTX(1)}$	N/A	150/250	**209.0**	mV	61
(Z_{ID}=80): $V_{CMTX(0)}$	N/A	150/250	**209.4**	mV	61
Test 1.4.8: Clock Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)					
(Z_{ID}=100): $\Delta V_{CMTX(1,0)}$	N/A	< 5	**0.1**	mV	-
(Z_{ID}=125): $\Delta V_{CMTX(1,0)}$	N/A	< 5	**-0.3**	mV	-
(Z_{ID}=80): $\Delta V_{CMTX(1,0)}$	N/A	< 5	**-0.2**	mV	-
Test 1.4.9: Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($V_{CMTX(LF)}$)					
(Z_{ID}=100): $V_{CMTX(LF)}$	N/A	< 25	**8.6**	mVpk	62
Test 1.4.10: Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($V_{CMTX(HF)}$)					
(Z_{ID}=100): $V_{CMTX(HF)}$	N/A	< 15	**5.4**	mV_{RMS}	62
Test 1.4.11: Clock Lane HS-TX 20%-80% Rise Time (t_R)					
(Z_{ID}=100): t_R	150/0.3*UI	150 / 375.04	**296.9**	ps	63
(Z_{ID}=125): t_R	150/0.3*UI	150 / 375.04	**309.9**	ps	64
(Z_{ID}=80): t_R	150/0.3*UI	150 / 375.04	**289.3**	ps	65

Test 1.4.12: Clock Lane HS-TX 80%-20% Fall Time (t_F)					
(Z_{ID}=100): t_F	150/0.3*UI	150 / 375.04	**306.7**	ps	66
(Z_{ID}=125): t_F	150/0.3*UI	150 / 375.04	**316.8**	ps	67
(Z_{ID}=80): t_F	150/0.3*UI	150 / 375.04	**296.5**	ps	68
Test 1.4.13: Clock Lane HS Exit: $T_{CLK-TRAIL}$ Value					
(Z_{ID}=100): $T_{CLK-TRAIL}$	N/A	> 60	**78.17**	ns	69
Test 1.4.14: Clock Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})					
Clock Lane T_{REOT}	N/A	< 35	**17.27**	ns	69
Test 1.4.15: Clock Lane HS Exit: T_{EOT} Value					
Clock Lane T_{EOT}	< 105+12*UI	< 120.00	**95.43**	ns	69
Test 1.4.16: Clock Lane HS Exit: $T_{HS-EXIT}$ Value					
Clock Lane $T_{HS-EXIT}$	N/A	> 100	**13450**	ns	-
Test 1.4.17: Clock Lane HS Clock Instantaneous (UI_{INST})					
Maximum UI_{INST}	N/A	< 12.5	**1.300**	ns	-

Table 1-5: (Section 1, Group 5): HS-TX Clock-to-Data Lane Timing Requirements

Test/Parameter	Conformance Range (Formula)	Conformance Range (Numeric)	Lane 0 Measured	Lane 1 Measured	Lane 2 Measured	Lane 3 Measured	Units	Fig.
Test 1.5.1: HS Entry: $T_{CLK-PRE}$ Value								
(Z_{ID}=100): $T_{CLK-PRE}$	> 8*UI	> 10.00	**13.23**	N/A	N/A	N/A	ns	19
Test 1.5.2: HS Exit: $T_{CLK-POST}$ Value								
(Z_{ID}=100): $T_{CLK-POST}$	> 60ns+52*UI	> 125.01	**147.56**	N/A	N/A	N/A	ns	42
Test 1.5.3: HS Clock Rising Edge Alignment to First Payload Bit								
First Data Lane payload bit of the HS burst aligns with a rising edge of the HS clock	N/A	Pass/Fail	**PASS**	N/A	N/A	N/A	-	73
Test 1.5.4: Data-to-Clock Skew ($T_{SKEW(TX)}$)								
Maximum observed Data-to-Clock Lane skew	N/A	-150/+150	**141.3**	N/A	N/A	N/A	mUI	74
Minimum observed Data-to-Clock Lane skew	N/A	-150/+150	**27.6**	N/A	N/A	N/A	mUI	74
Mean Data-to-Clock Lane skew (Informative)	N/A	-150/+150	**84.0**	N/A	N/A	N/A	mUI	75

Table 1-6: (Section 1, Group 6): LP-TX INIT, ULPS, and BTA Requirements

Test/Parameter	Conformance Range (Formula)	Conformance Range (Numeric)	Measured	Units	Fig.
Test 1.6.1: INIT: LP-TX Initialization Period ($T_{INIT,MASTER}$)					
(Clock Lane): $T_{INIT,MASTER}$	N/A	> 100	**531.5**	us	-
(Data Lane 0): $T_{INIT,MASTER}$	N/A	> 100	**543.1**	us	-
(Data Lane 1): $T_{INIT,MASTER}$	N/A	> 100	N/A	us	-
(Data Lane 2): $T_{INIT,MASTER}$	N/A	> 100	N/A	us	-
(Data Lane 3): $T_{INIT,MASTER}$	N/A	> 100	N/A	us	-
Test 1.6.2: ULPS Entry: Verification of Clock Lane LP-TX ULPS support					
Verify DUT Clock Lane transmits proper LP-11/10/00 Clock Lane ULPS Entry sequence	N/A	Pass/Fail	**PASS**	-	-
Test 1.6.3: ULPS Exit: Transmitted T_{WAKEUP} Interval					
(Clock Lane): T_{WAKEUP}	N/A	> 1	**1061.5**	ms	-
(Data Lane 0): T_{WAKEUP}	N/A	> 1	**1073.7**	ms	-
(Data Lane 1): T_{WAKEUP}	N/A	> 1	N/A	ms	-
(Data Lane 2): T_{WAKEUP}	N/A	> 1	N/A	ms	-
(Data Lane 3): T_{WAKEUP}	N/A	> 1	N/A	ms	-
Test 1.6.4: BTA: TX-Side T_{TA-GO} Interval Value					
Measured T_{TA-GO}	>= 4*T_{LPX}	>= 203.84	N/A	ns	-
Test 1.6.5: BTA: RX-Side $T_{TA-SURE}$ Interval Value					
Measured $T_{TA-SURE}$	1*T_{LPX} / 2*T_{LPX}	50.96 / 101.92	N/A	ns	-
Test 1.6.6: BTA: RX-Side T_{TA-GET} Interval Value					
Measured T_{TA-GET}	> 5*T_{LPX}	>= 254.80	N/A	ns	-

Figure 1: Dp VOH, VOL Values (Data Lane 0, 50pF CLOAD Test Fixture)

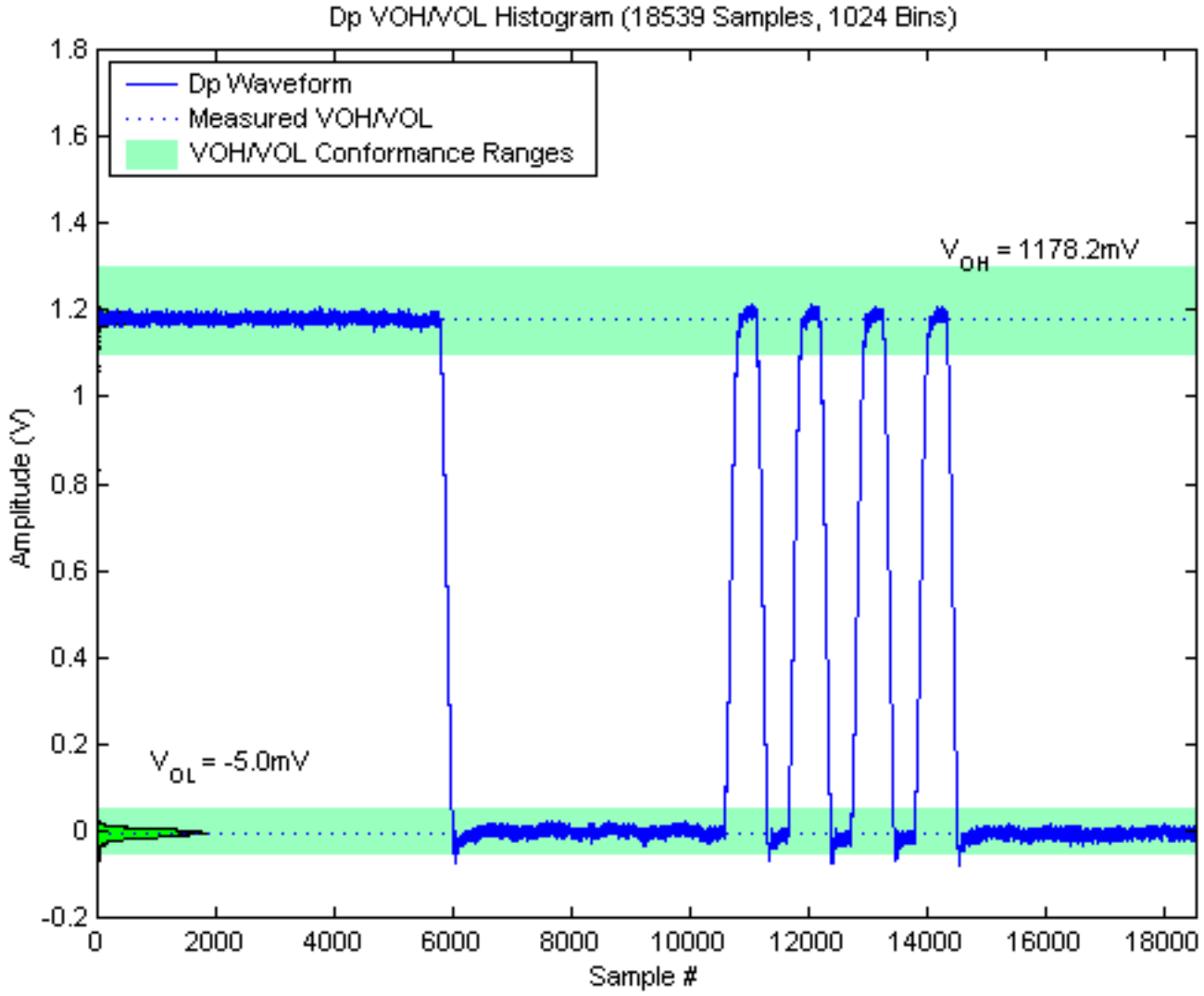

Figure 2: Dp VOH, VOL Values (Data Lane 0, 50pF CLOAD Test Fixture)

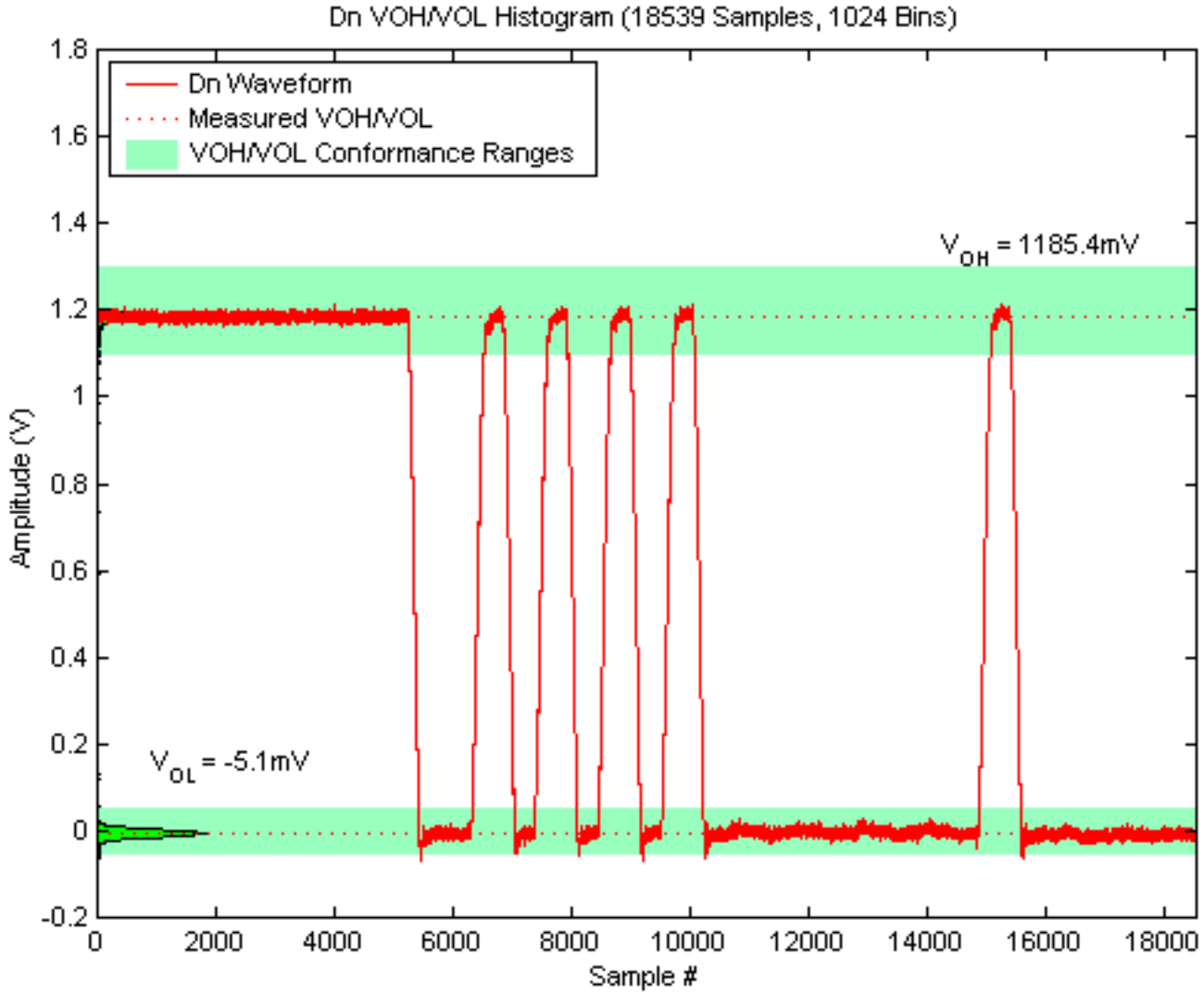

Figure 3: Dp VOH, VOL Values (Data Lane 0, No CLOAD Test Fixture)

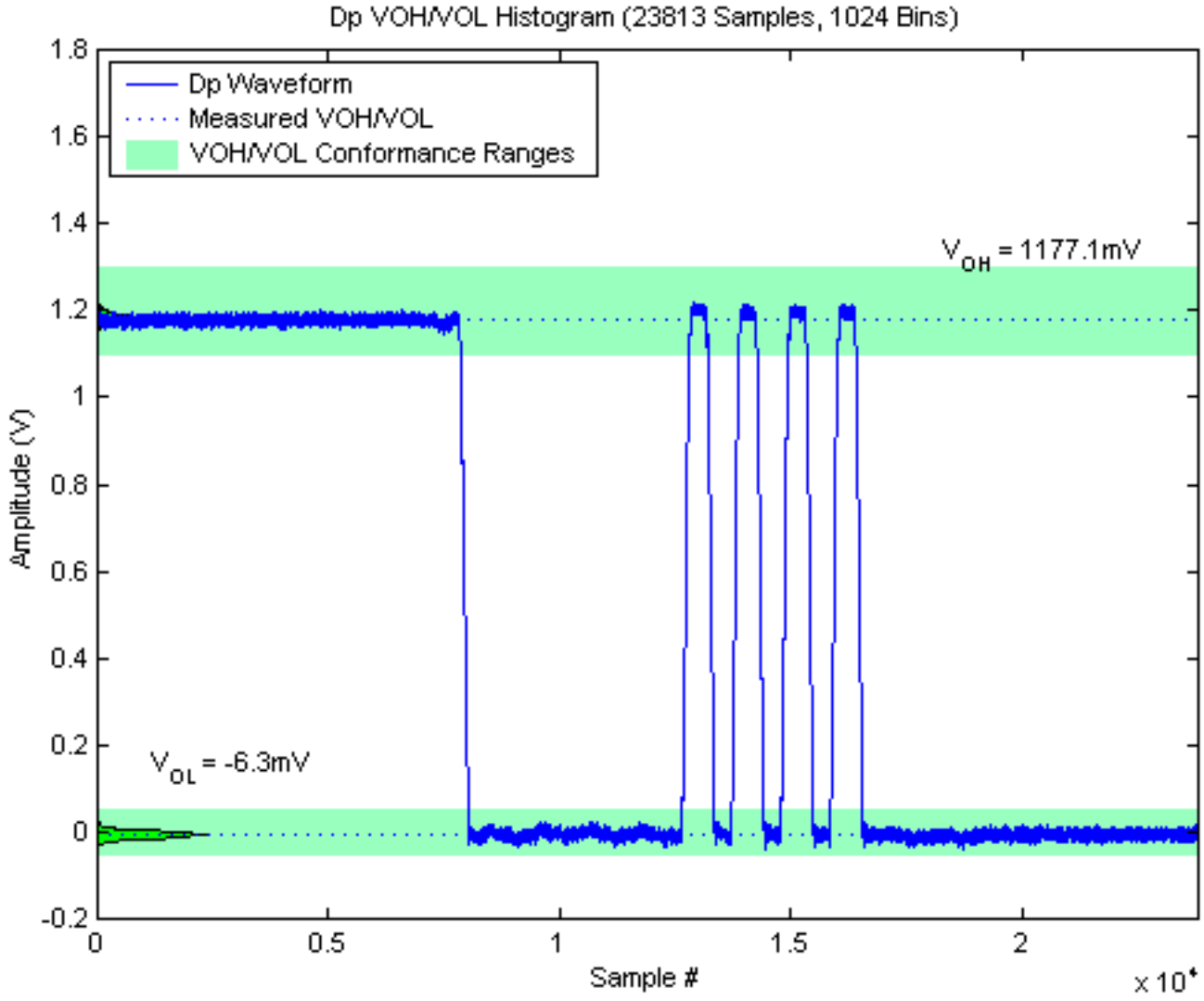

Figure 4: Dp VOH, VOL Values (Data Lane 0, No CLOAD Test Fixture)

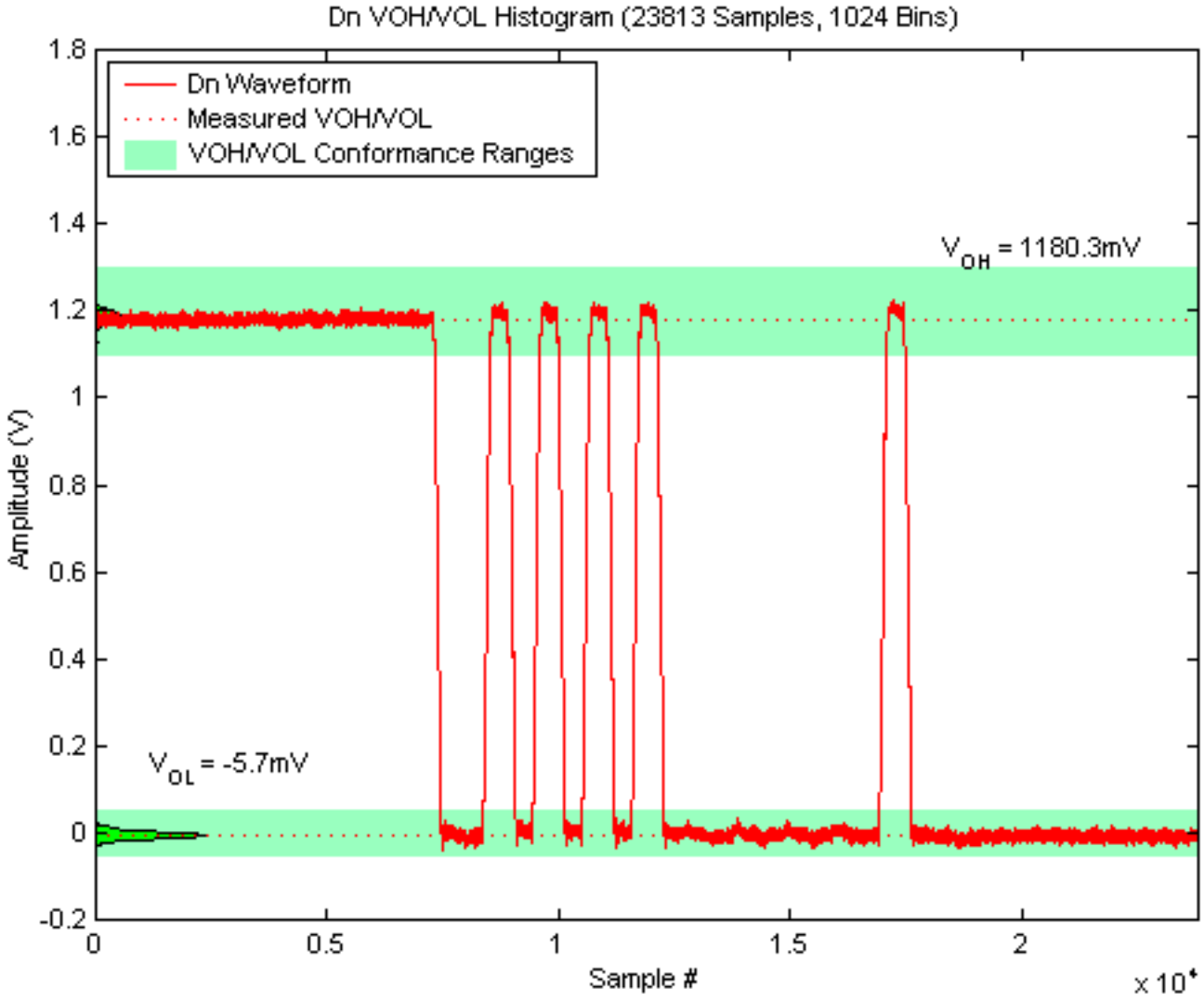

Figure 5: Dp LP-TX Rise Time (Data Lane 0, 50pF CLOAD)

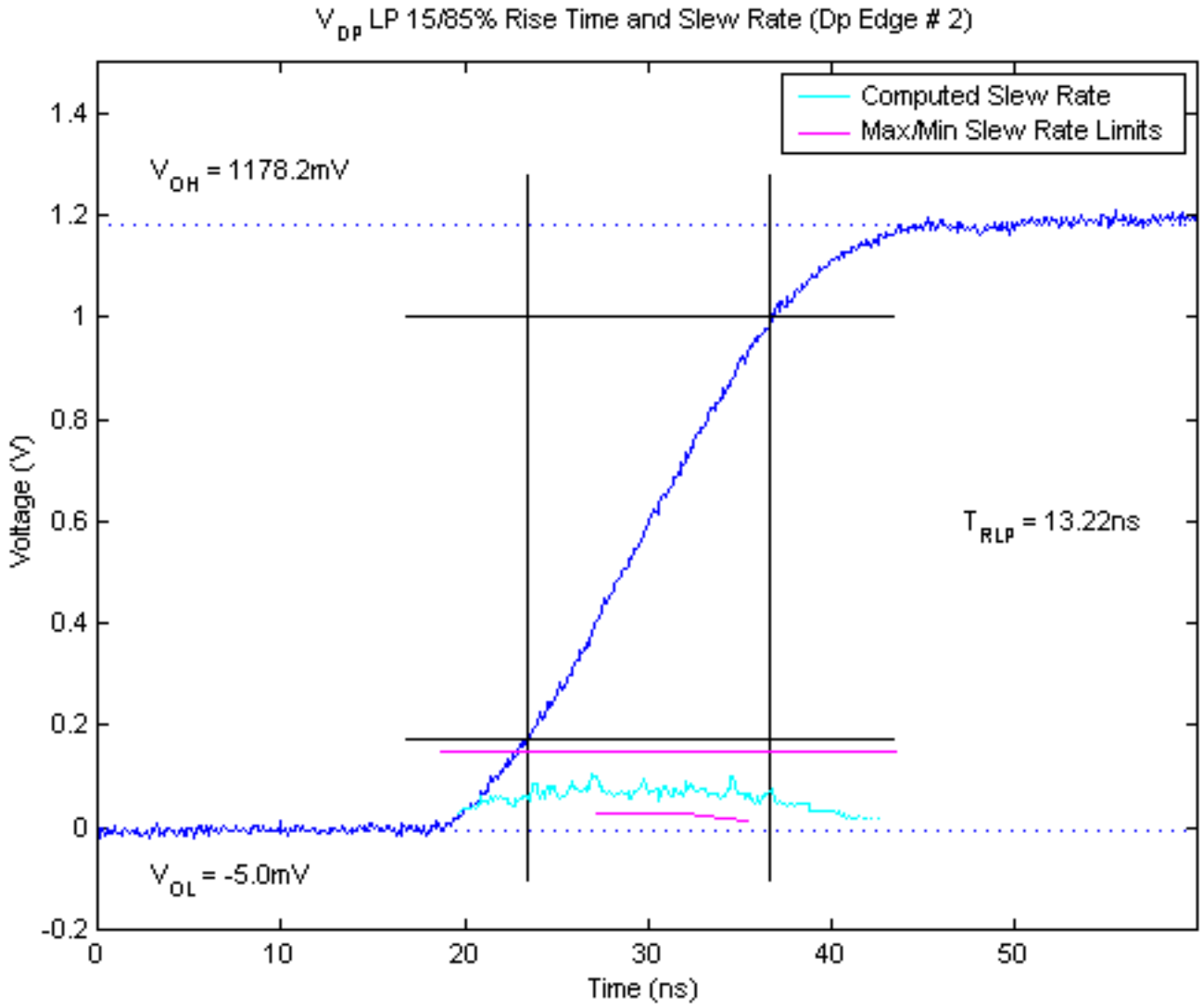

Figure 6: Dn LP-TX Rise Time (Data Lane 0, 50pF CLOAD)

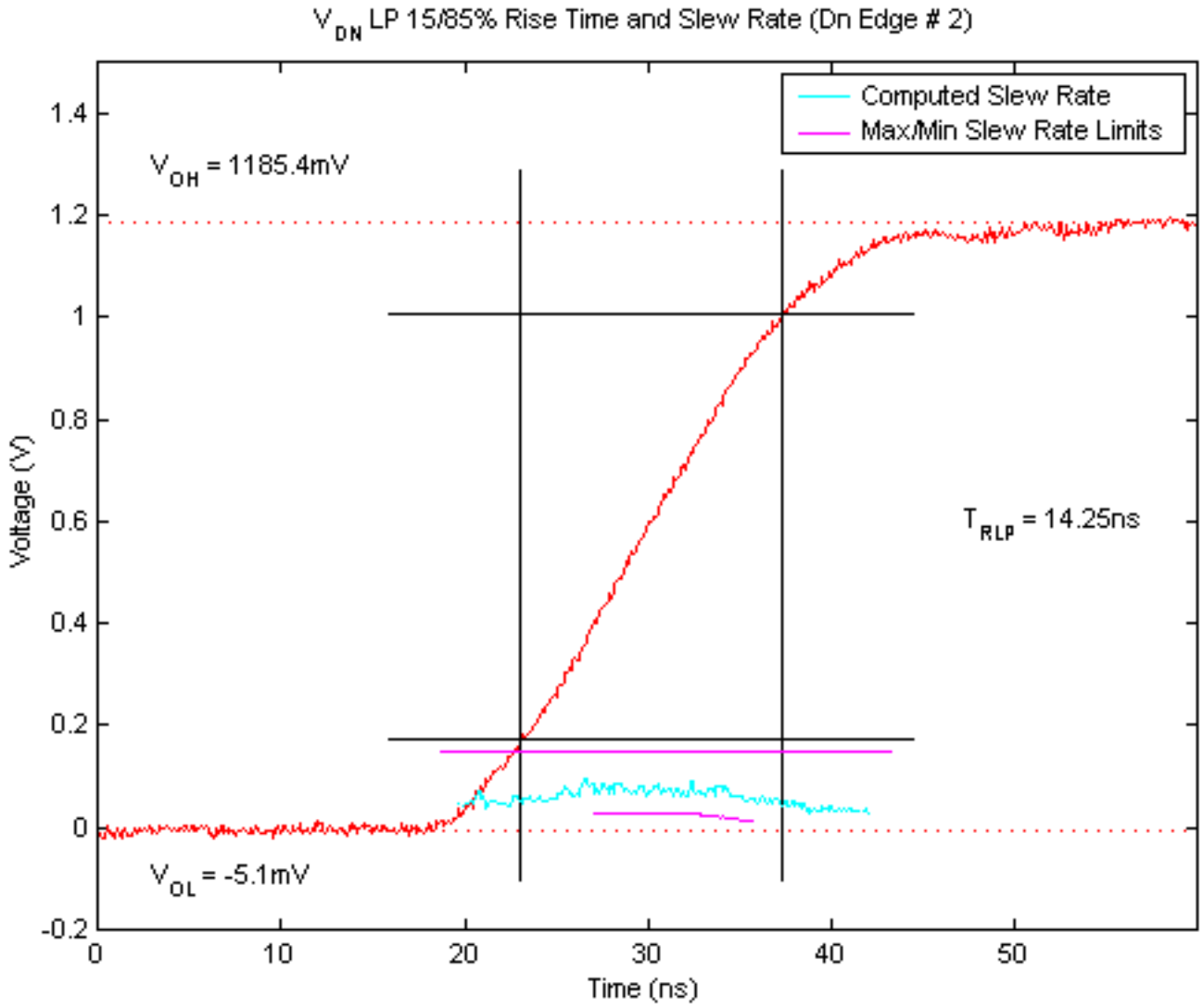

Figure 7: Dp LP-TX Rise Time (Data Lane 0, No CLOAD)

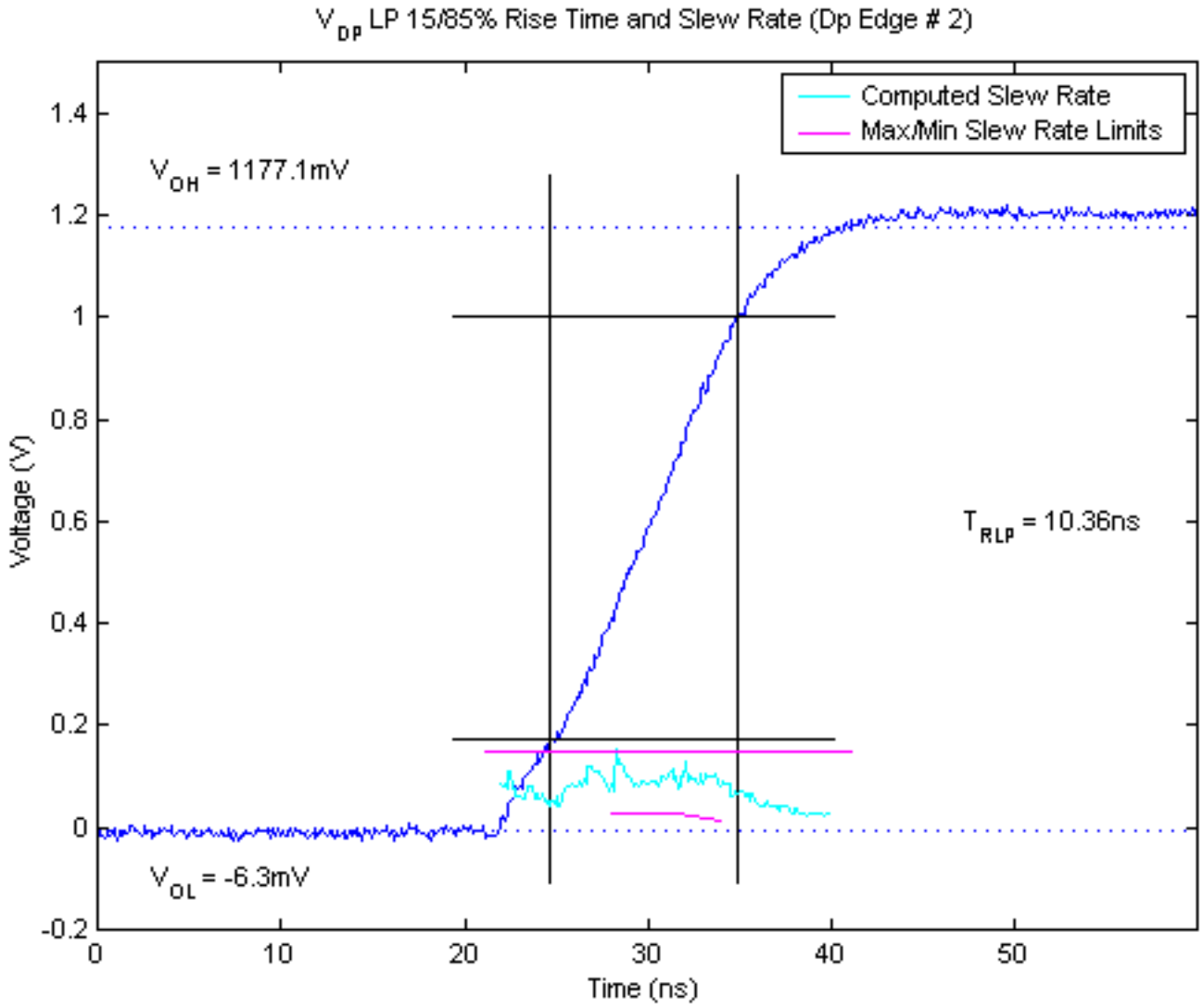

Figure 8: Dn LP-TX Rise Time (Data Lane 0, No CLOAD)

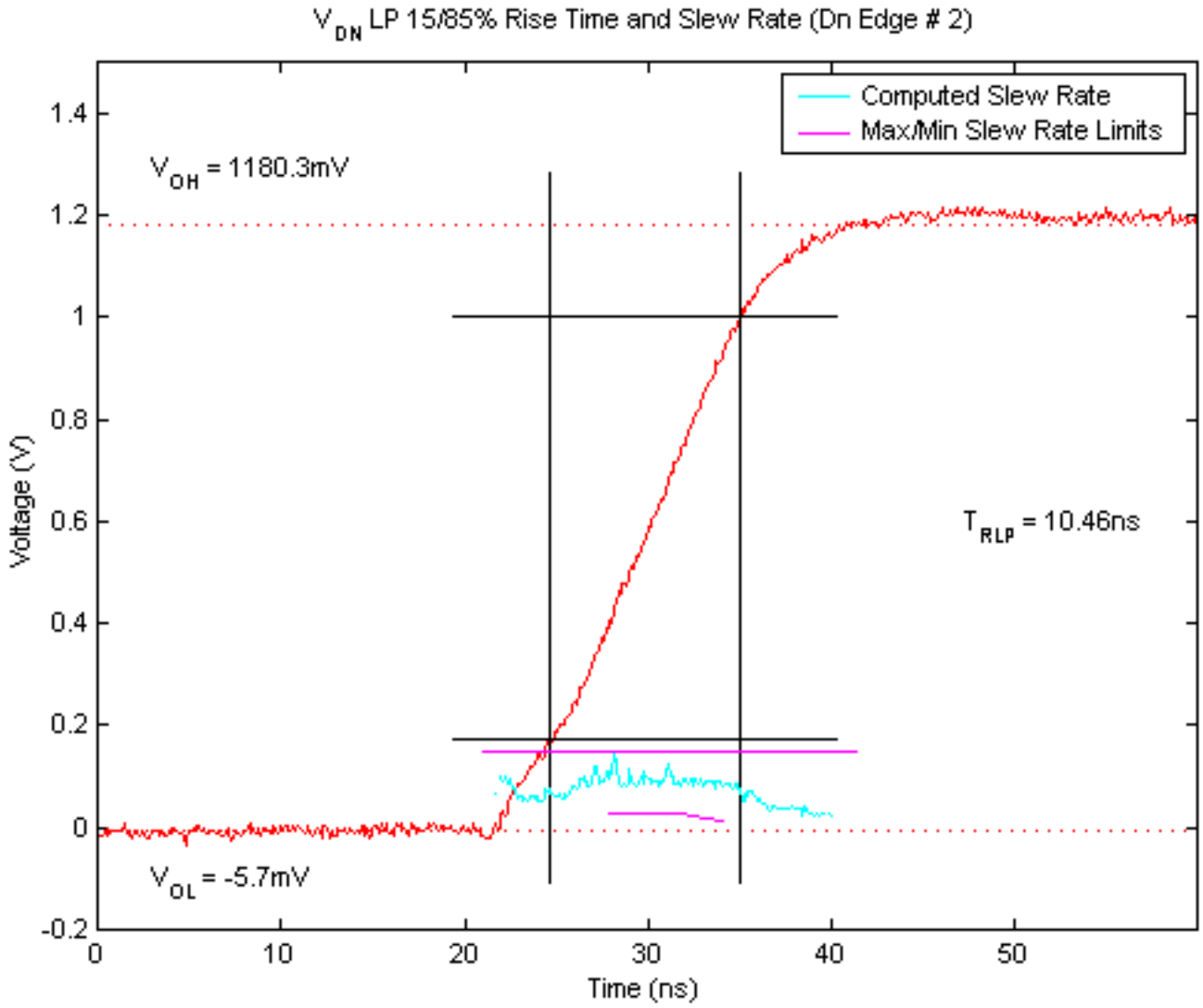

Figure 9: Dp LP-TX Fall Time (Data Lane 0, 50pF CLOAD)

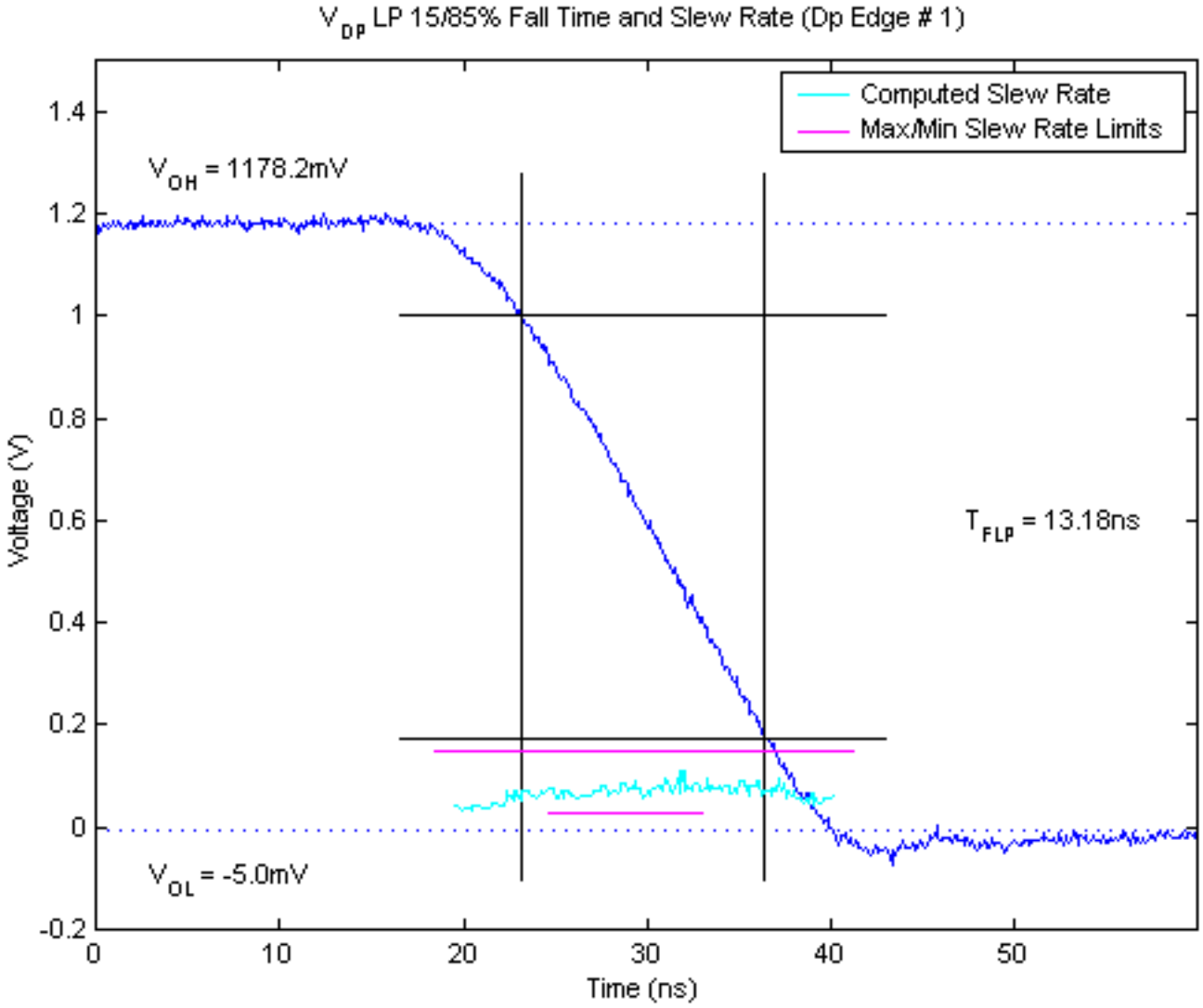

Figure 10: Dn LP-TX Fall Time (Data Lane 0, 50pF CLOAD)

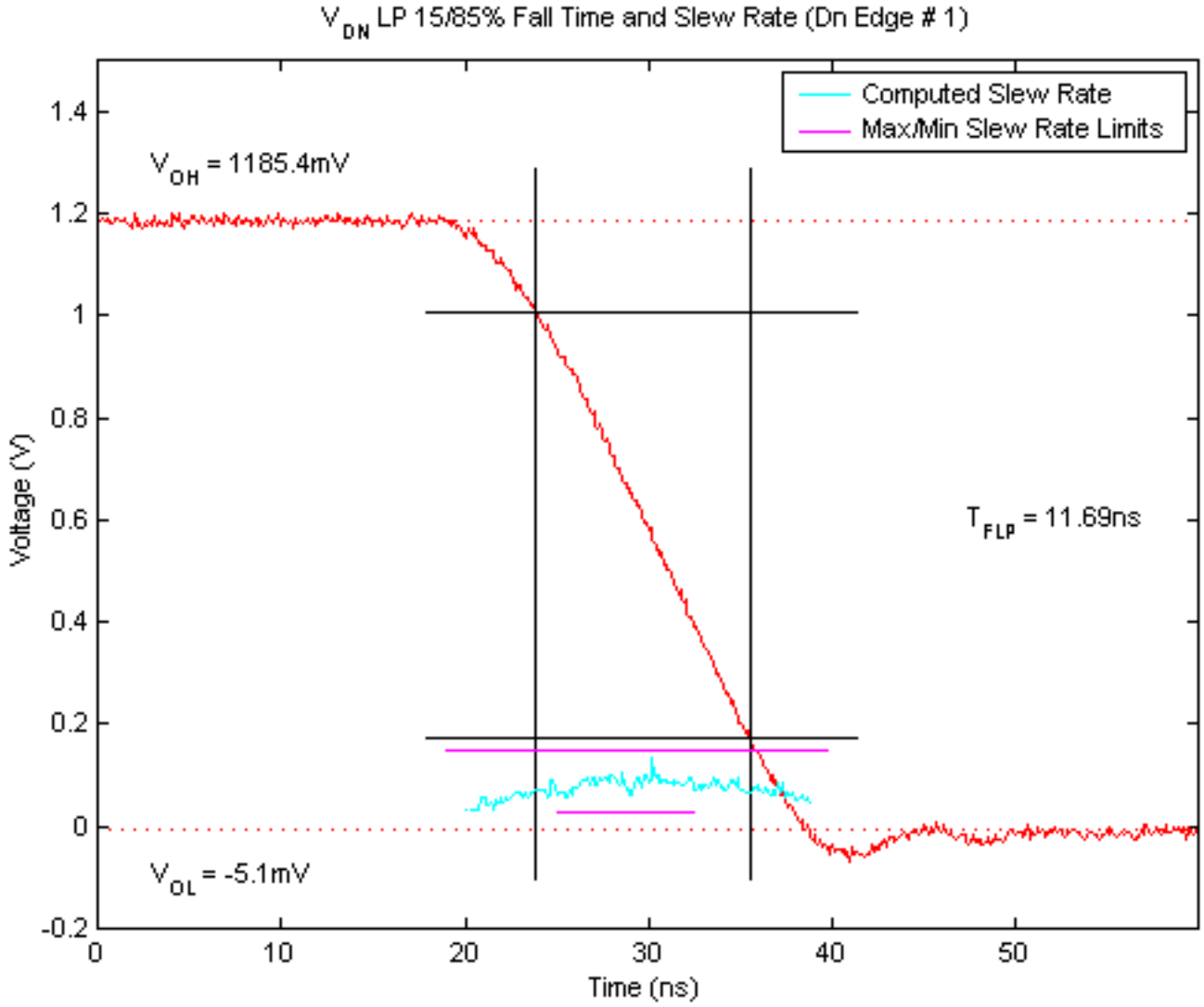

Figure 11: Dp LP-TX Fall Time (Data Lane 0, No CLOAD)

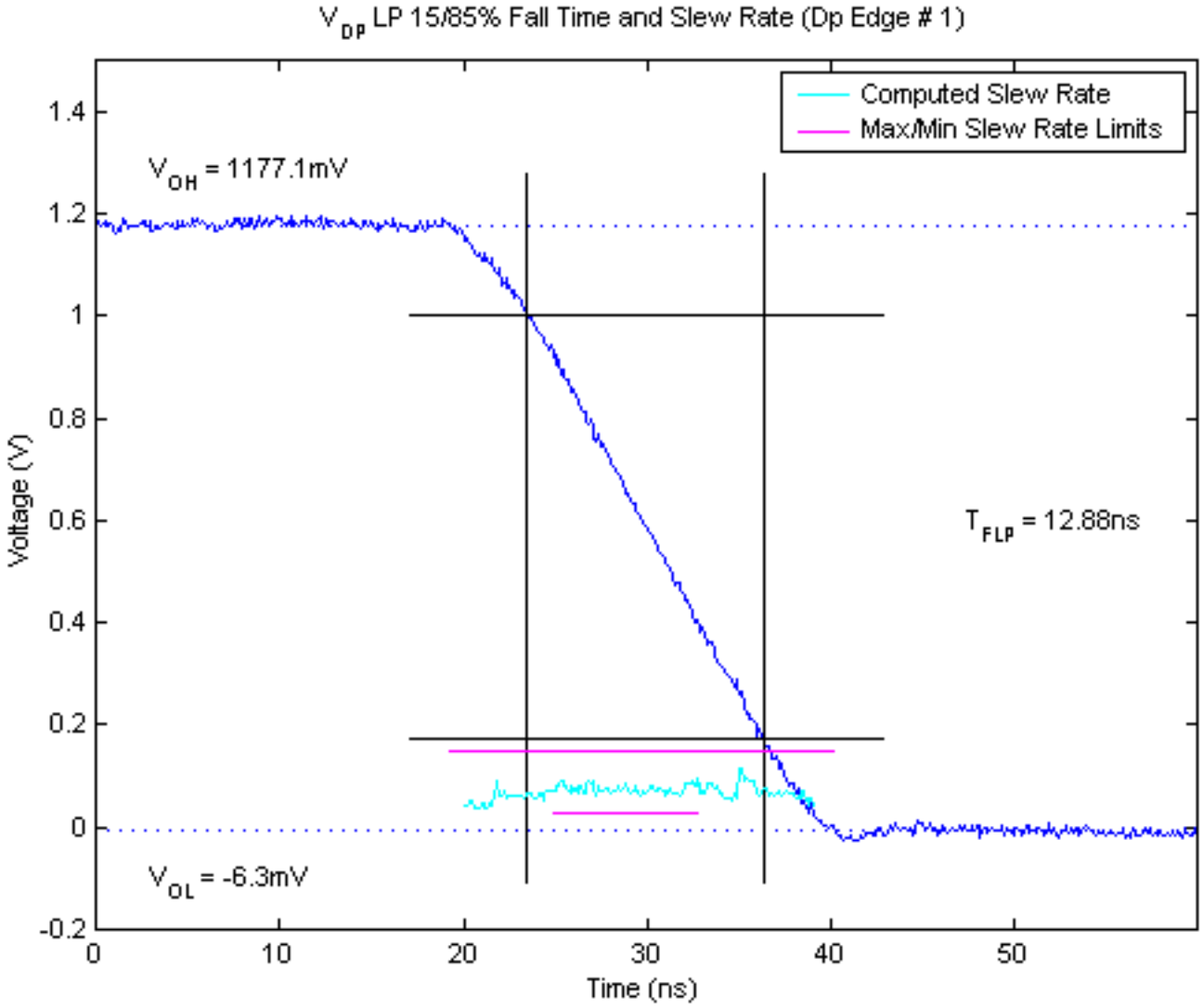

Figure 12: Dn LP-TX Fall Time (Data Lane 0, No CLOAD)

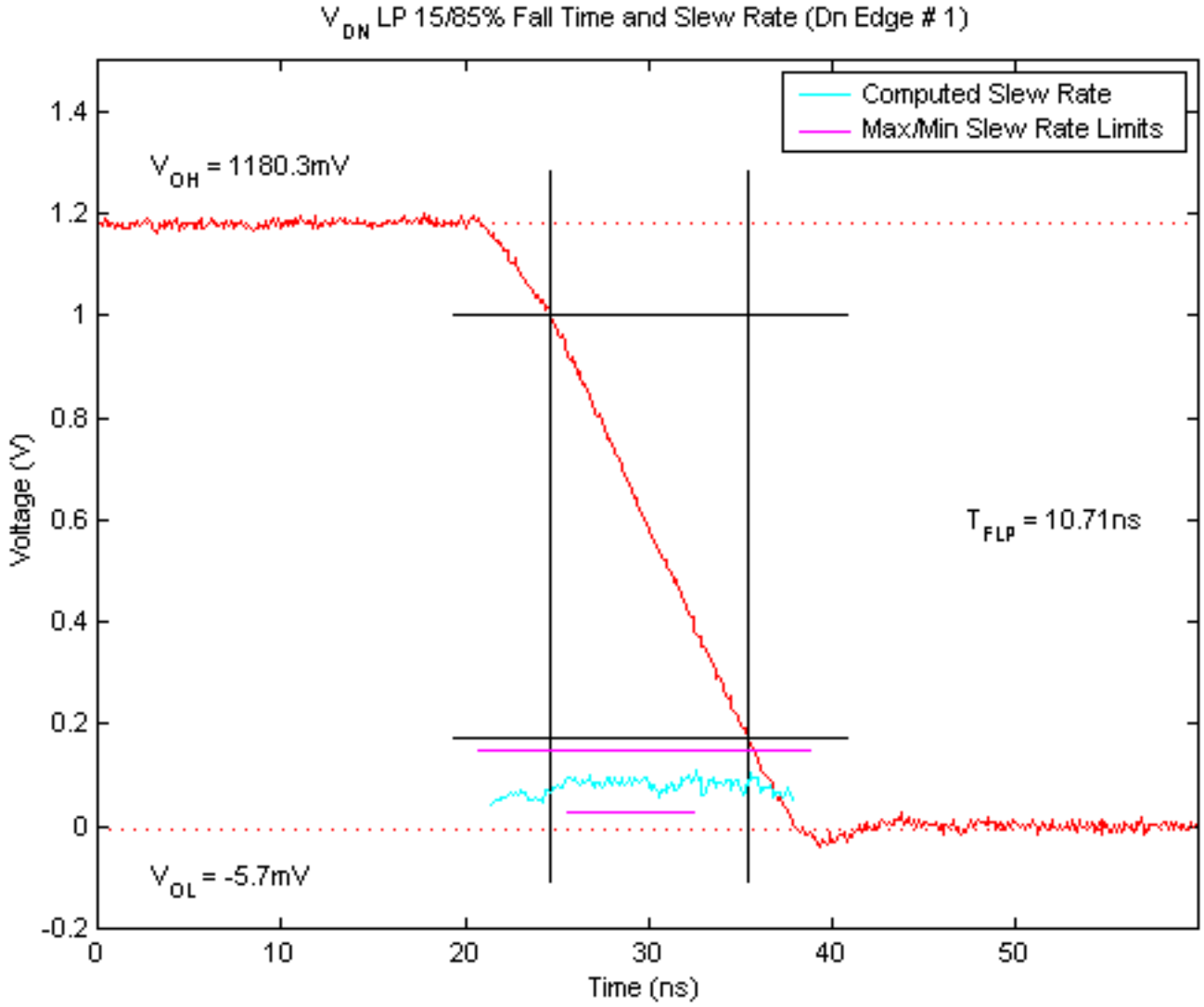

Figure 13: Computed LP XOR Clock (Data Lane 0, 50pF CLOAD, 930mV and 500mV Trip Levels)

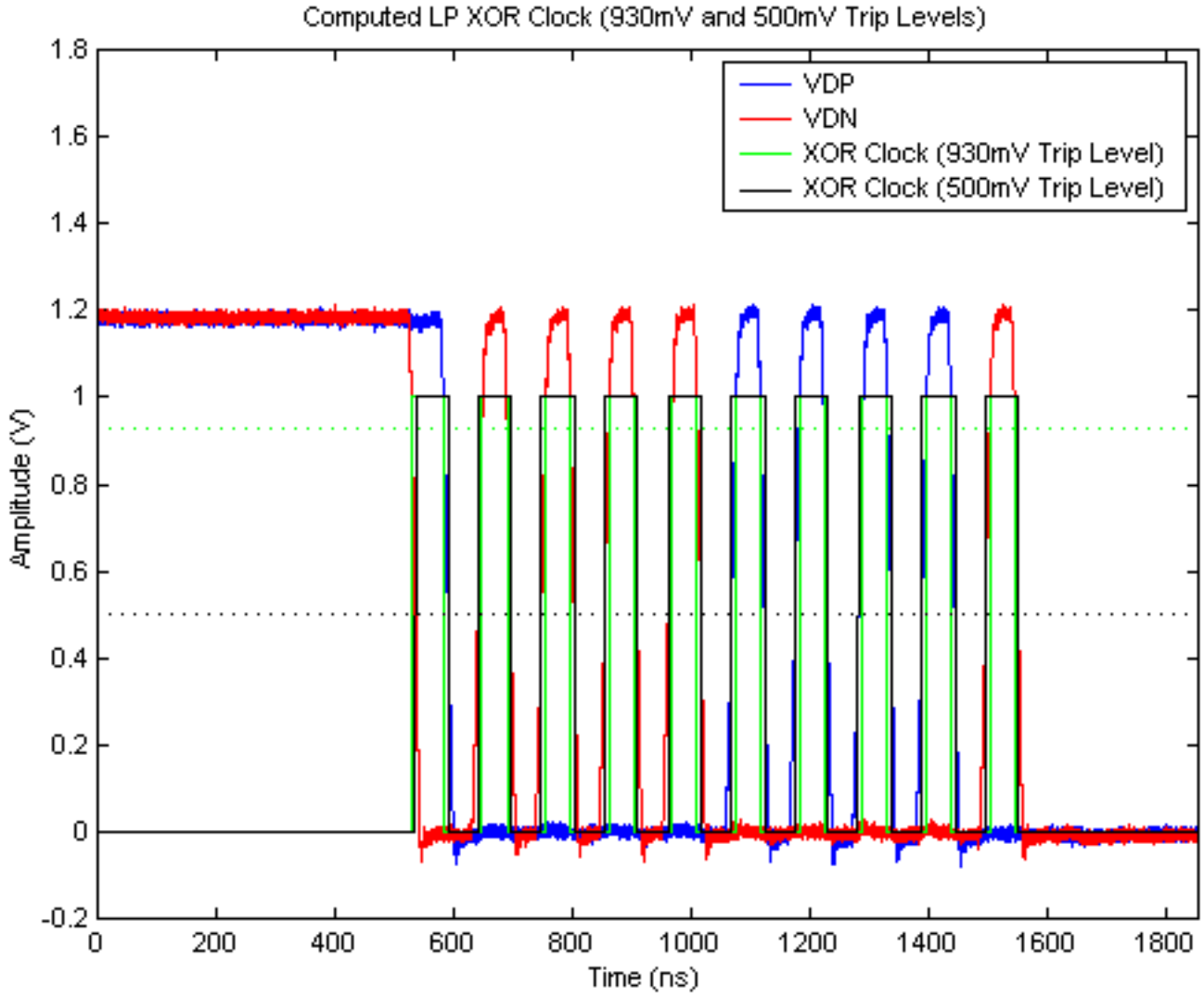

Figure 14: LP XOR Clock Pulse/Period Widths (Data Lane 0, 50pF CLOAD, 930mV Trip Level)

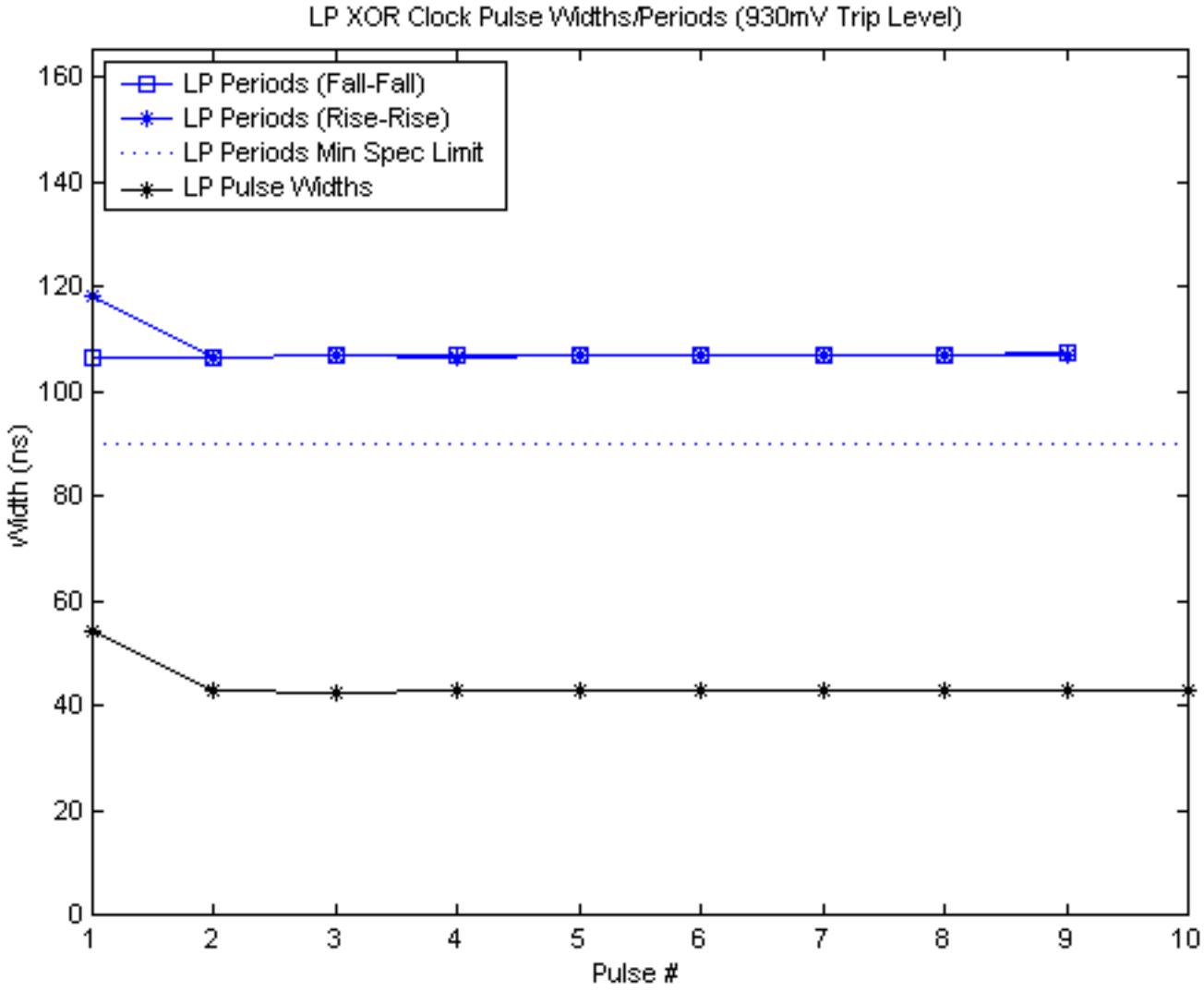

Figure 15: LP XOR Clock Pulse/Period Widths (Data Lane 0, 50pF CLOAD, 500mV Trip Level)

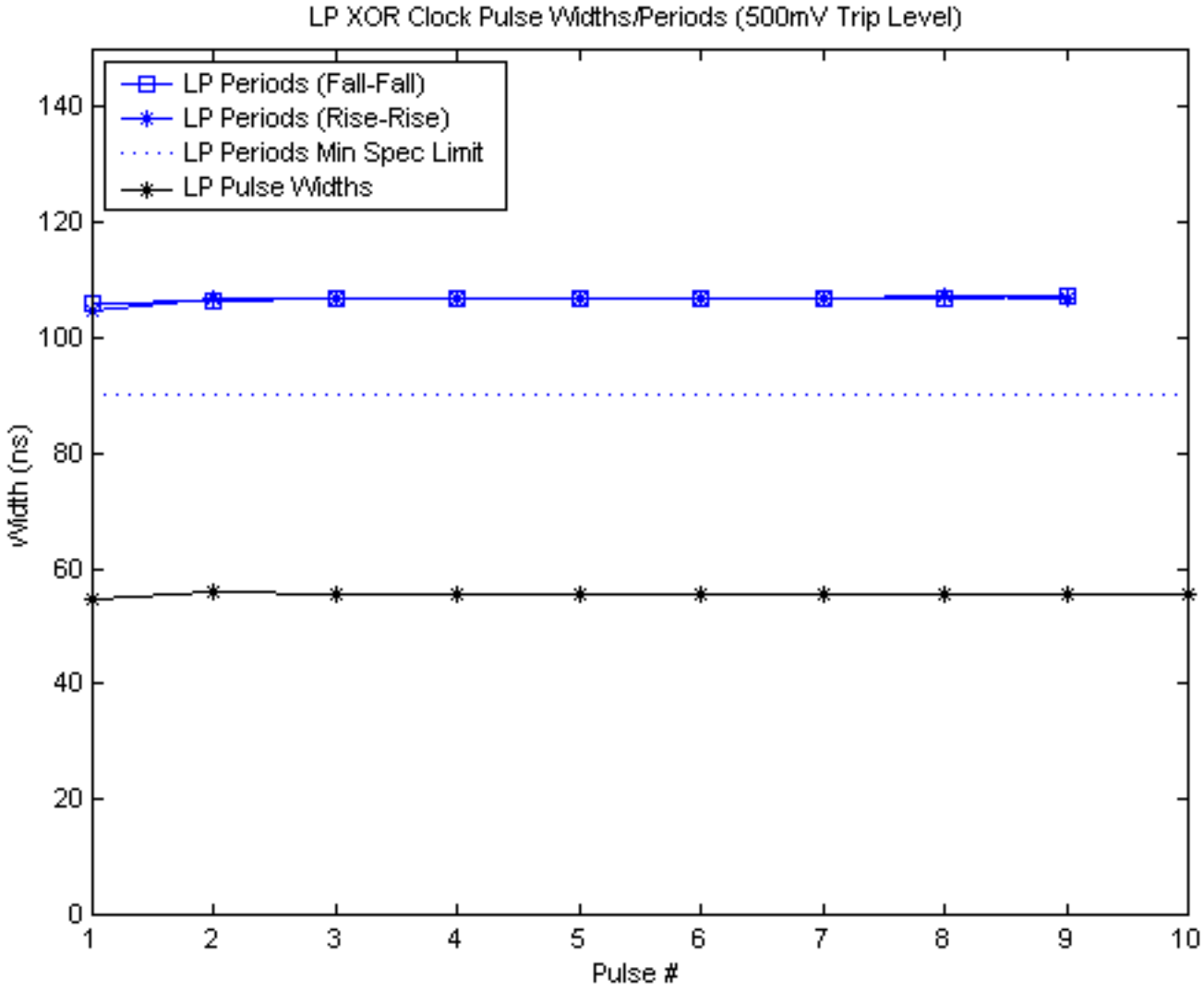

Figure 16: Computed LP XOR Clock (Data Lane 0, No CLOAD, 930mV and 500mV Trip Levels)

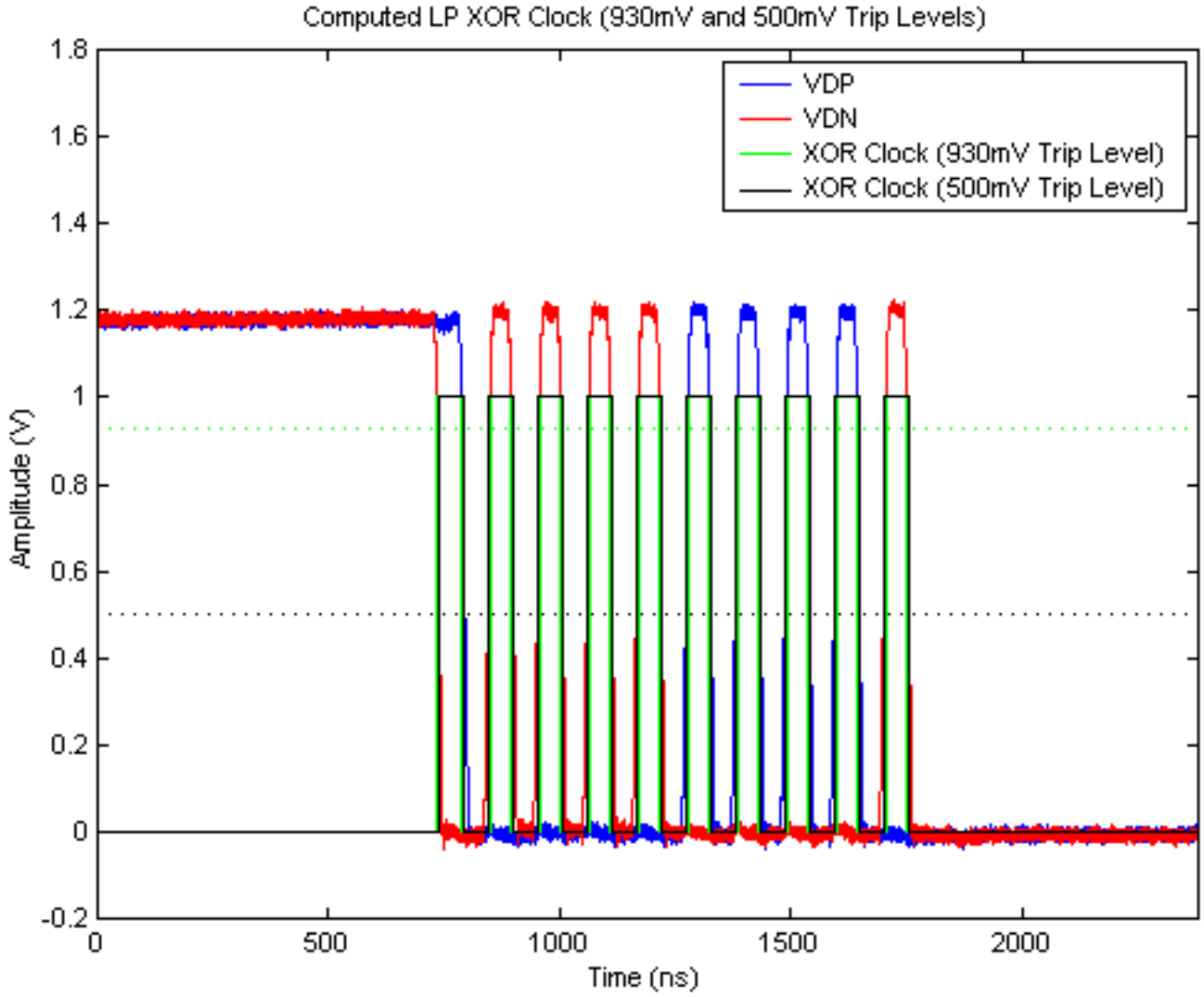

Figure 17: LP XOR Clock Pulse/Period Widths (Data Lane 0, No CLOAD, 930mV Trip Level)

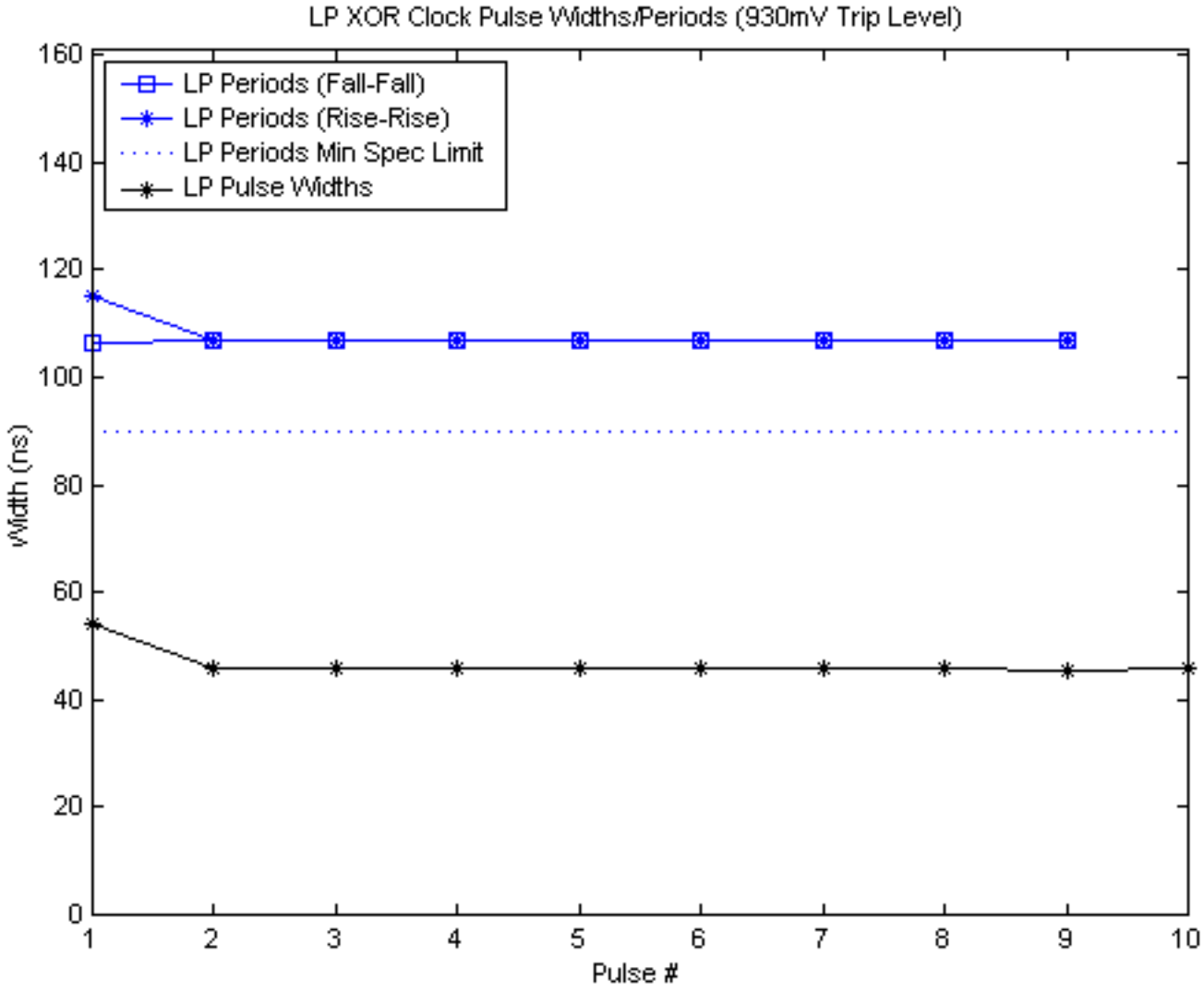

Figure 18: LP XOR Clock Pulse/Period Widths (Data Lane 0, No CLOAD, 500mV Trip Level)

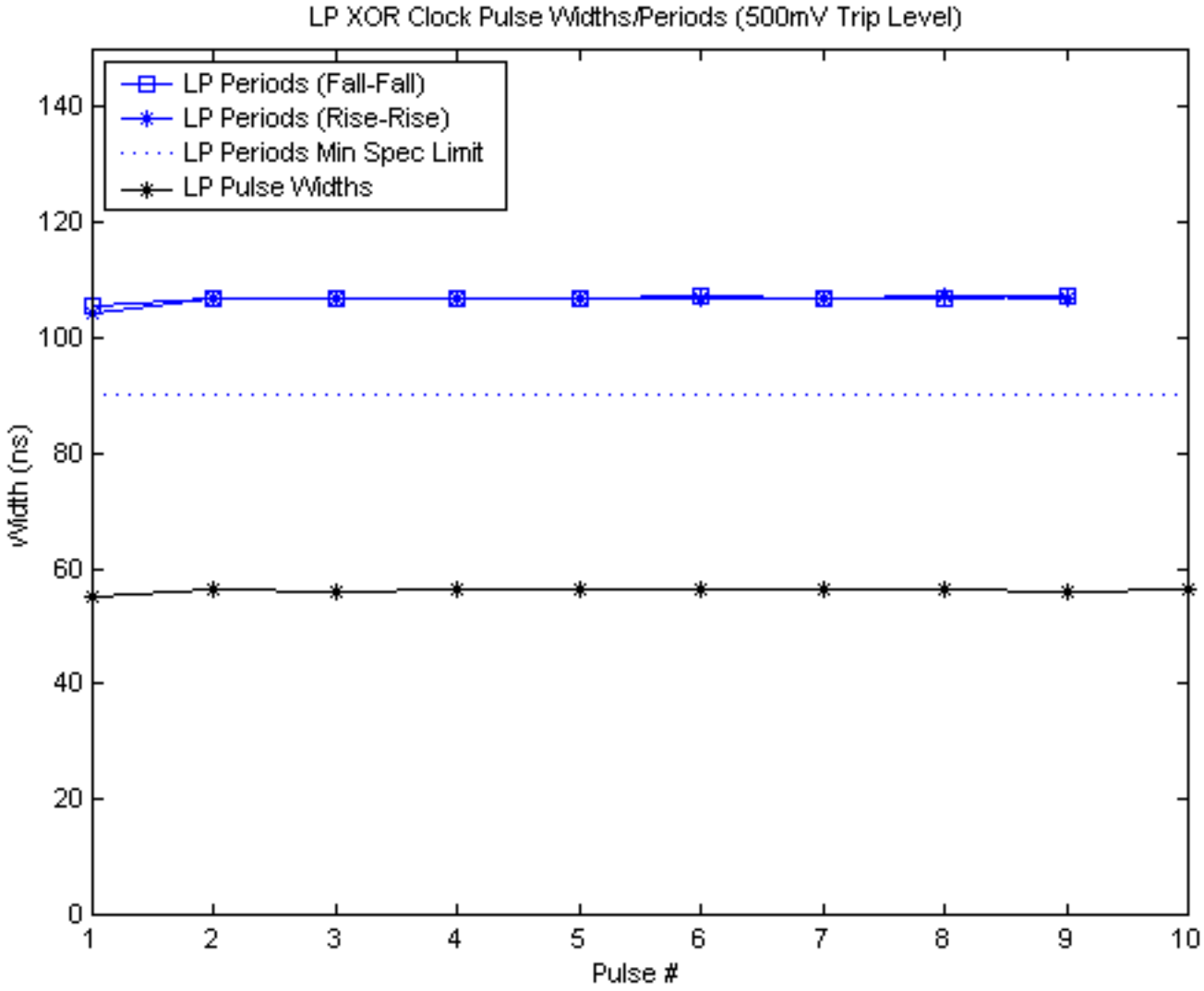

Figure 19: TCLK-PRE, TLPX, THS-PREPARE, and THS-ZERO Intervals (Data Lane 0, ZID=100)

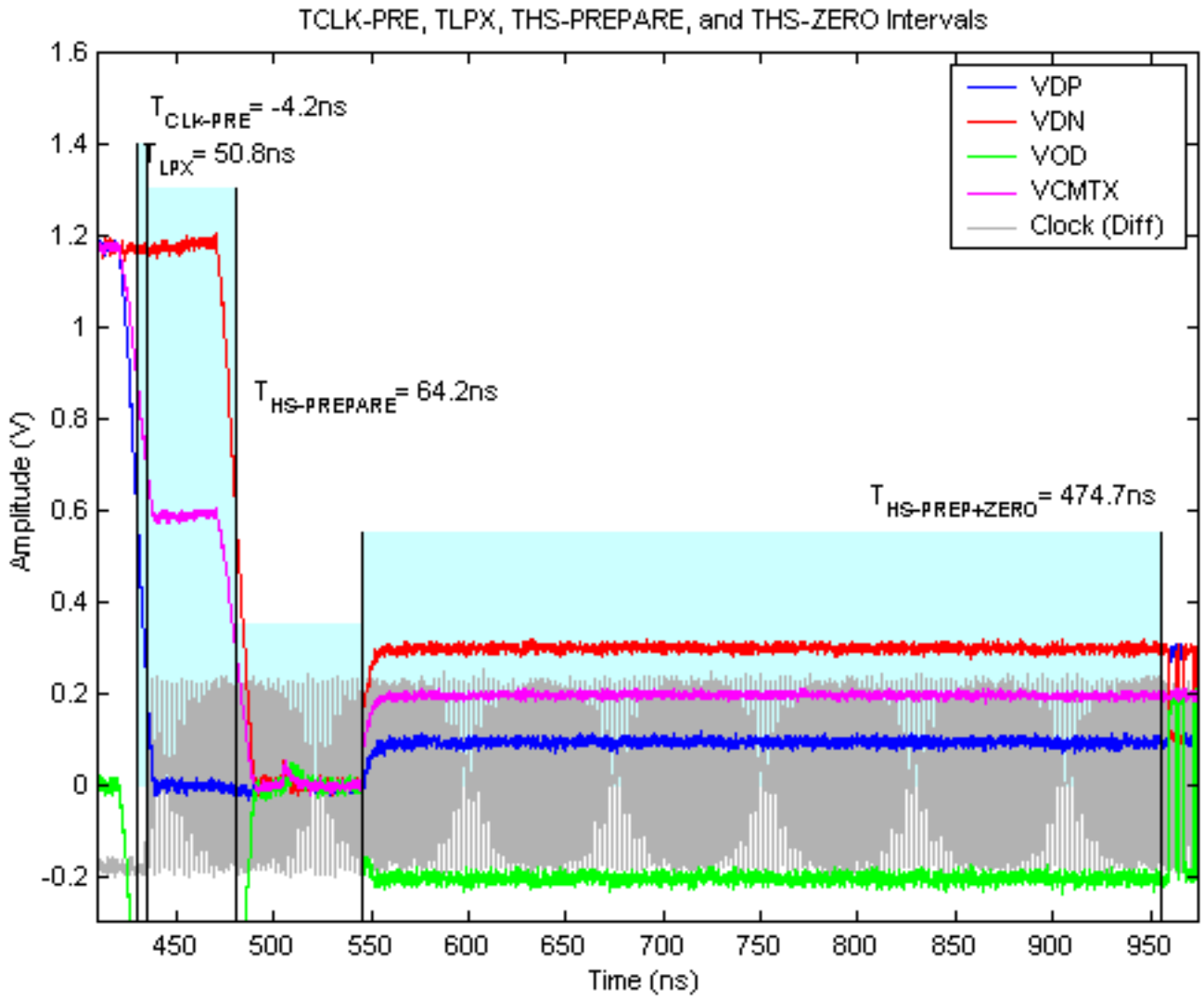

Figure 20: HS-TX Differential Voltage VOD(1) (Data Lane 0, ZID=100)

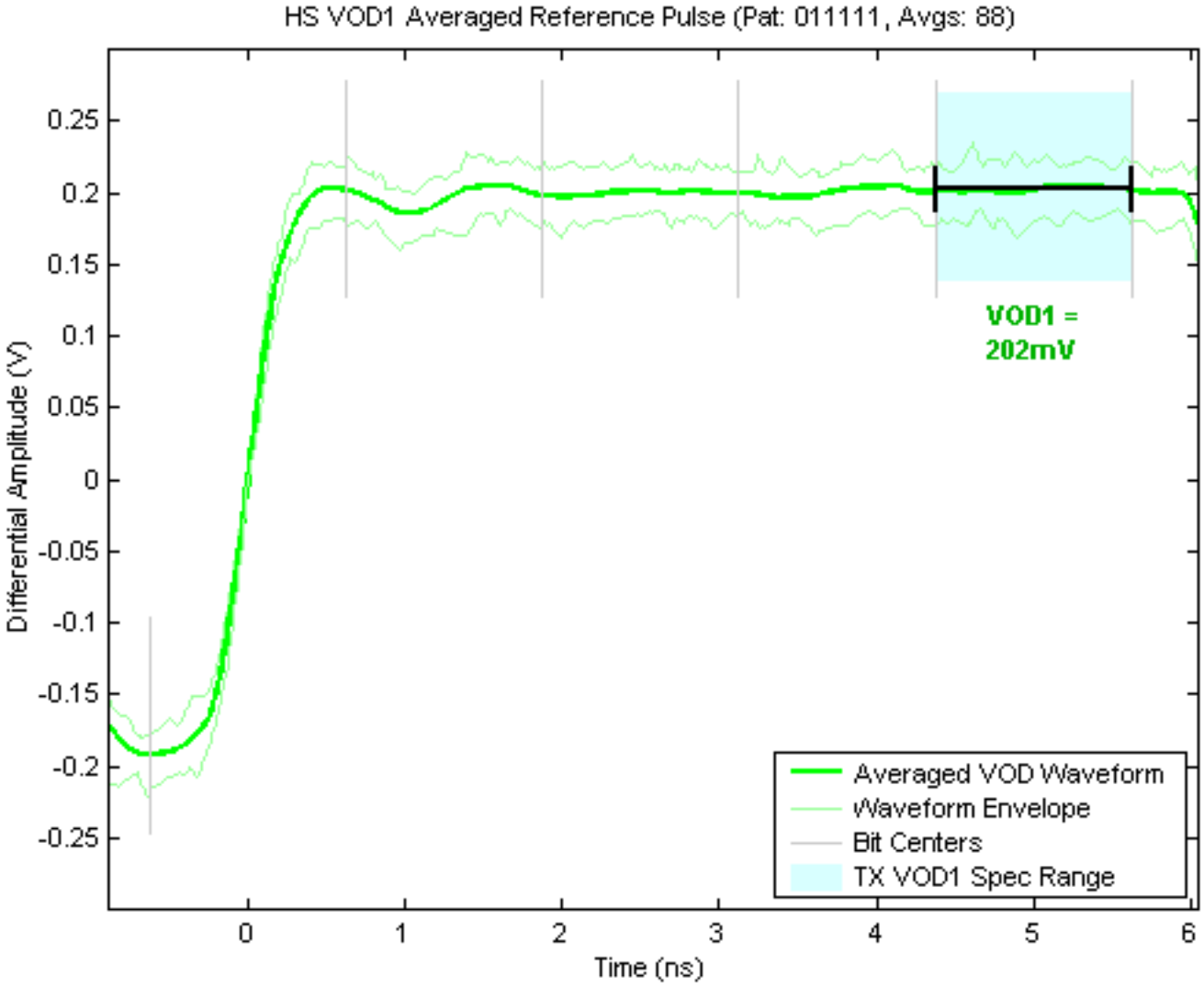

Figure 21: HS-TX Differential Voltage VOD(0) (Data Lane 0, ZID=100)

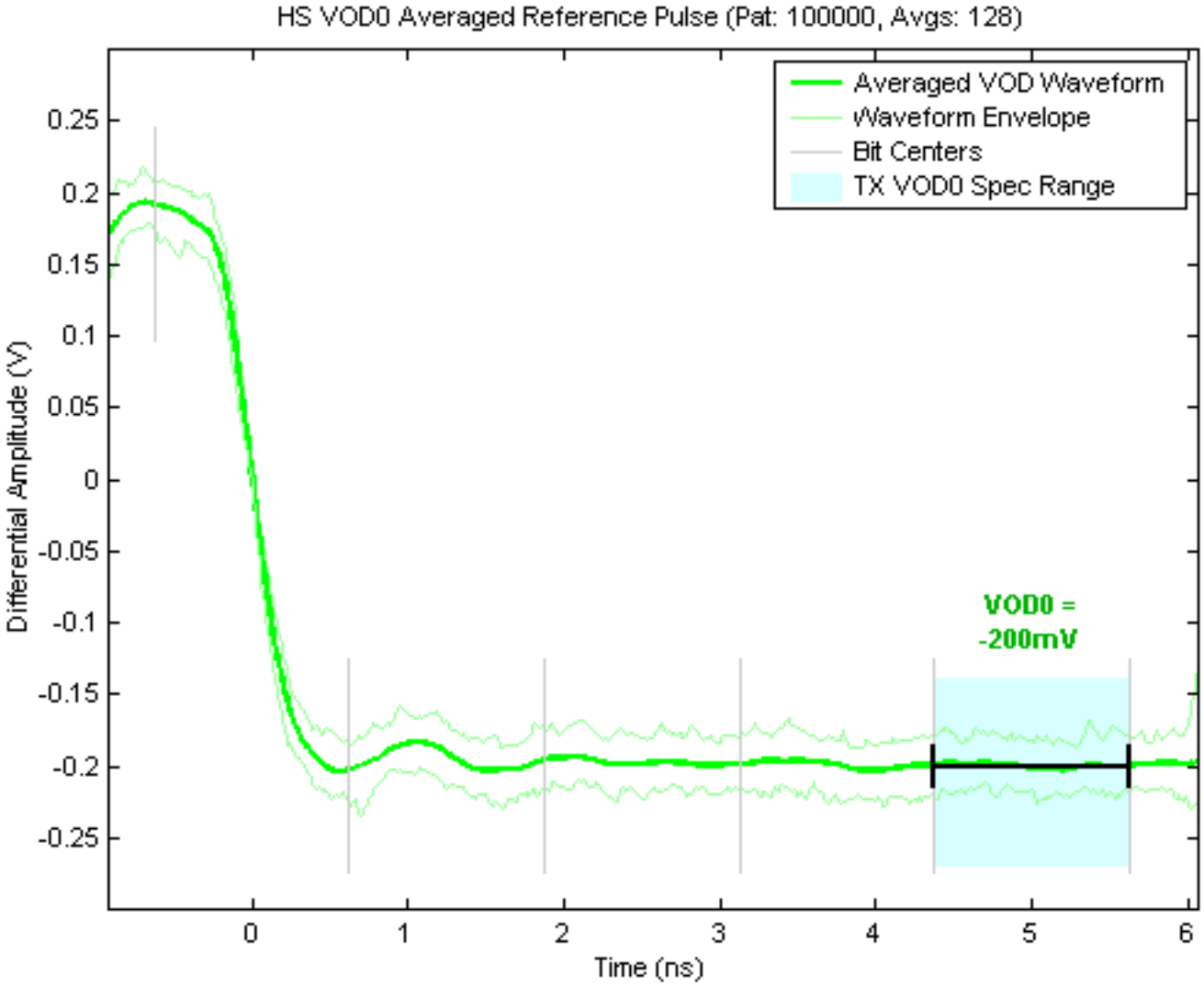

Figure 22: HS-TX Differential Voltage VOD(1) (Data Lane 0, ZID=125)

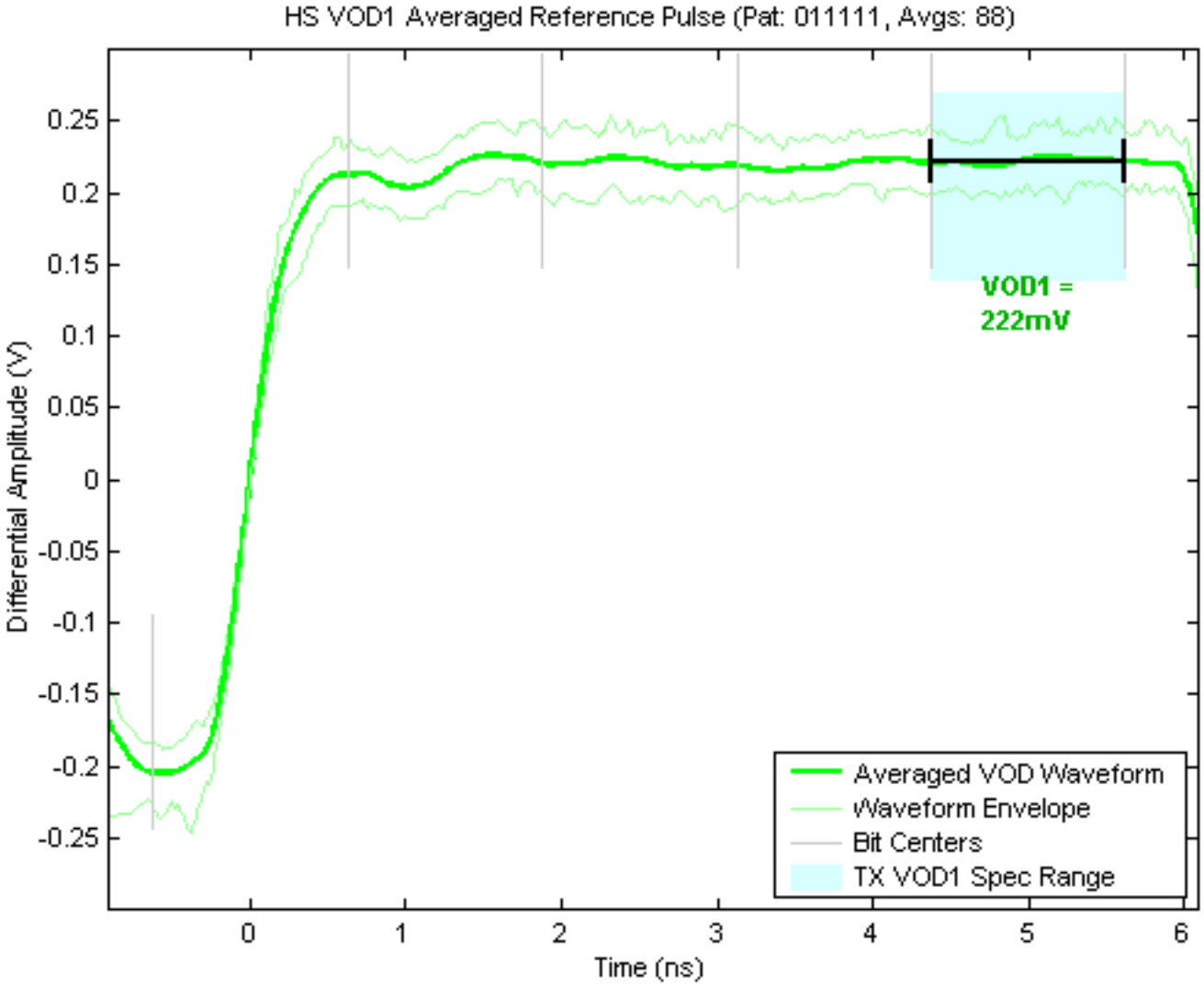

Figure 23: HS-TX Differential Voltage VOD(0) (Data Lane 0, ZID=125)

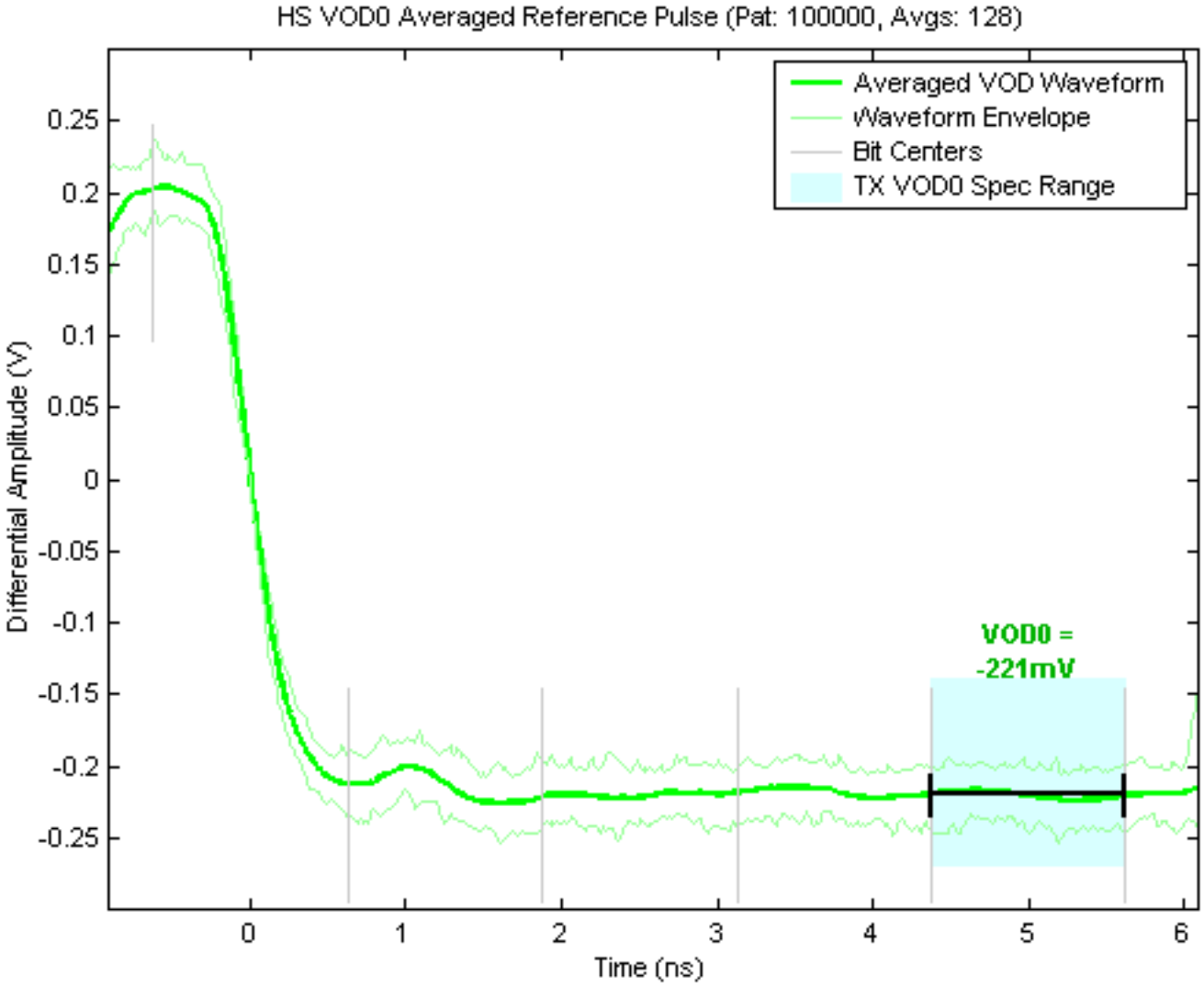

Figure 24: HS-TX Differential Voltage VOD(1) (Data Lane 0, ZID=80)

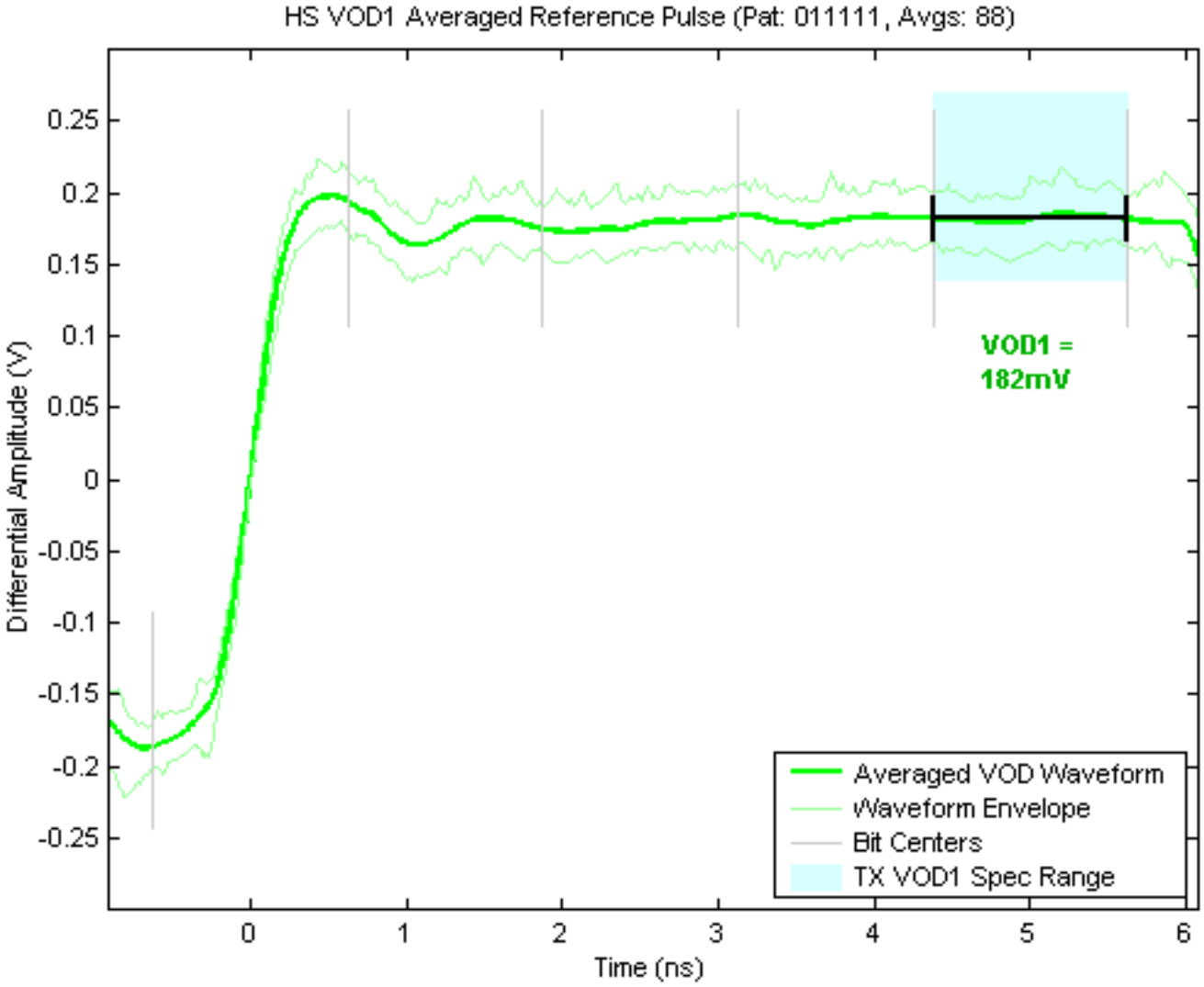

Figure 25: HS-TX Differential Voltage VOD(0) (Data Lane 0, ZID=80)

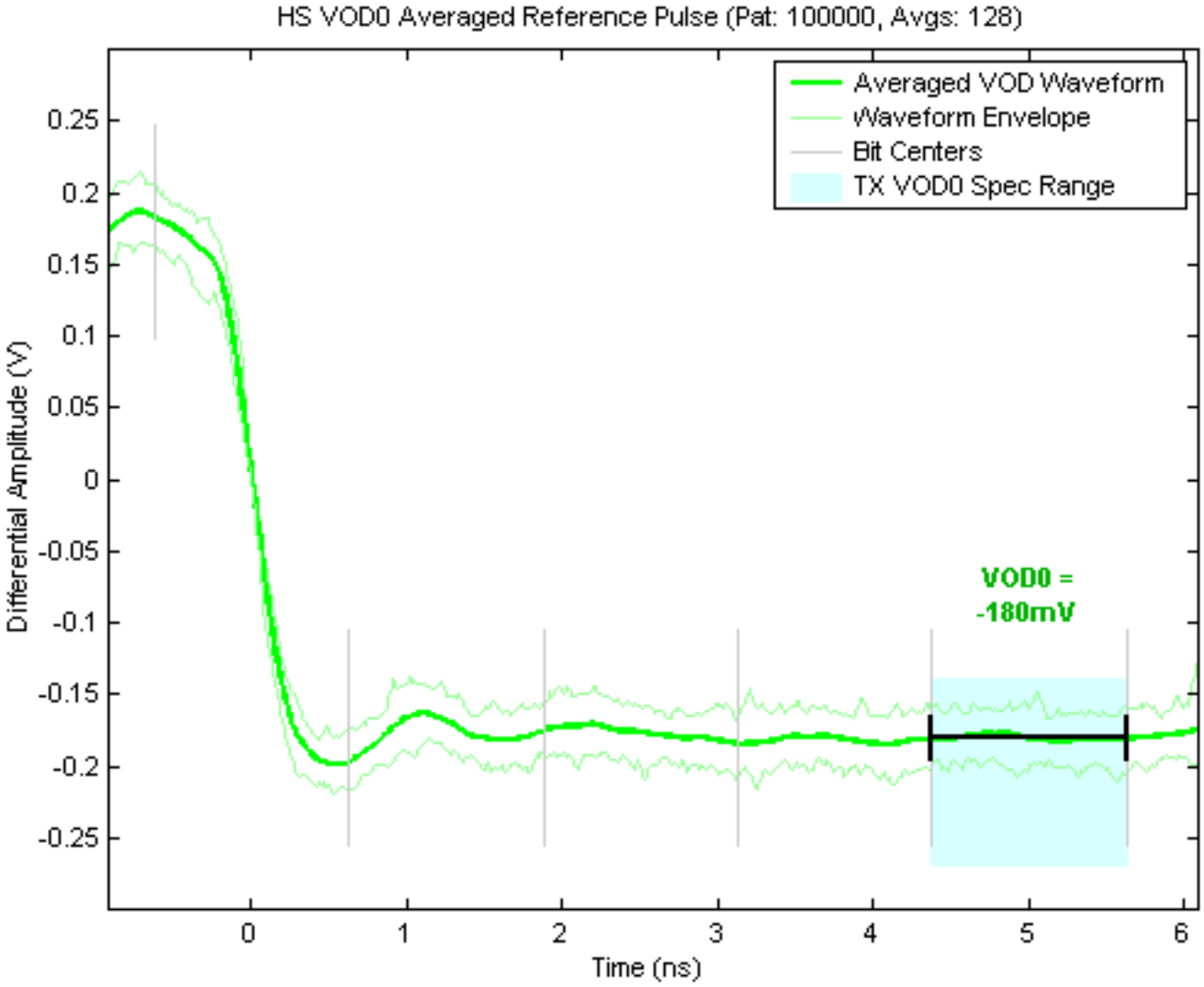

Figure 26: HS-TX Single-Ended Voltage Dp VOHHS (Data Lane 0, ZID=100)

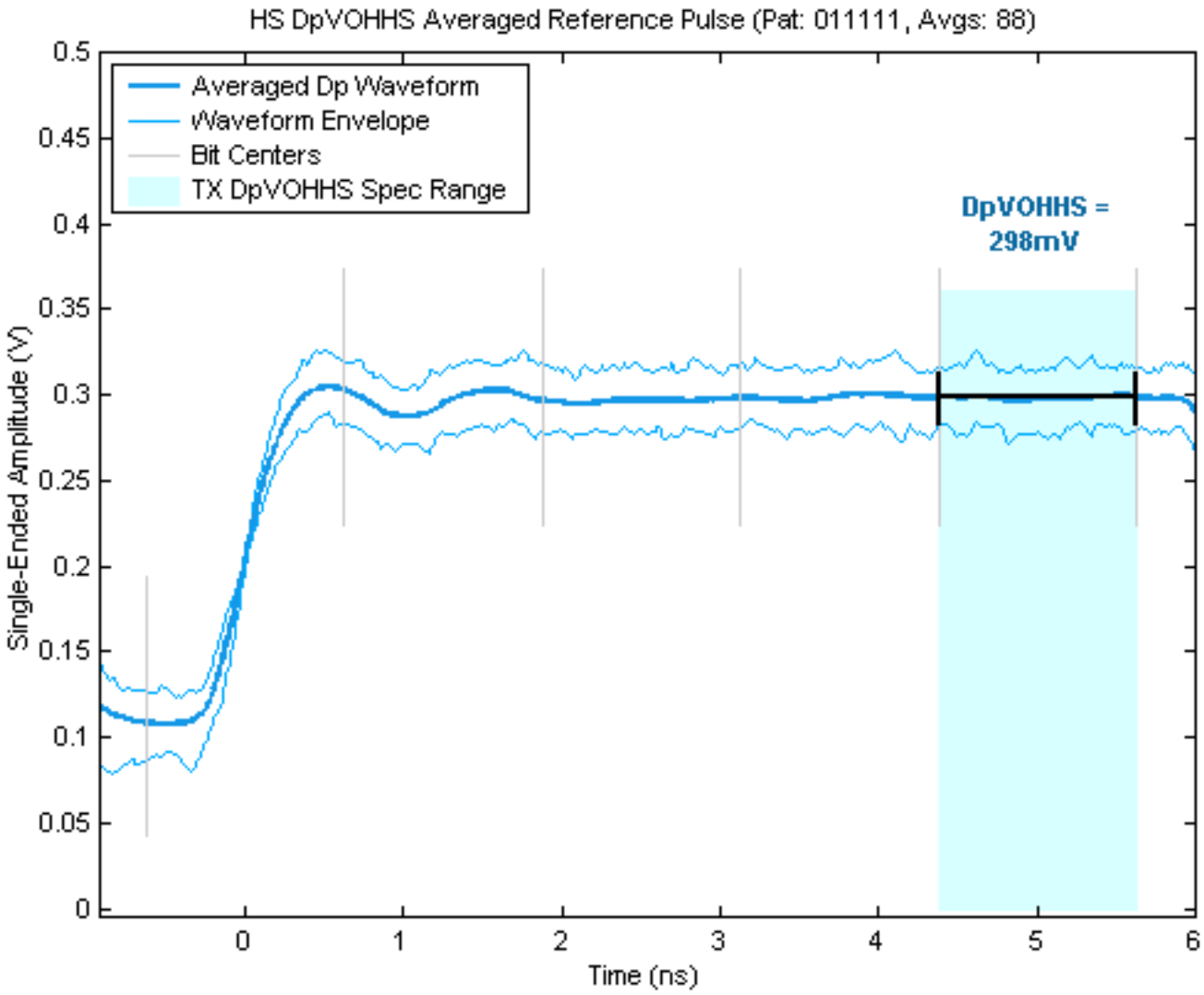

Figure 27: HS-TX Single-Ended Voltage Dn VOHHS (Data Lane 0, ZID=100)

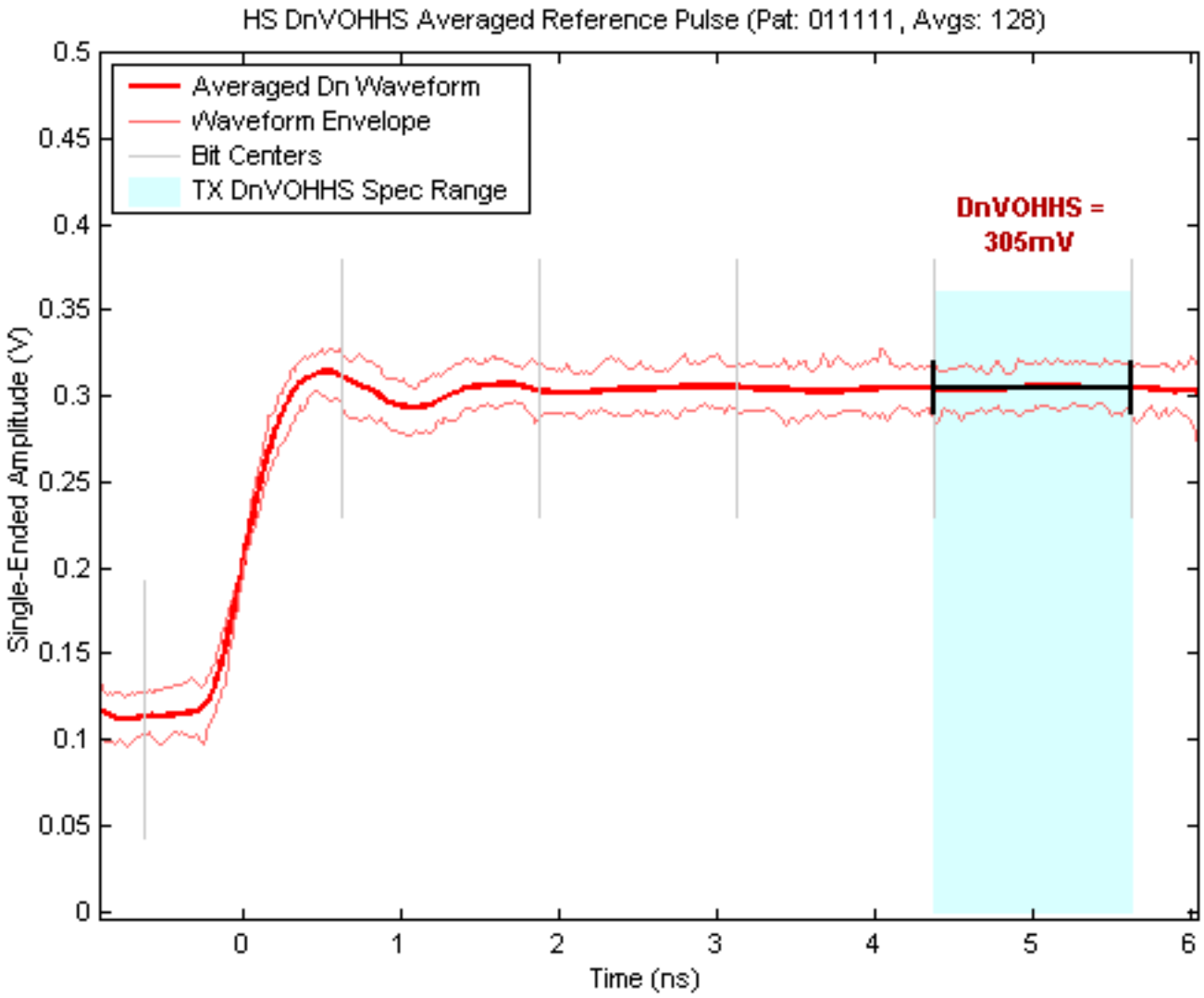

Figure 28: HS-TX Single-Ended Voltage Dp VOHHS (Data Lane 0, ZID=125)

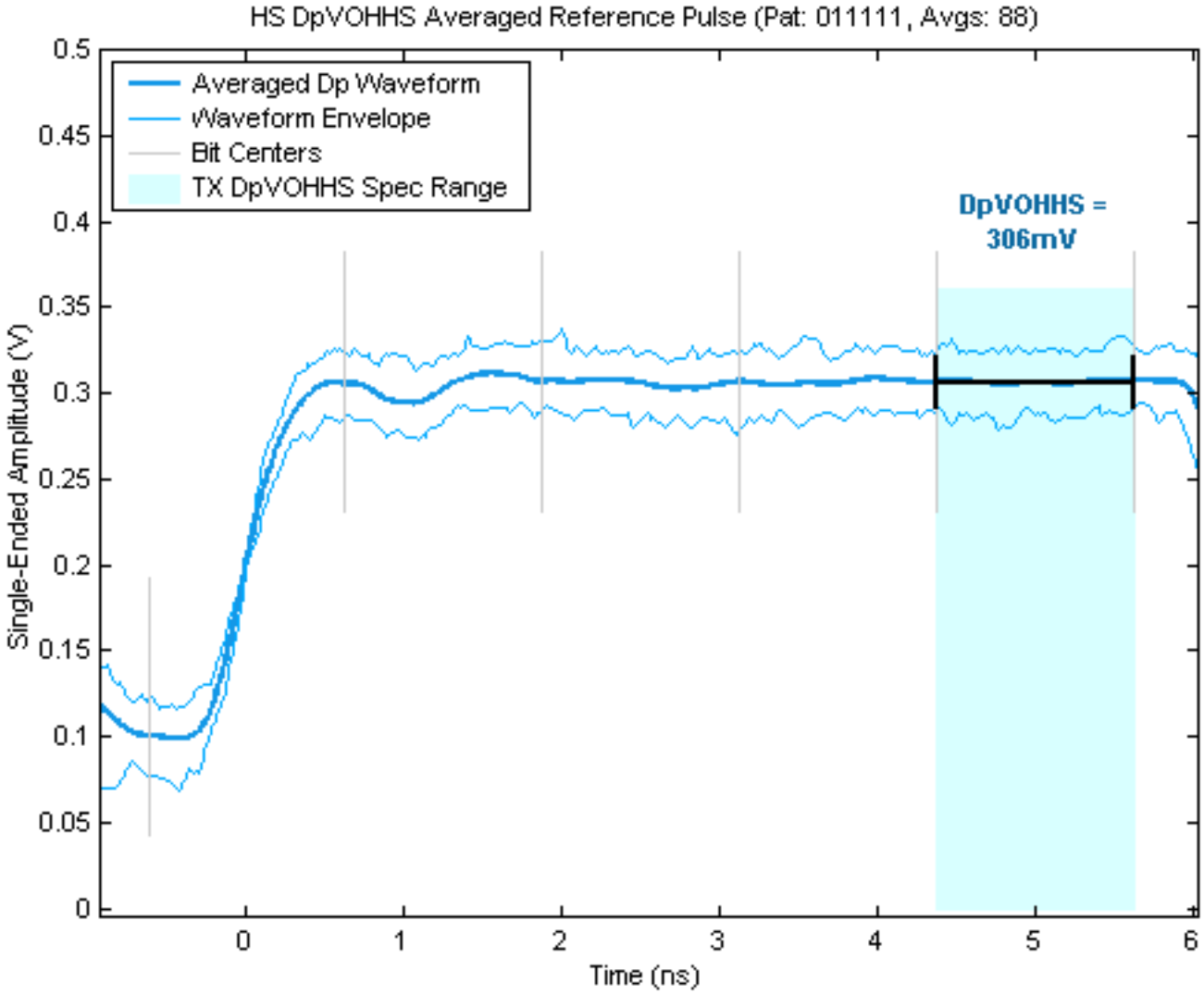

Figure 29: HS-TX Single-Ended Voltage Dn VOHHS (Data Lane 0, ZID=125)

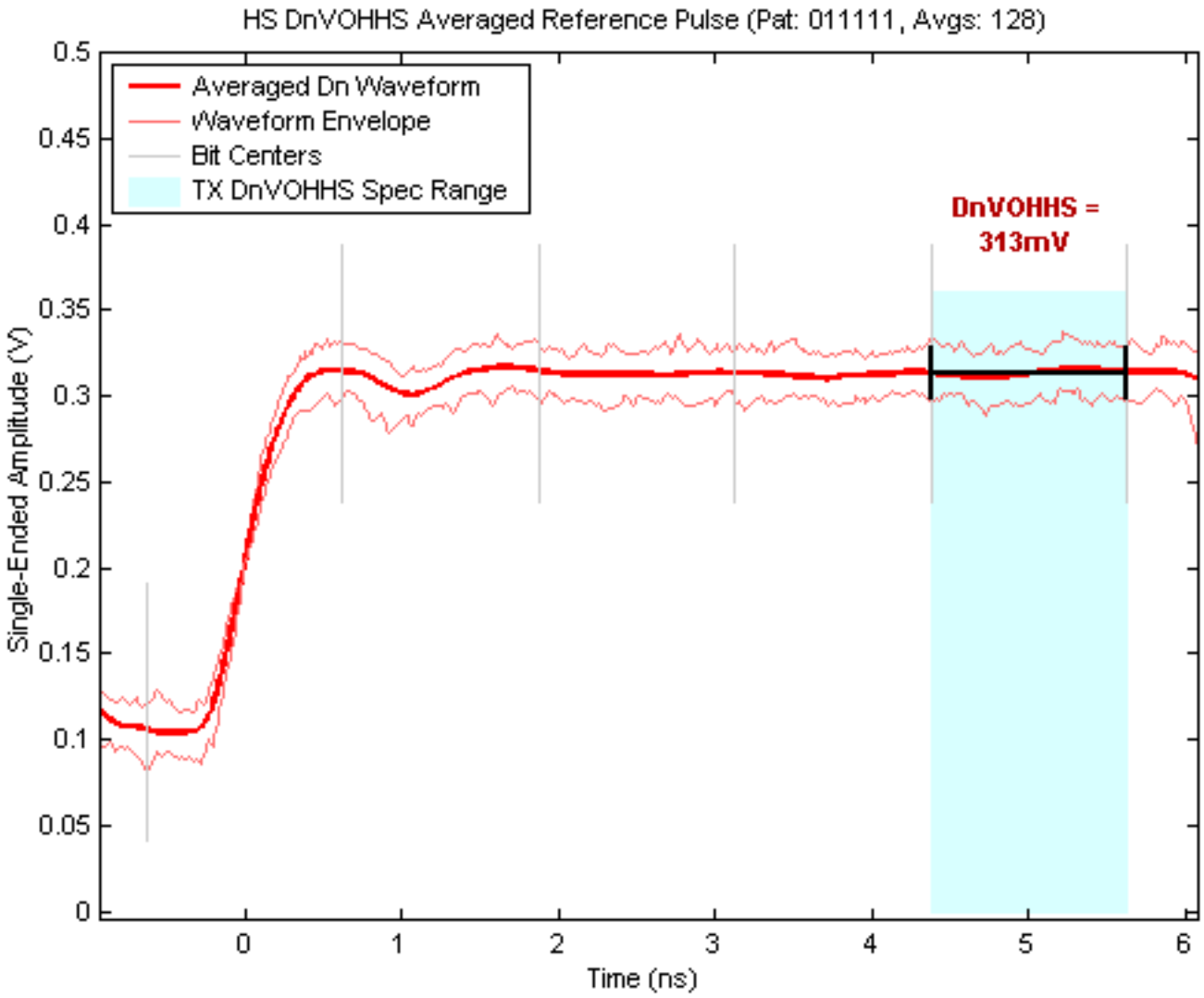

Figure 30: HS-TX Single-Ended Voltage Dp VOHHS (Data Lane 0, ZID=80)

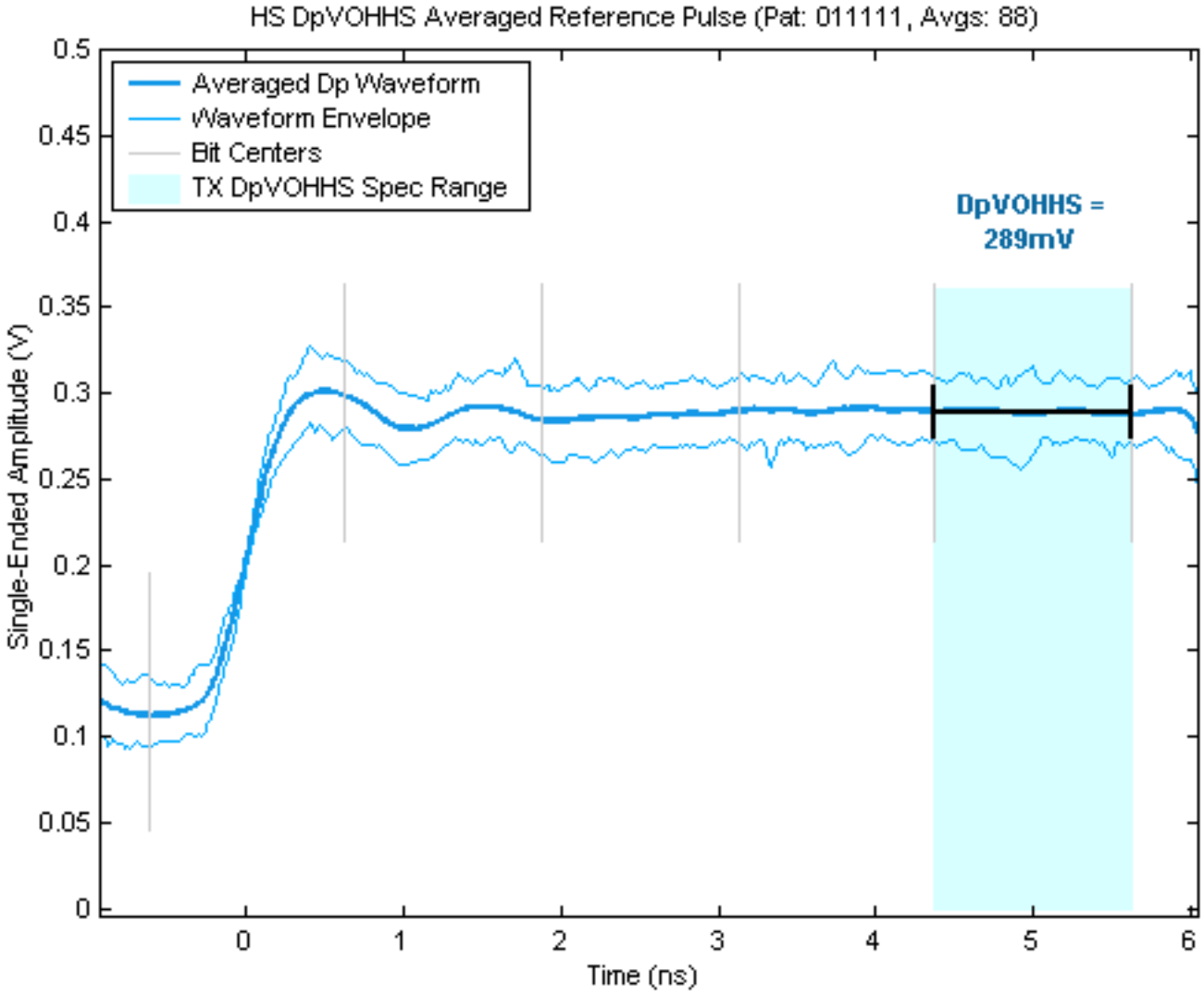

Figure 31: HS-TX Single-Ended Voltage Dn VOHHS (Data Lane 0, ZID=80)

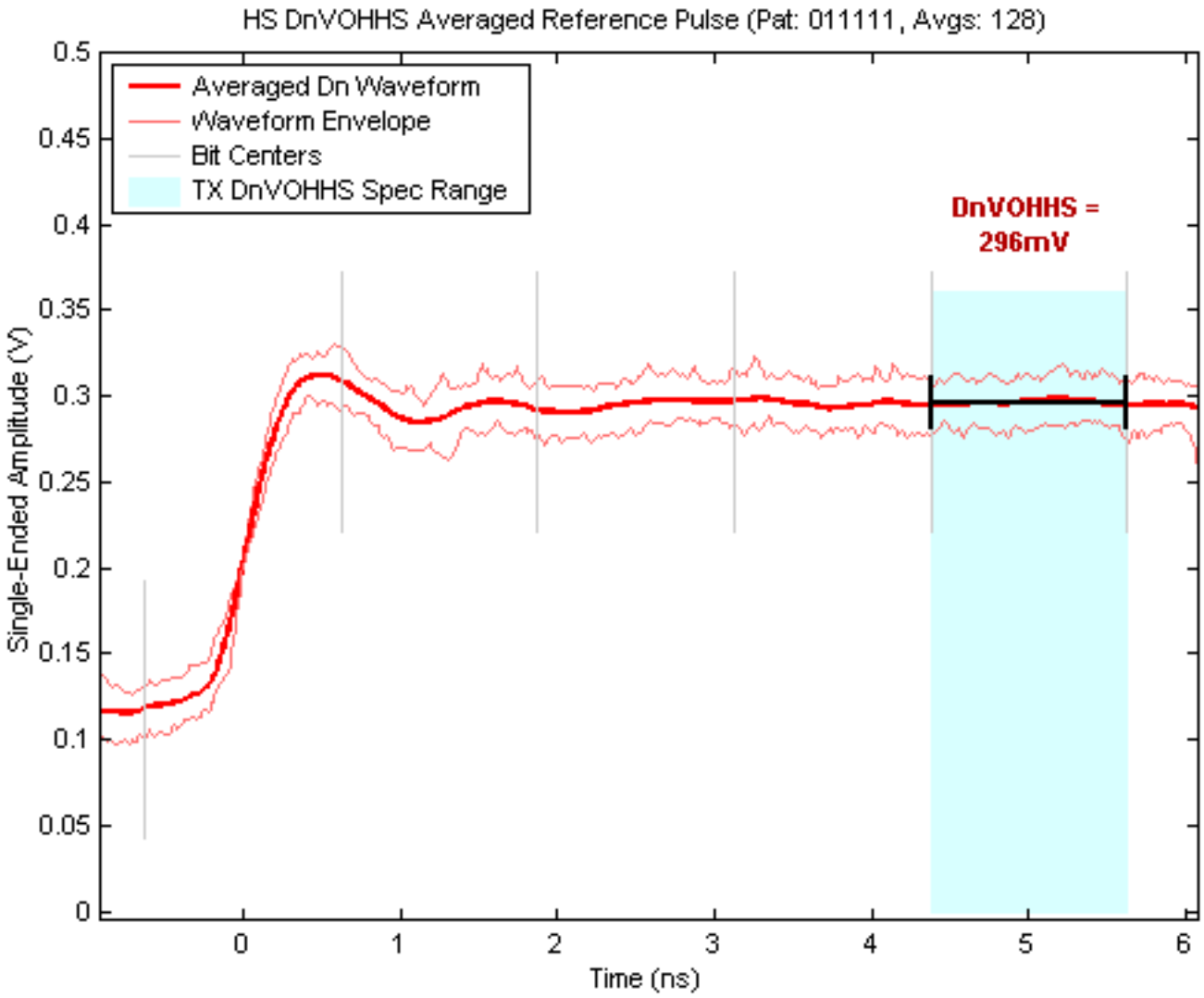

Figure 32: HS-TX Static Common-Mode Voltages, VCMTX (Data Lane 0, ZID=100)

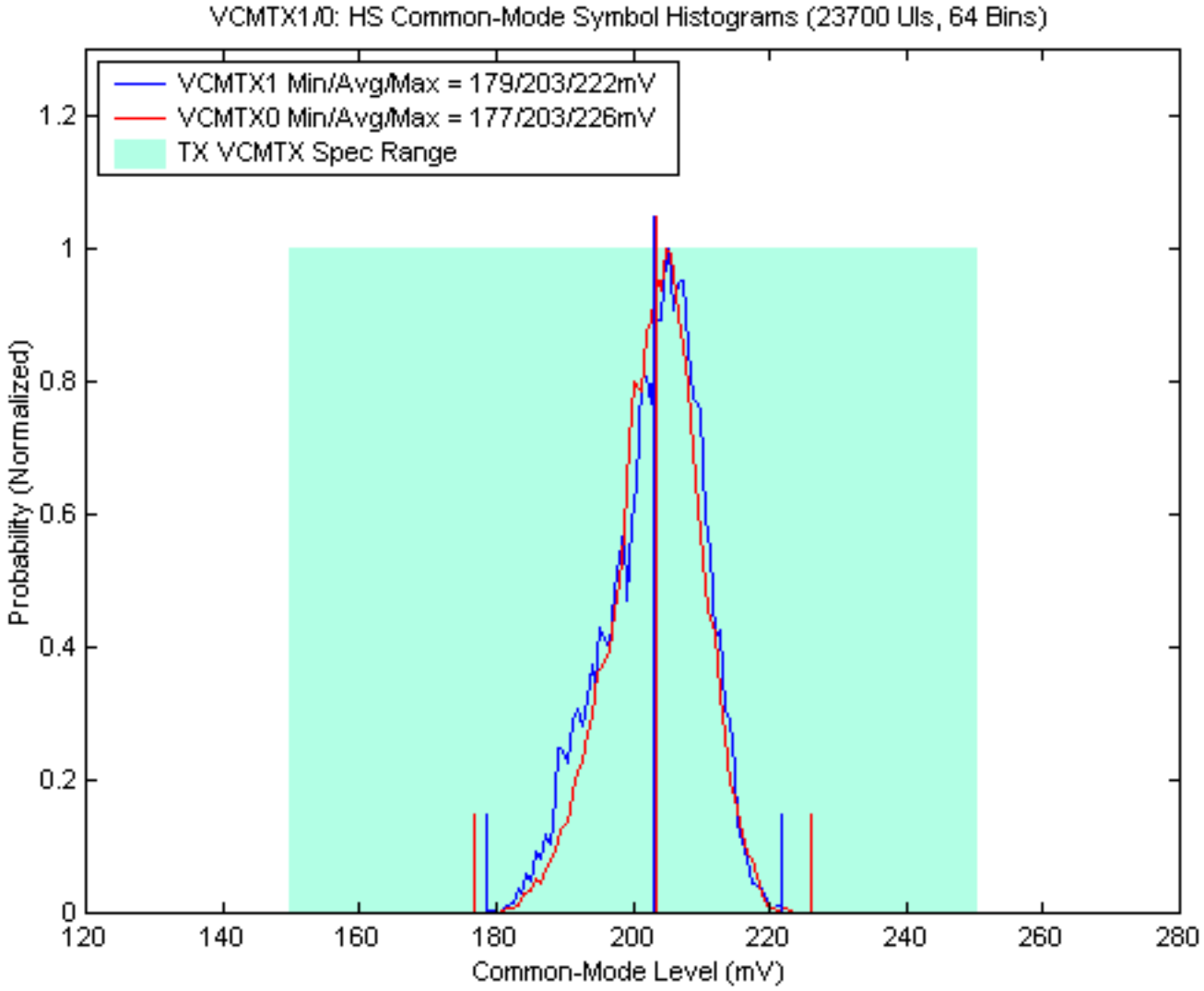

Figure 33: HS-TX Static Common-Mode Voltages, VCMTX (Data Lane 0, ZID=125)

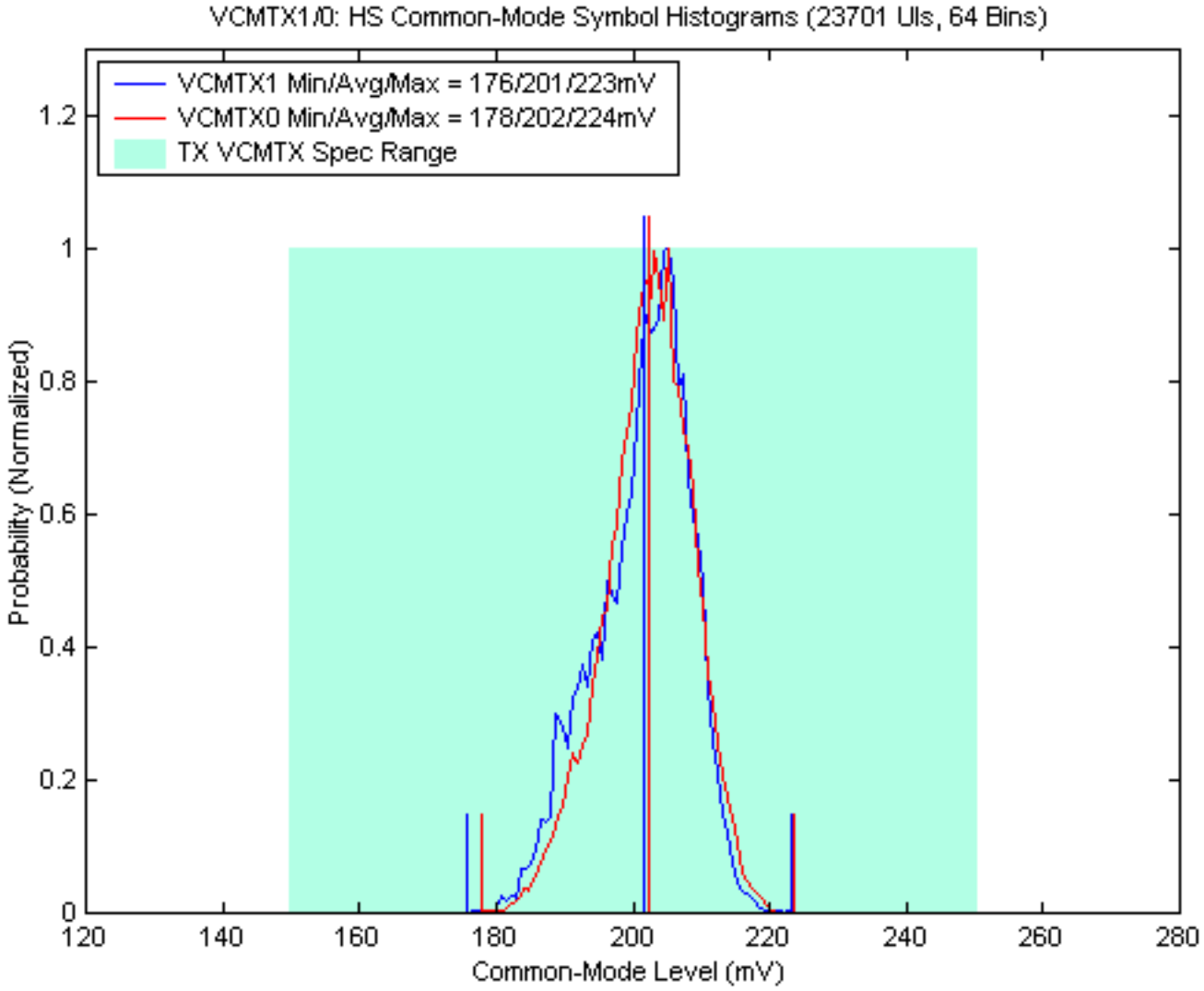

Figure 34: HS-TX Static Common-Mode Voltages, VCMTX (Data Lane 0, ZID=80)

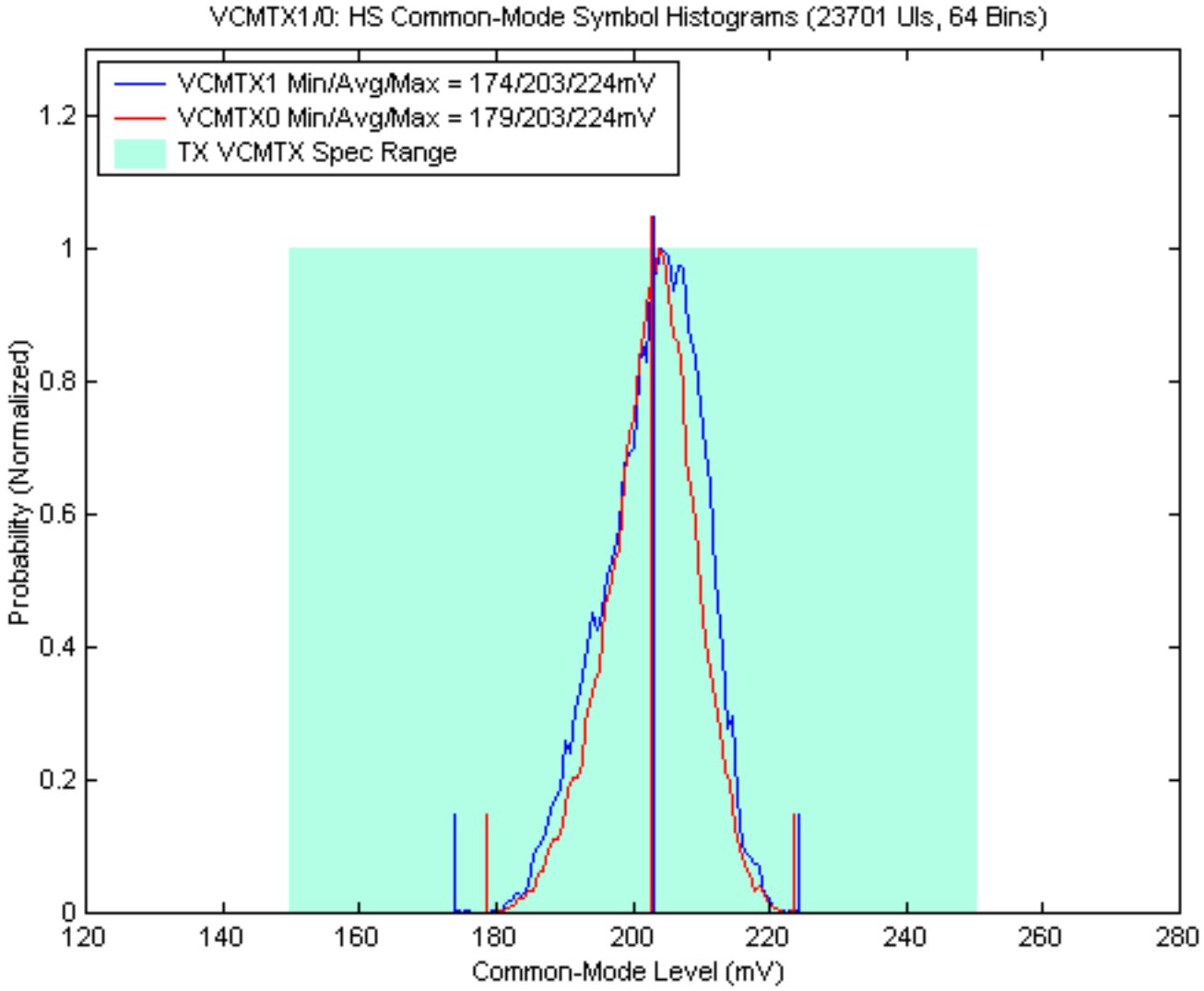

Figure 35: HF/LF Filtered HS-TX Common-Mode Waveforms (Data Lane 0, ZID=100)

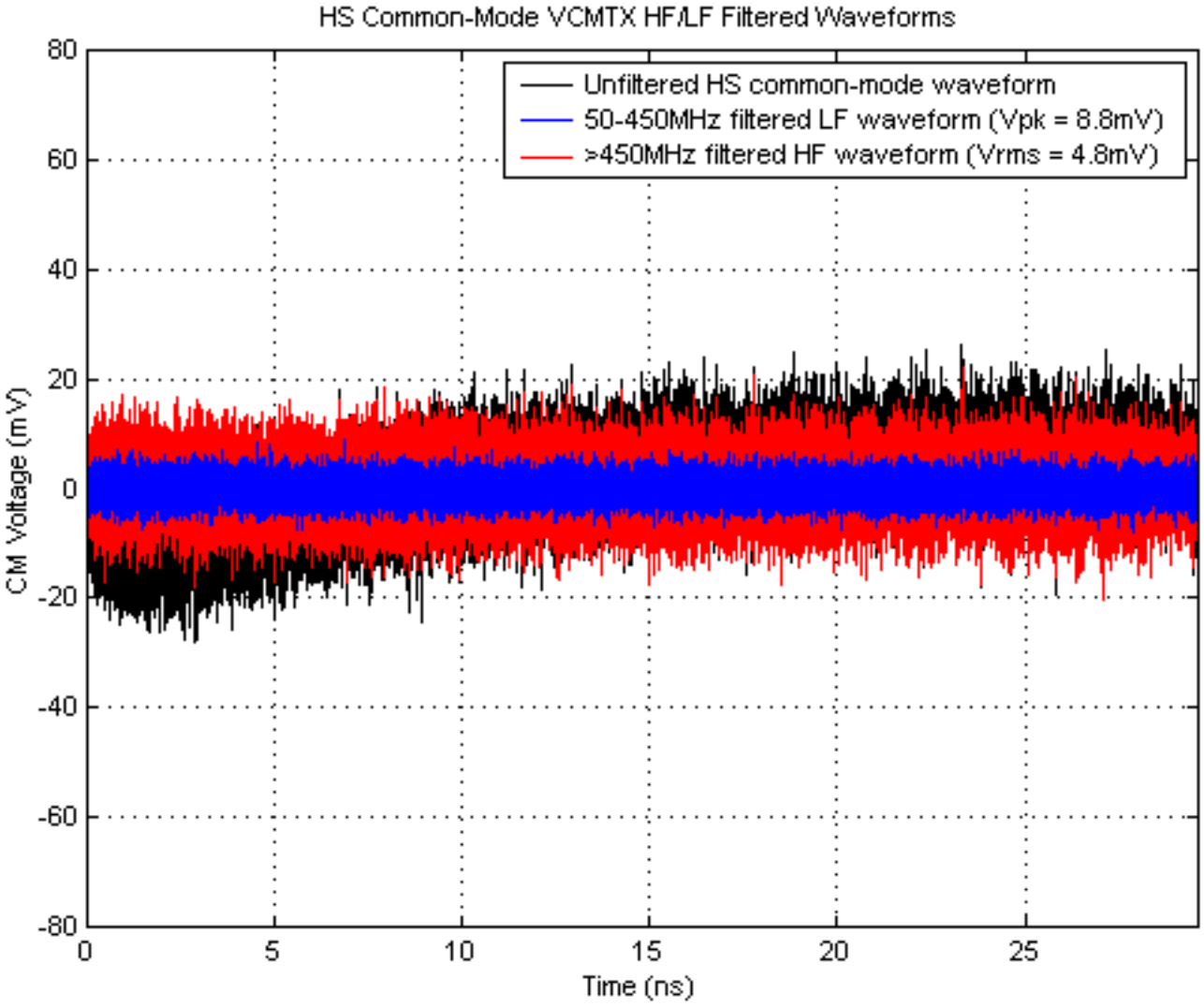

Figure 36: HS-TX 20%-80% Rise Time (Data Lane 0, ZID=100)

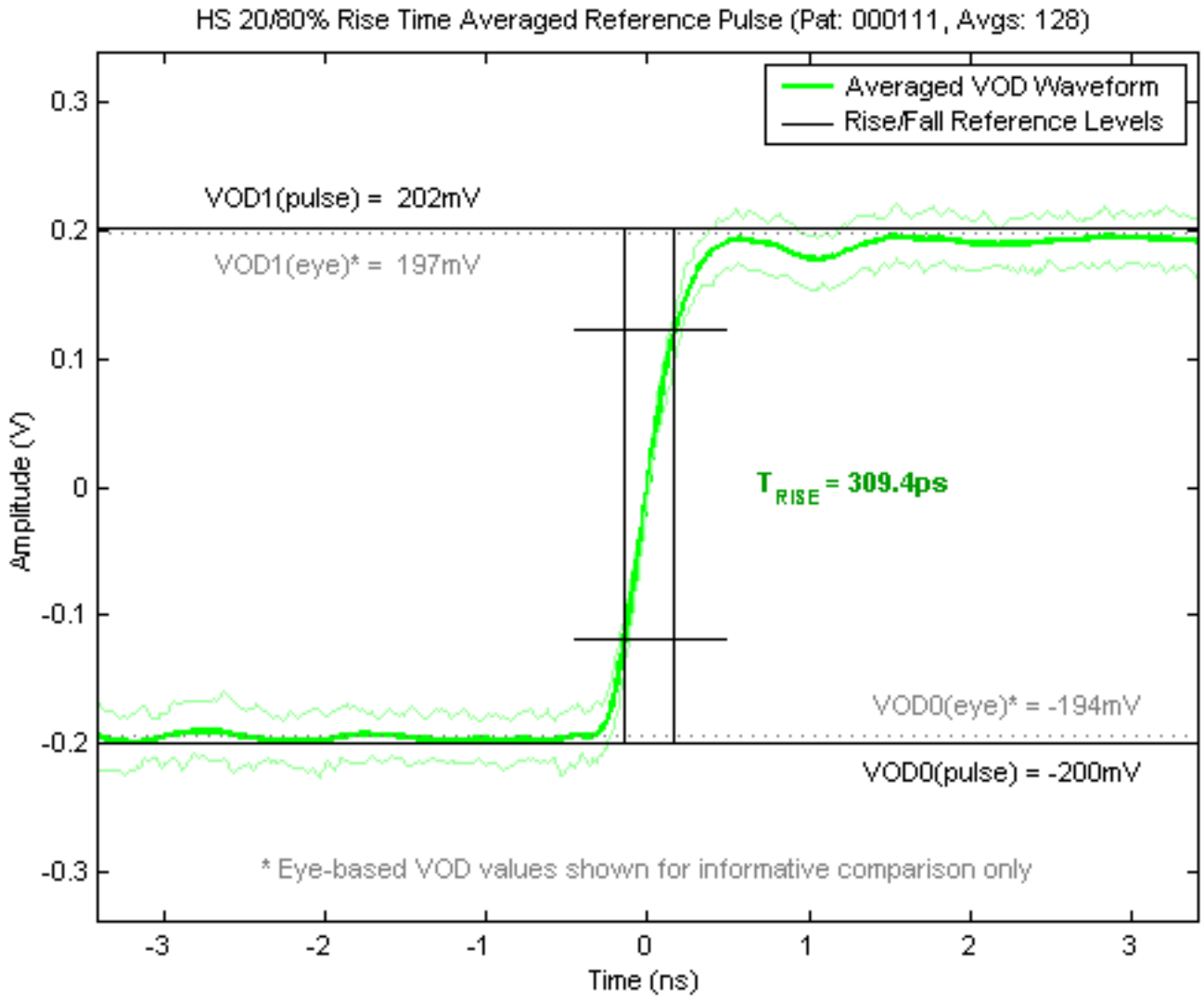

Figure 37: HS-TX 20%-80% Rise Time (Data Lane 0, ZID=125)

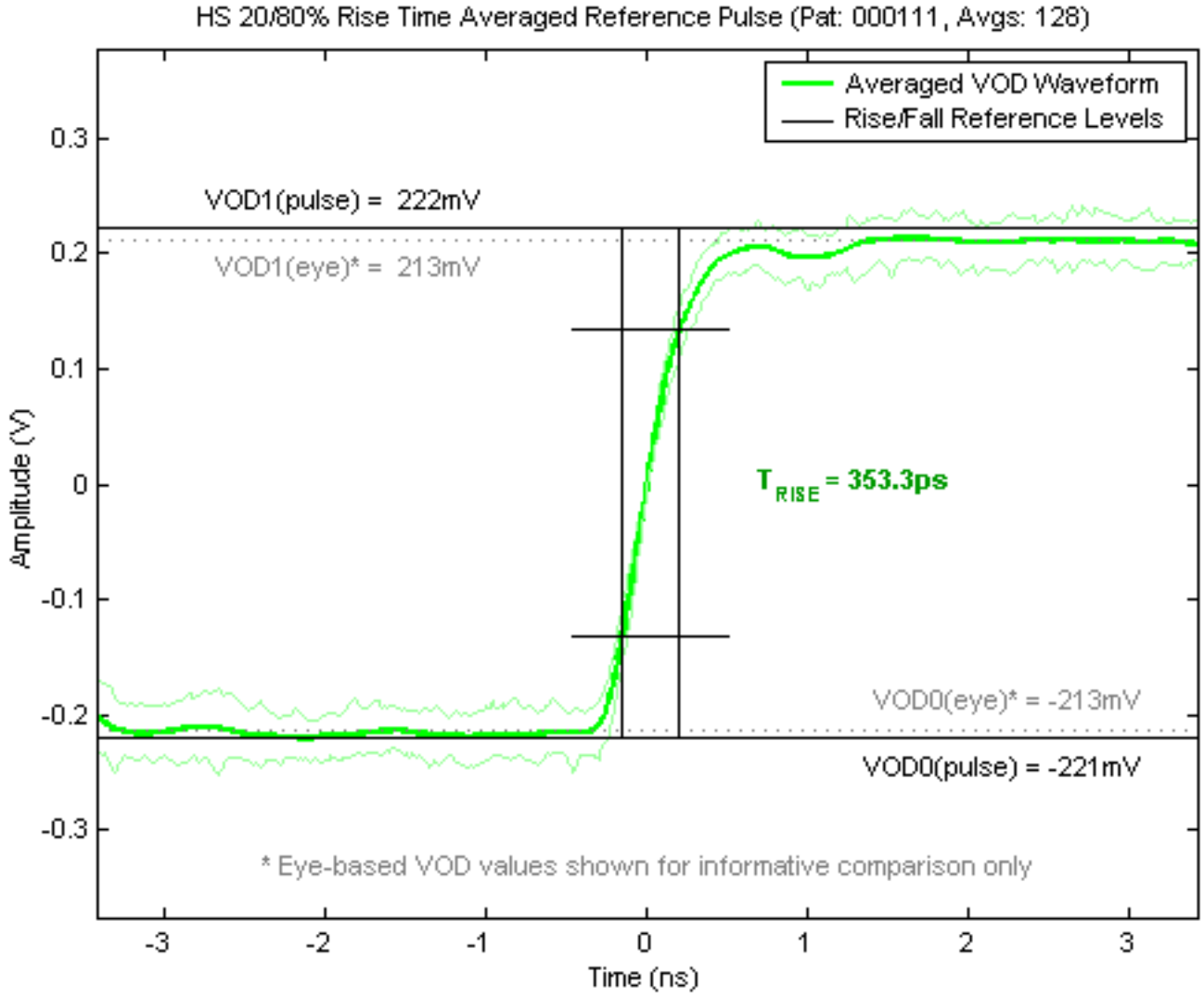

Figure 38: HS-TX 20%-80% Rise Time (Data Lane 0, ZID=80)

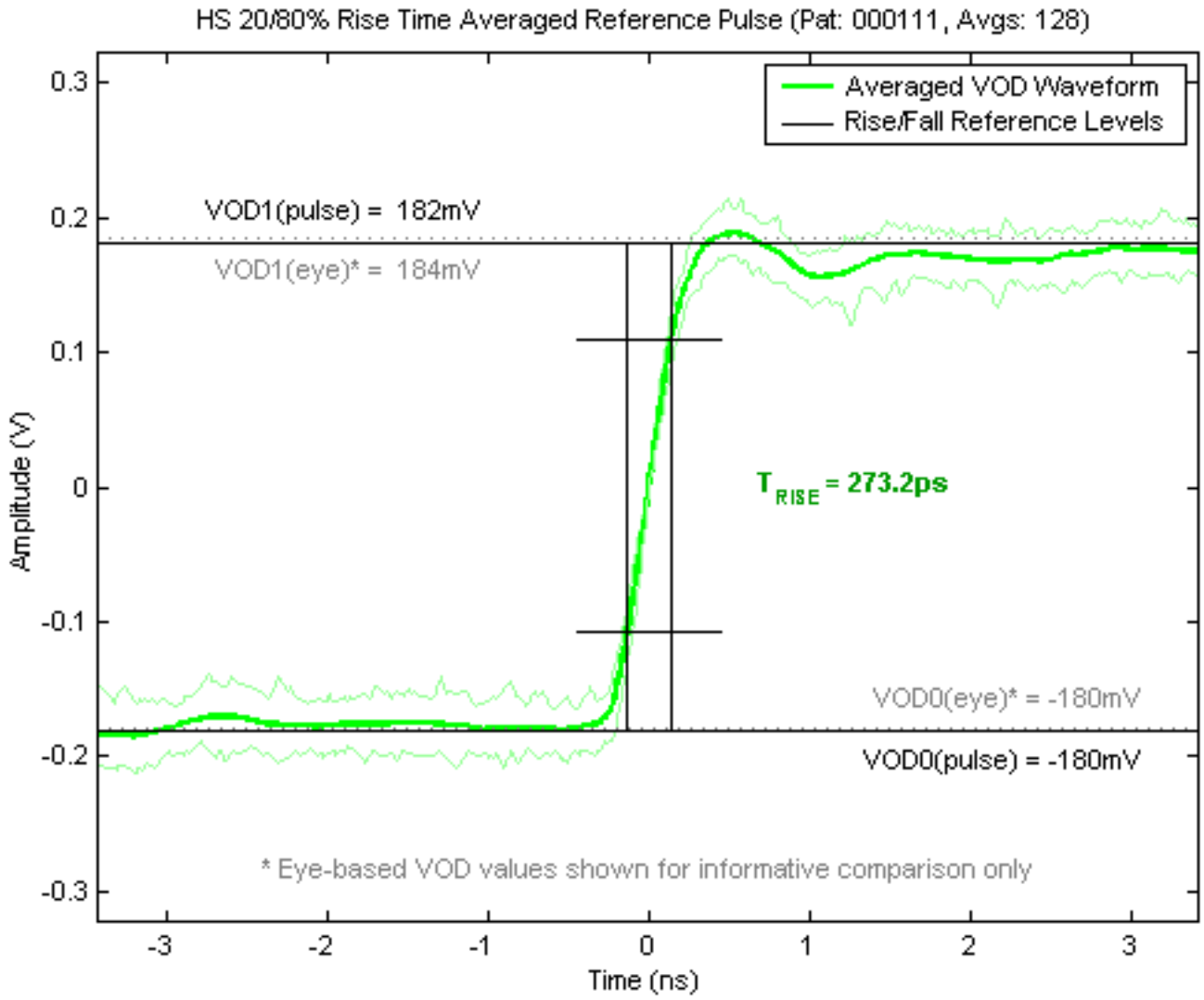

Figure 39: HS-TX 20%-80% Fall Time (Data Lane 0, ZID=100)

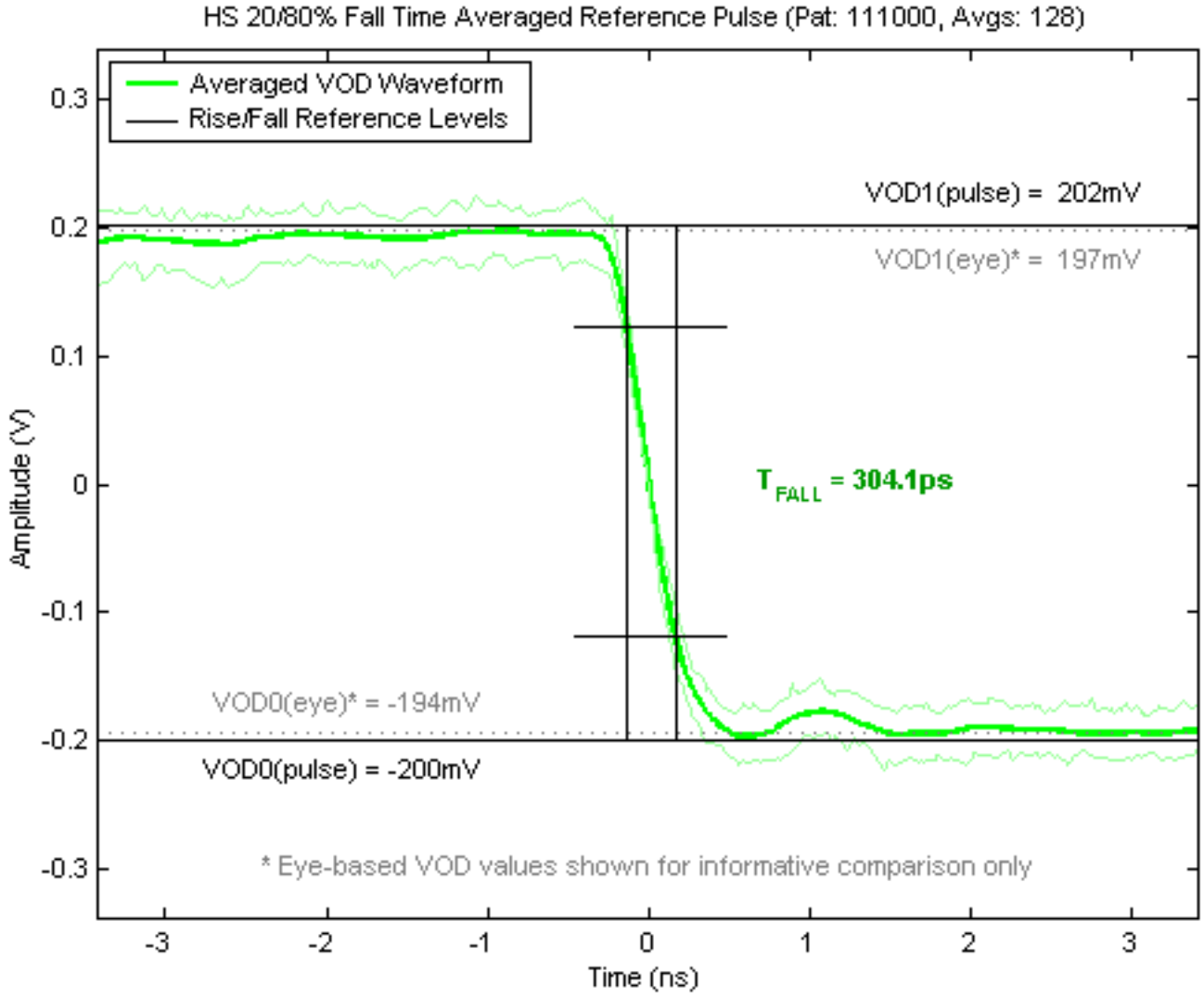

Figure 40: HS-TX 20%-80% Fall Time (Data Lane 0, ZID=125)

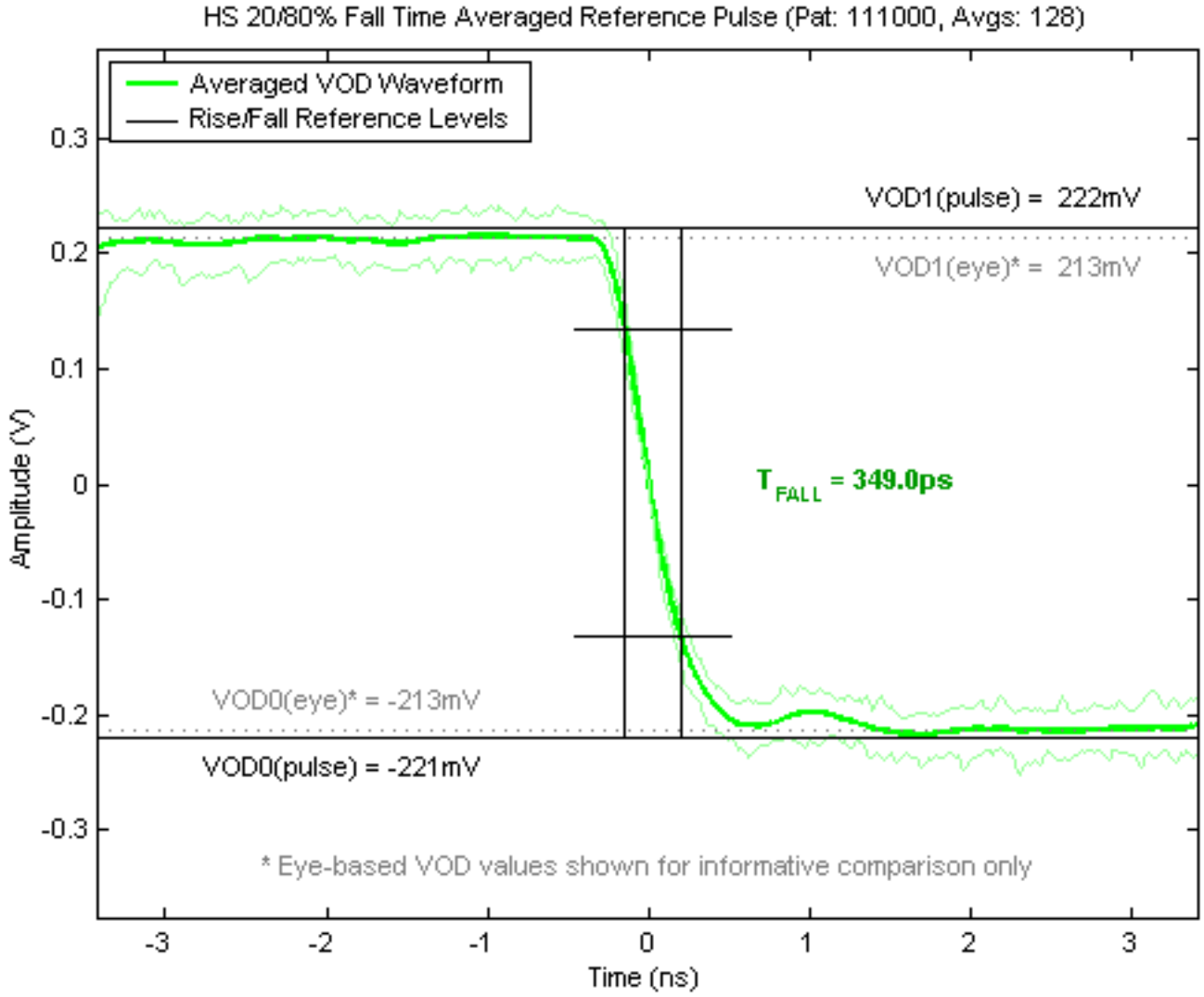

Figure 41: HS-TX 20%-80% Fall Time (Data Lane 0, ZID=80)

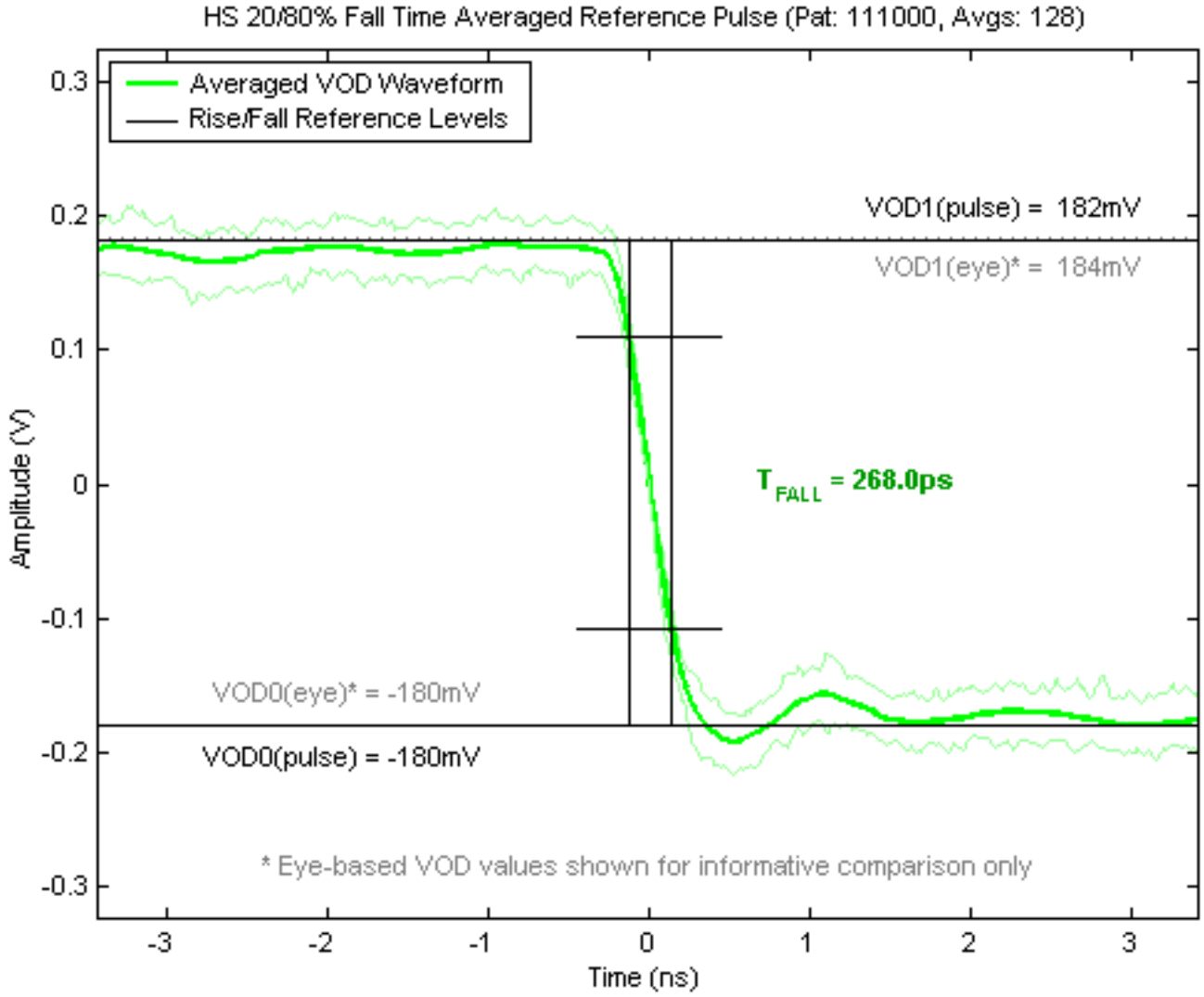

Figure 42: THS-TRAIL, TREOT, TEOT, TCLK-POST Intervals (Data Lane 0, ZID=100)

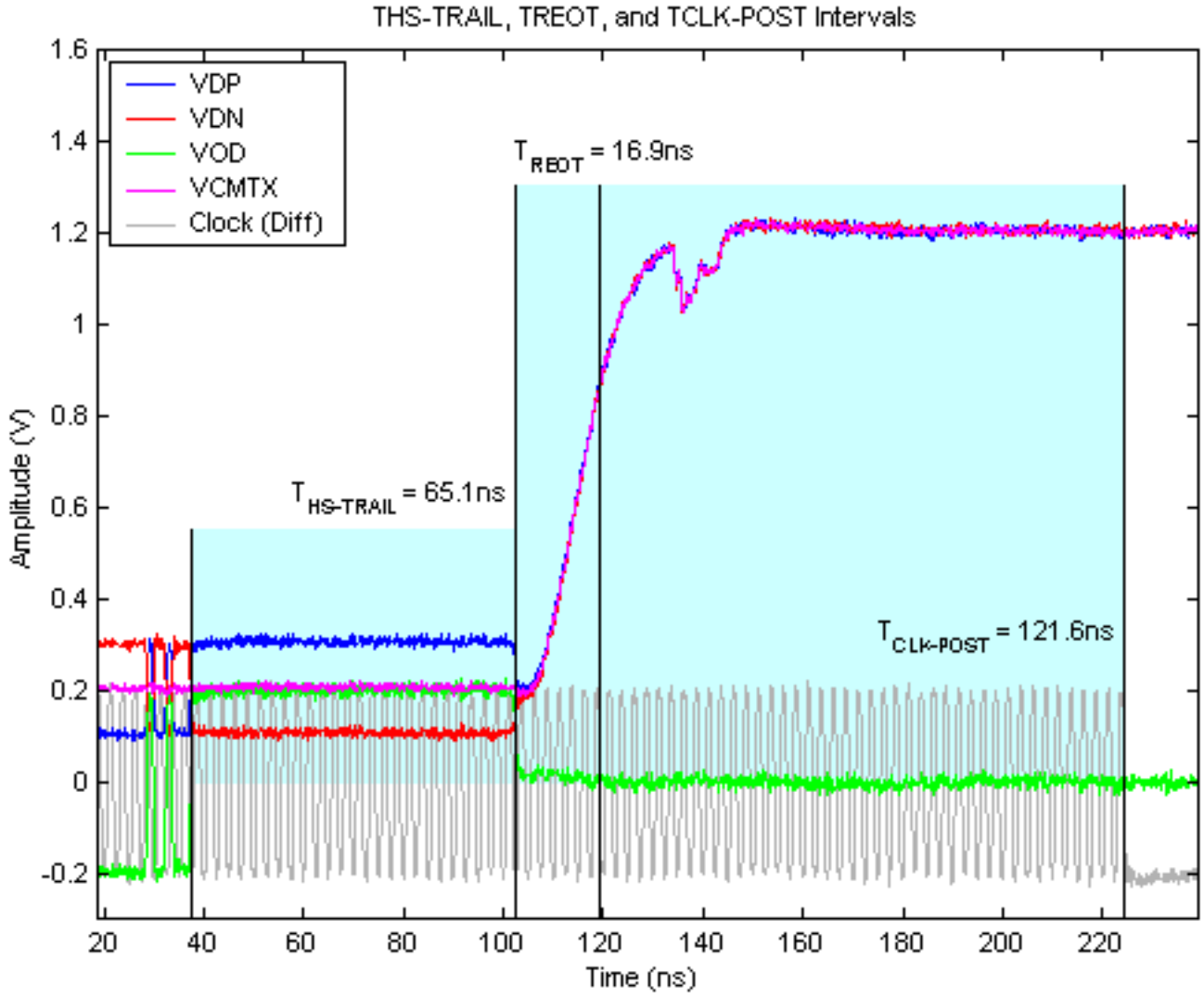

Figure 43: HS Eye Diagram (Data Lane 0, ZID=100) (INFORMATIVE)

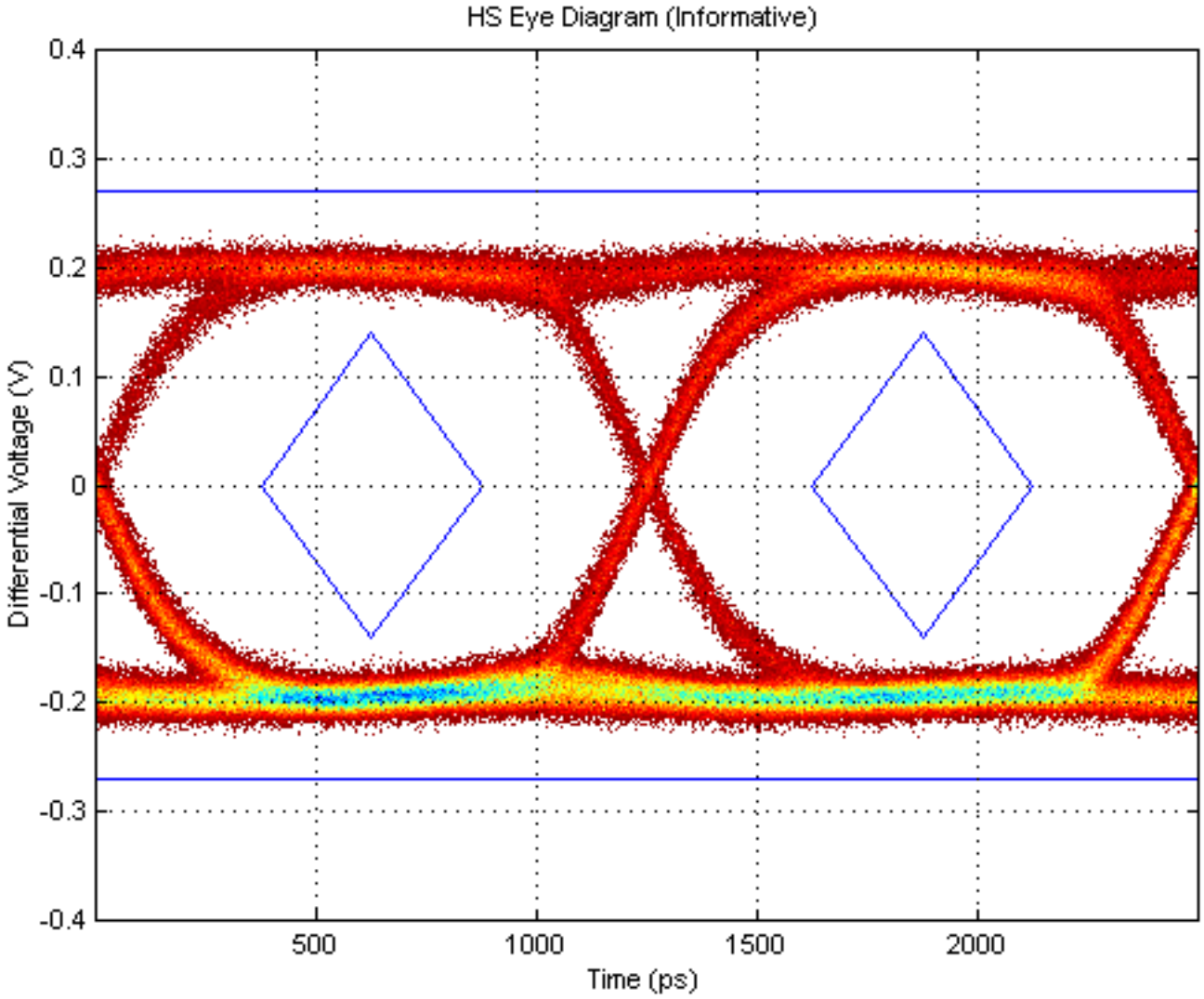

Figure 44: HS Eye Diagram (Data Lane 0, ZID=125) (INFORMATIVE)

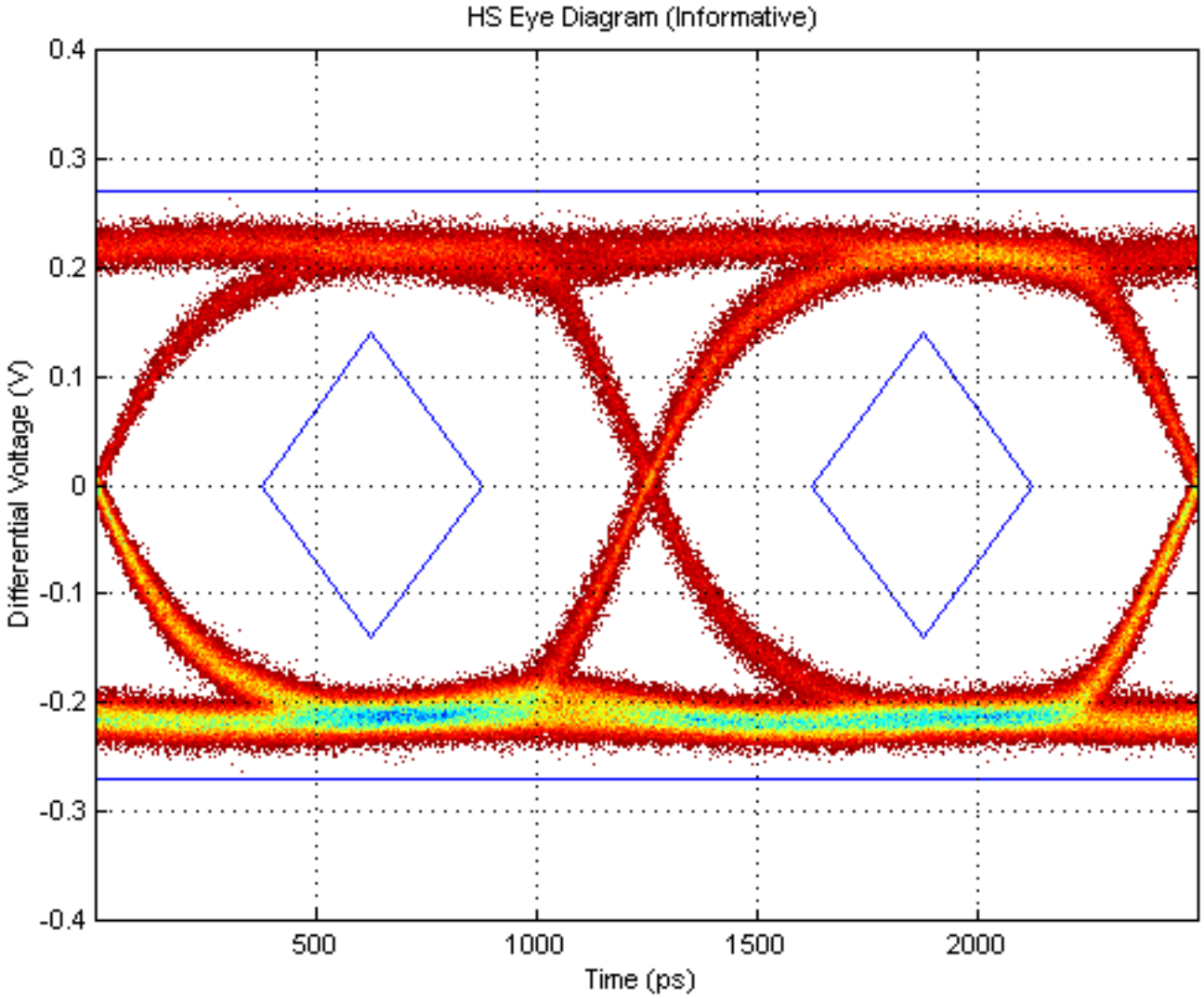

Figure 45: HS Eye Diagram (Data Lane 0, ZID=80) (INFORMATIVE)

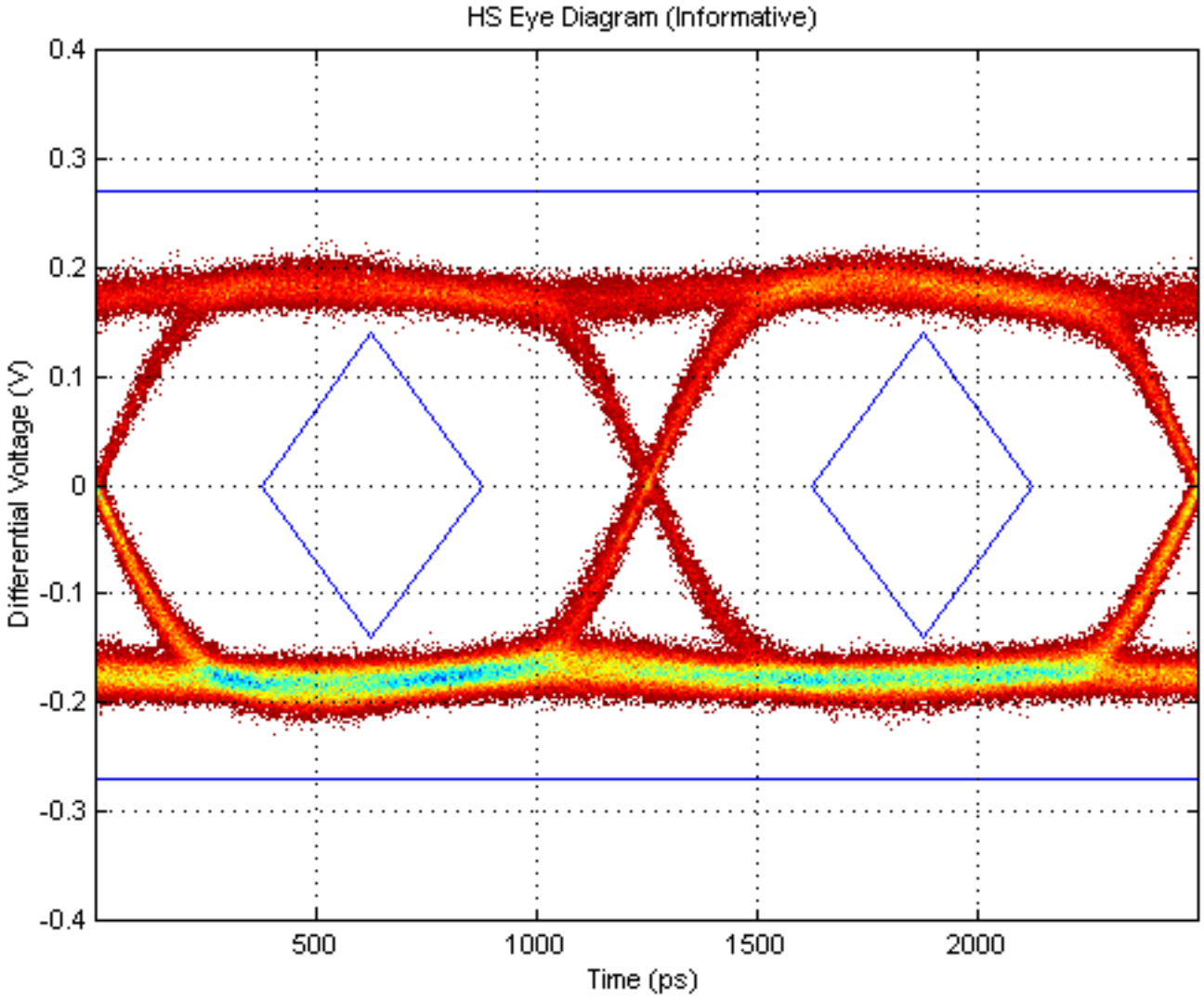

Figure 46: Clock TLPX, TCLK-PREPARE, and TCLK-ZERO Intervals (ZID=100)

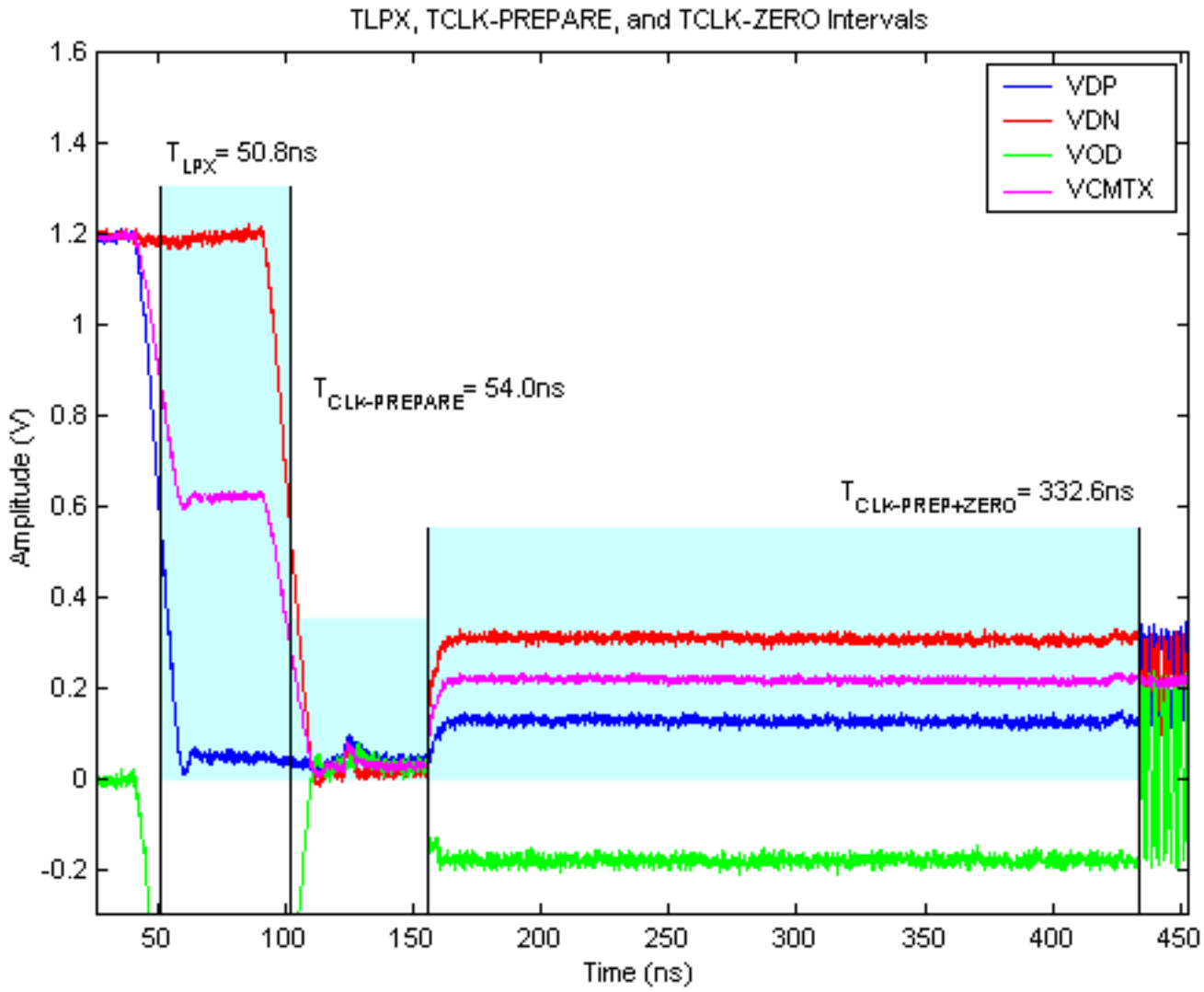

Figure 47: HS-TX Differential Voltage VOD(1) (Clock Lane, ZID=100)

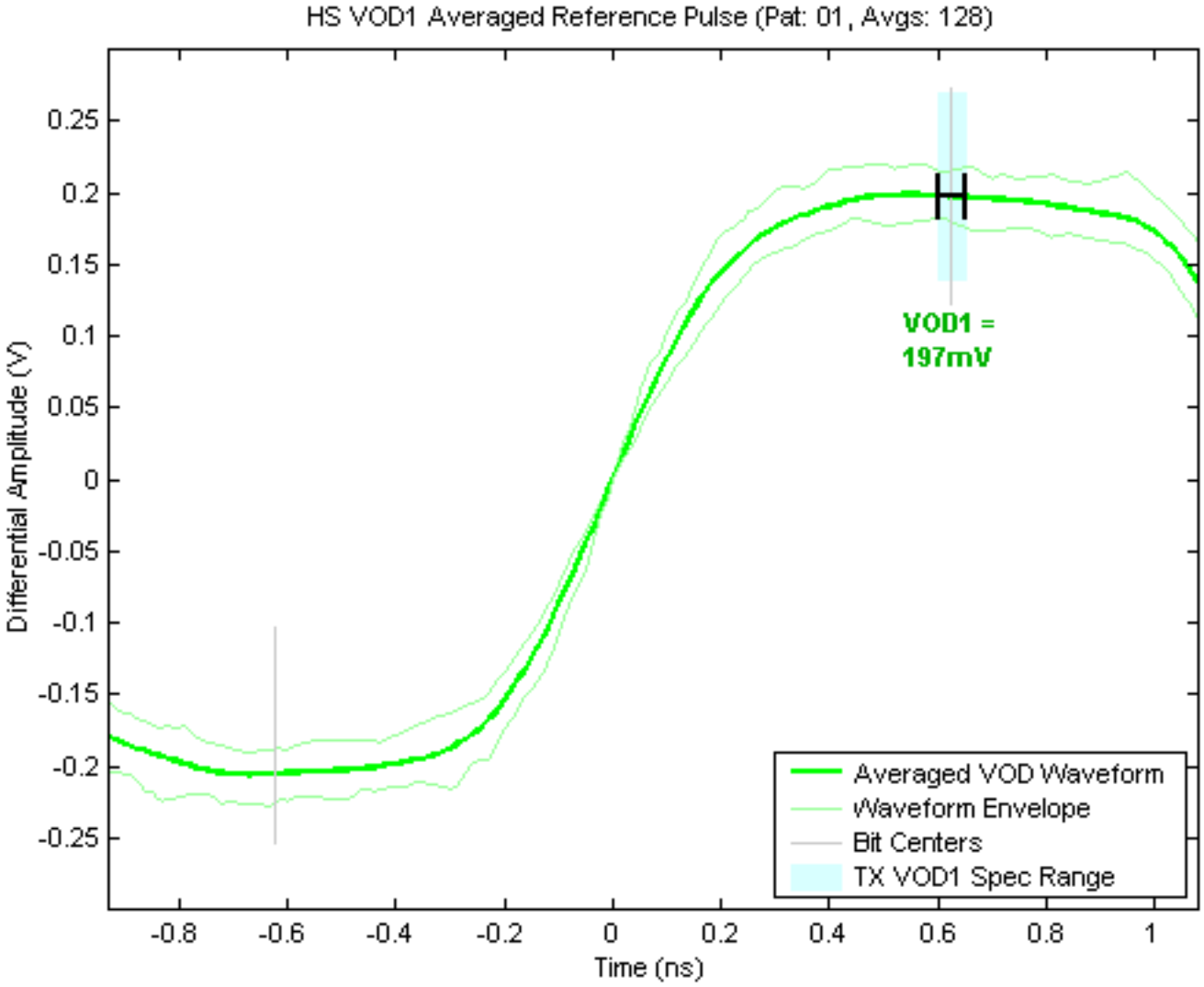

Figure 48: HS-TX Differential Voltage VOD(0) (Clock Lane, ZID=100)

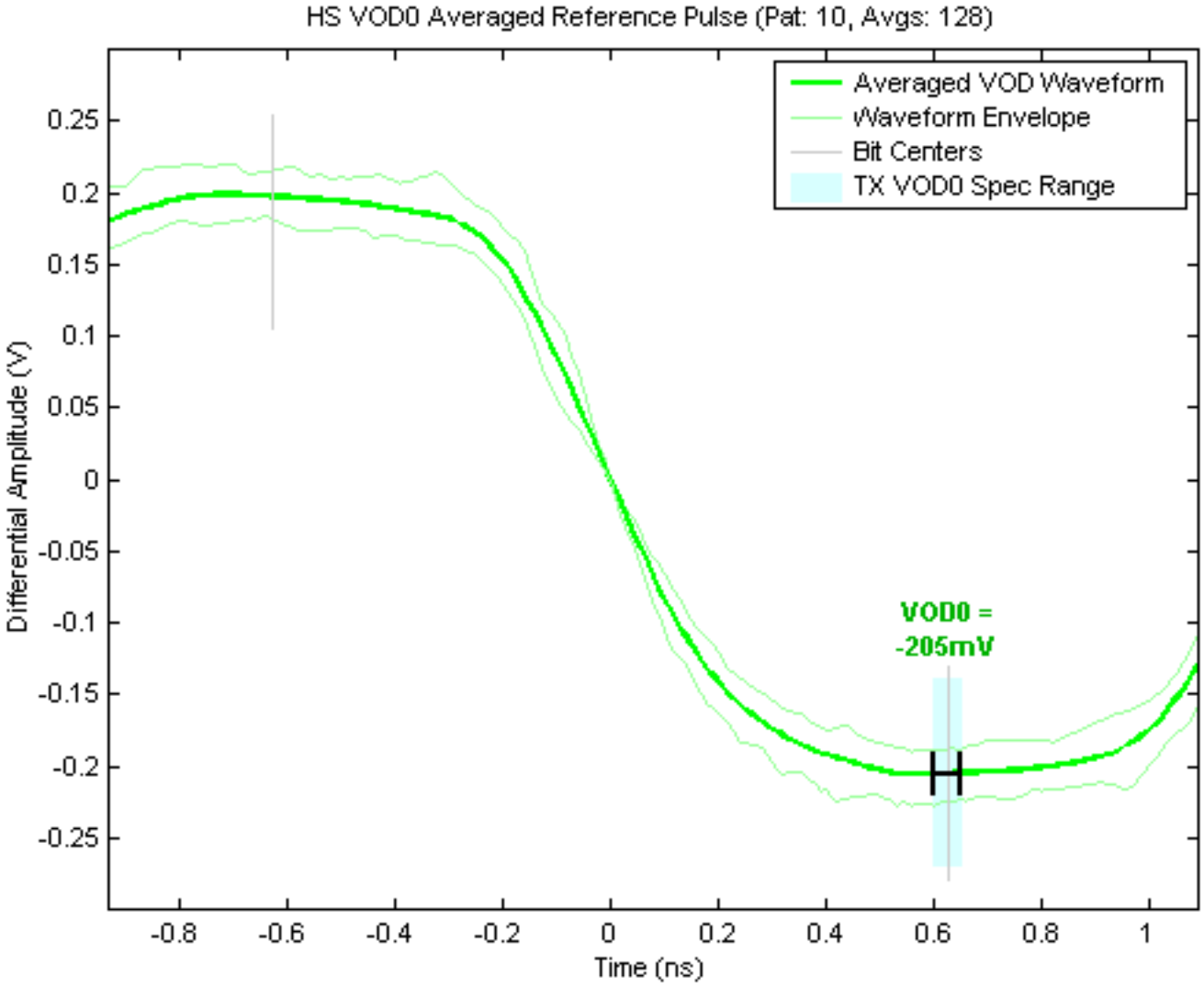

Figure 49: HS-TX Differential Voltage VOD(1) (Clock Lane, ZID=125)

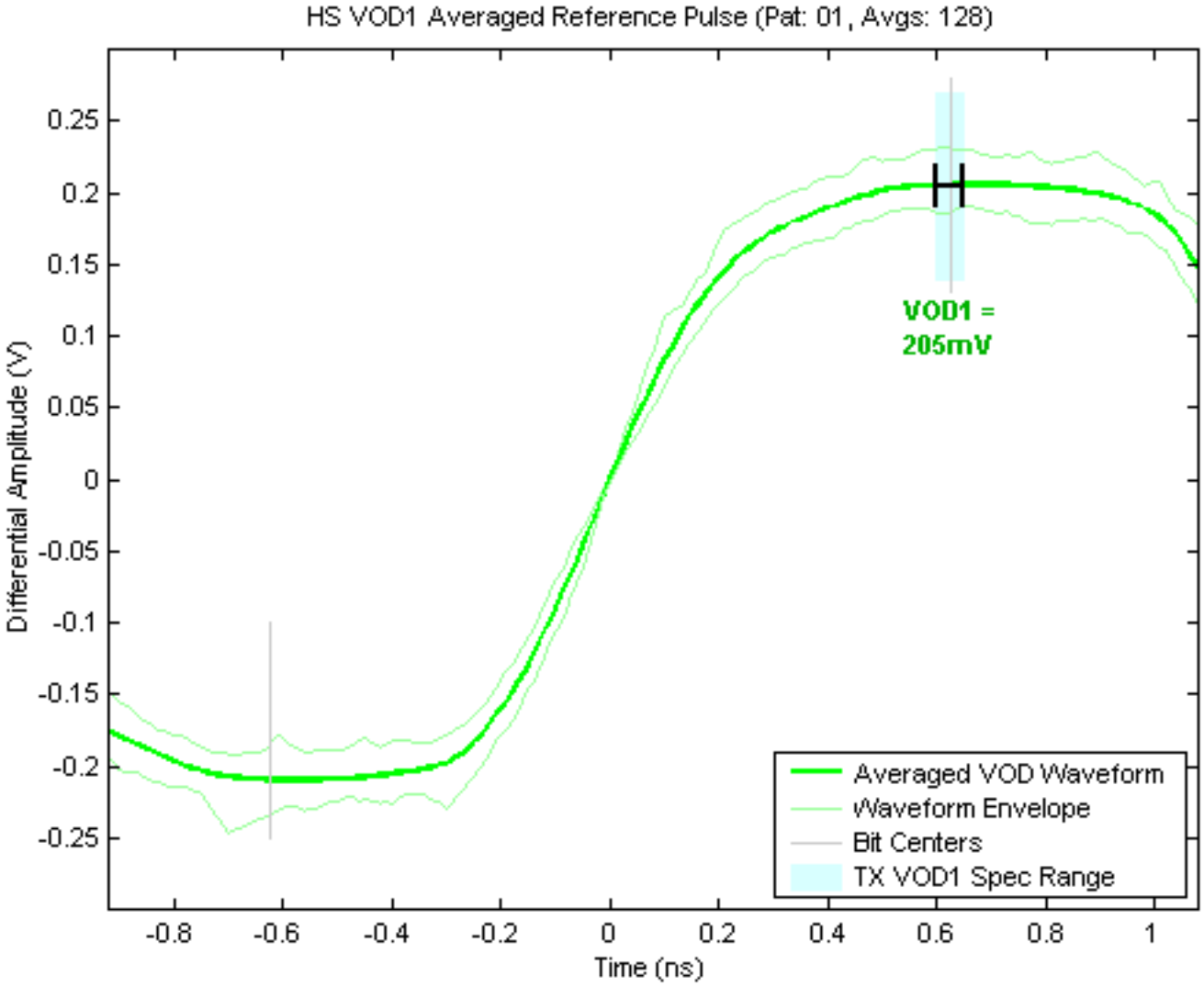

Figure 50: HS-TX Differential Voltage VOD(0) (Clock Lane, ZID=125)

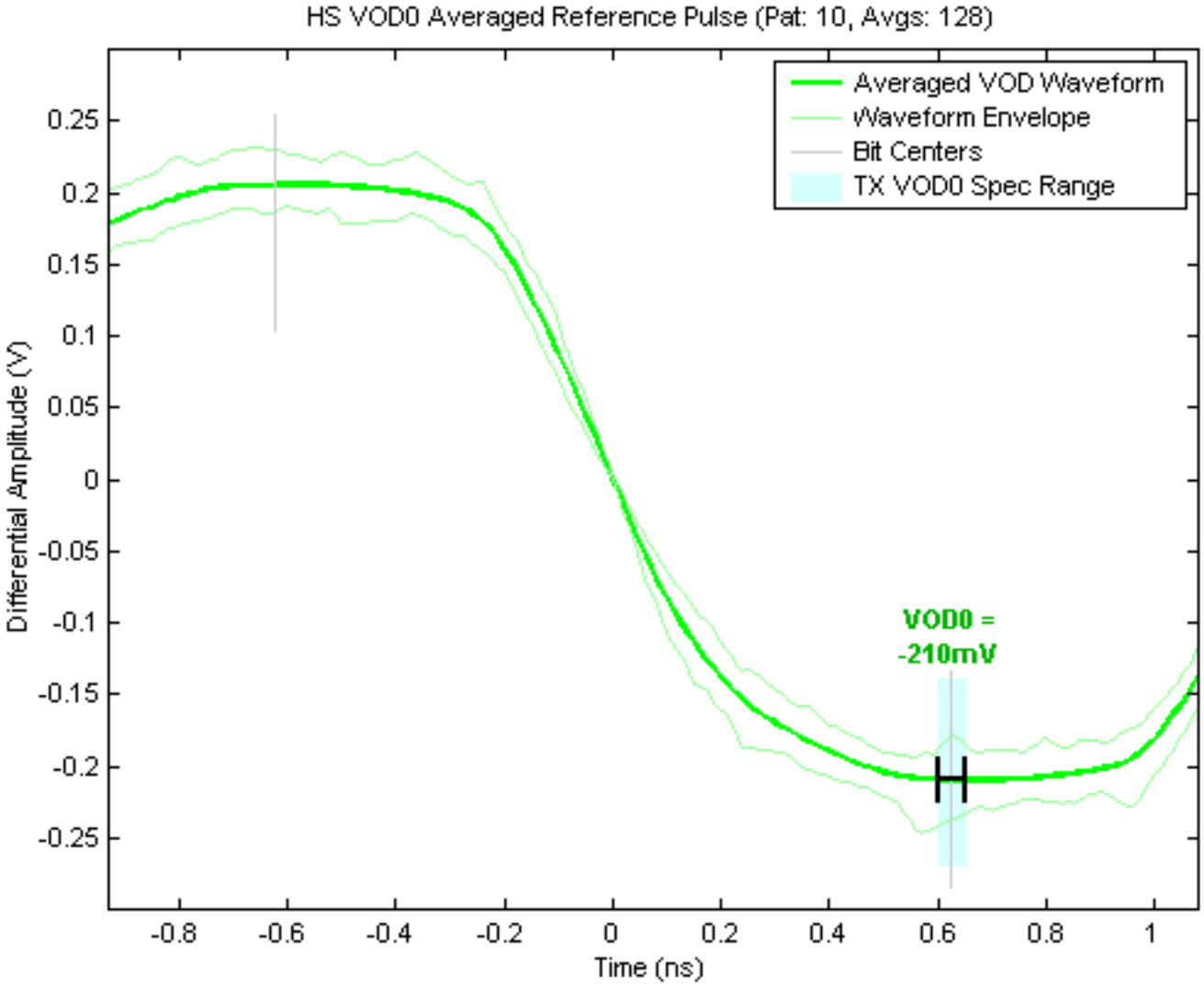

Figure 51: HS-TX Differential Voltage VOD(1) (Clock Lane, ZID=80)

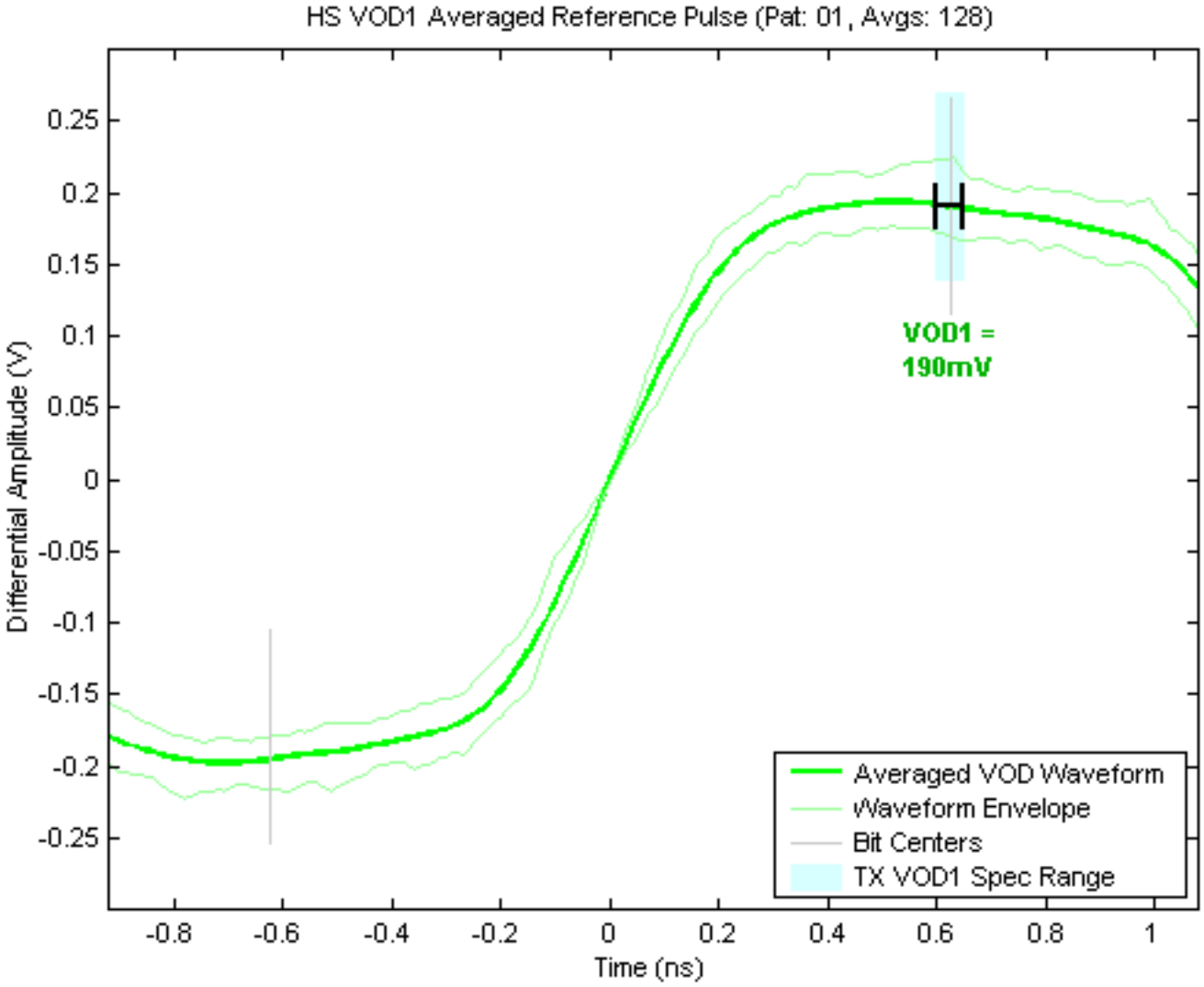

Figure 52: HS-TX Differential Voltage VOD(0) (Clock Lane, ZID=80)

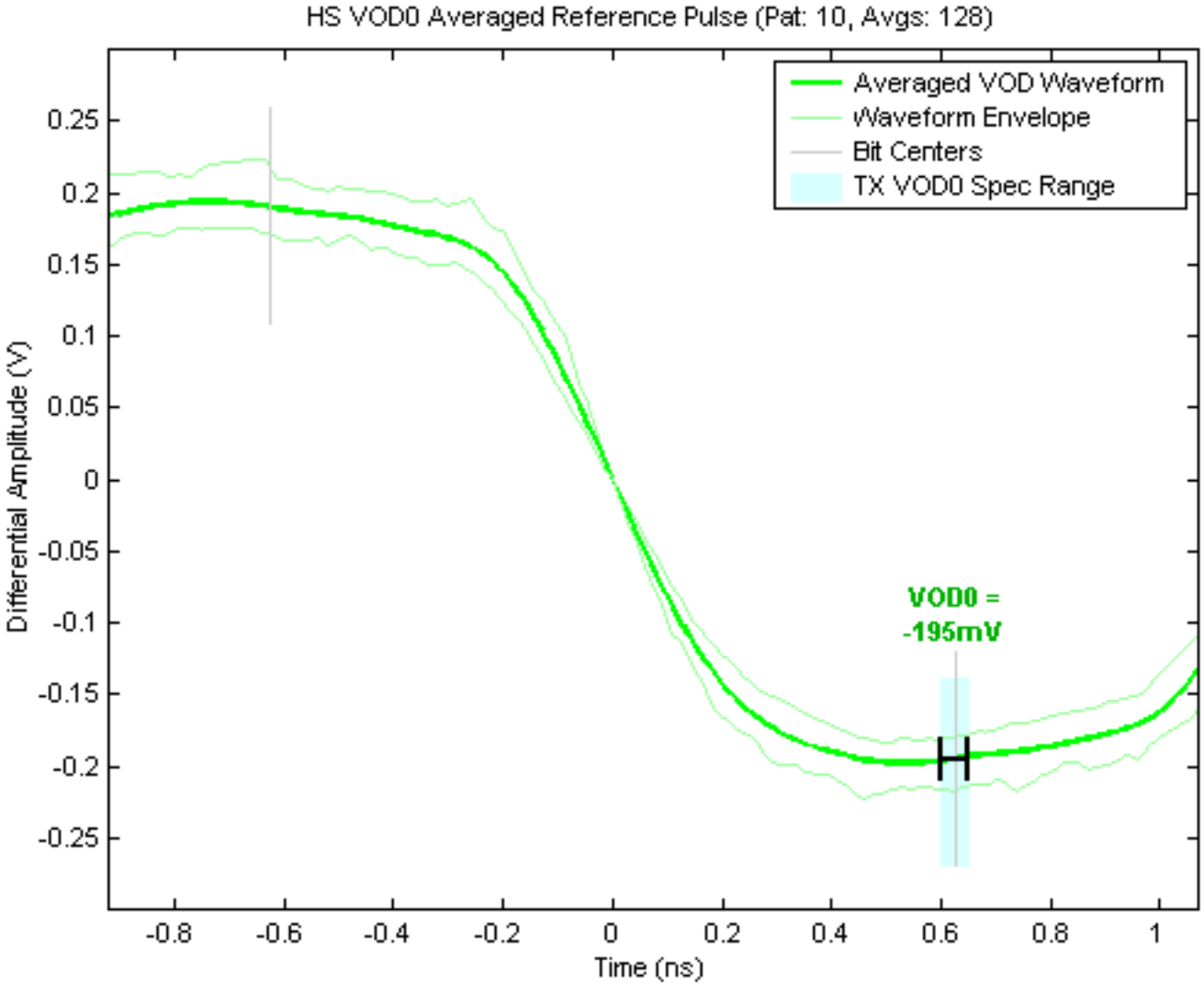

Figure 53: HS-TX Single-Ended Voltage Dp VOHHS (Clock Lane, ZID=100)

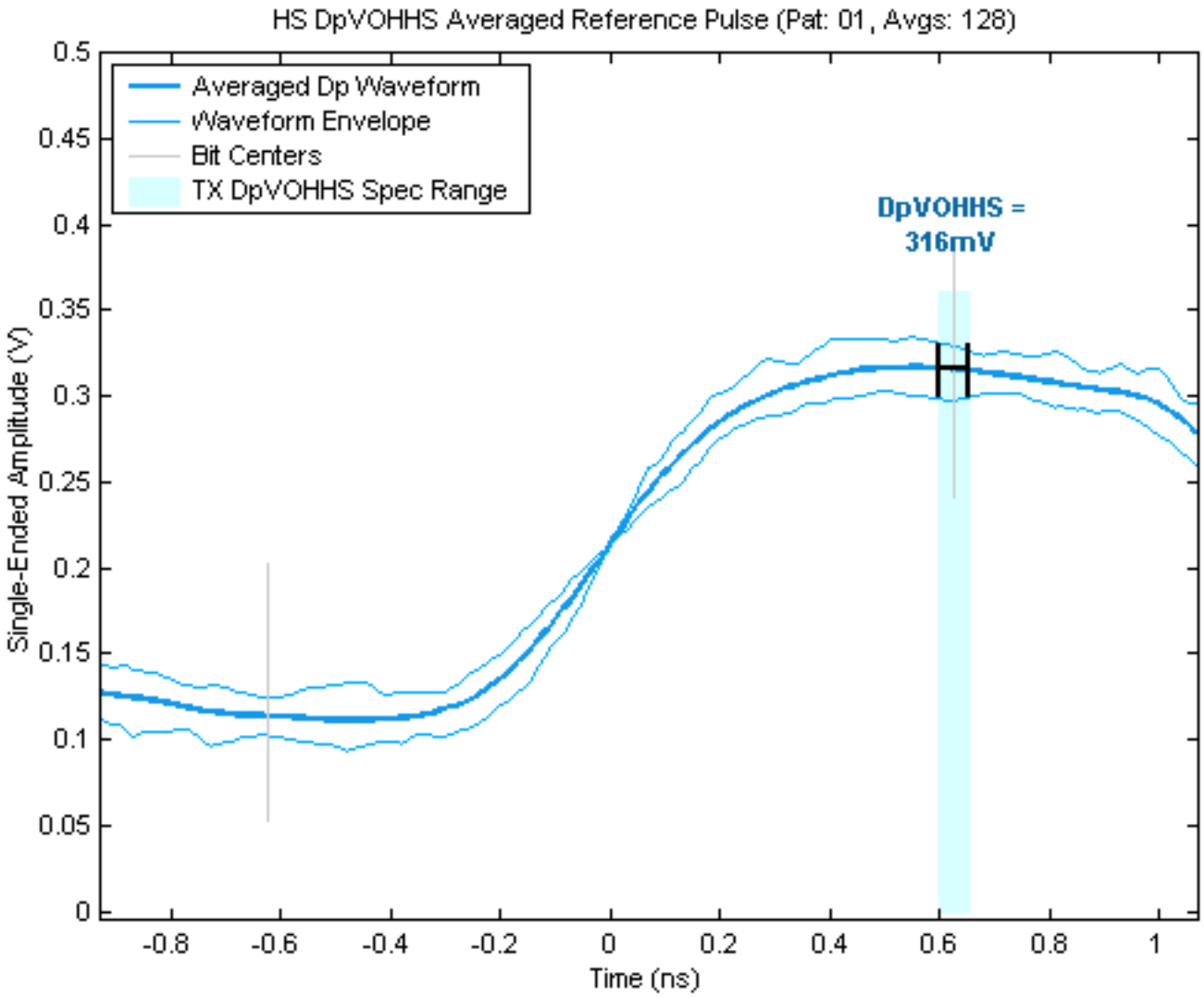

Figure 54: HS-TX Single-Ended Voltage Dn VOHHS (Clock Lane, ZID=100)

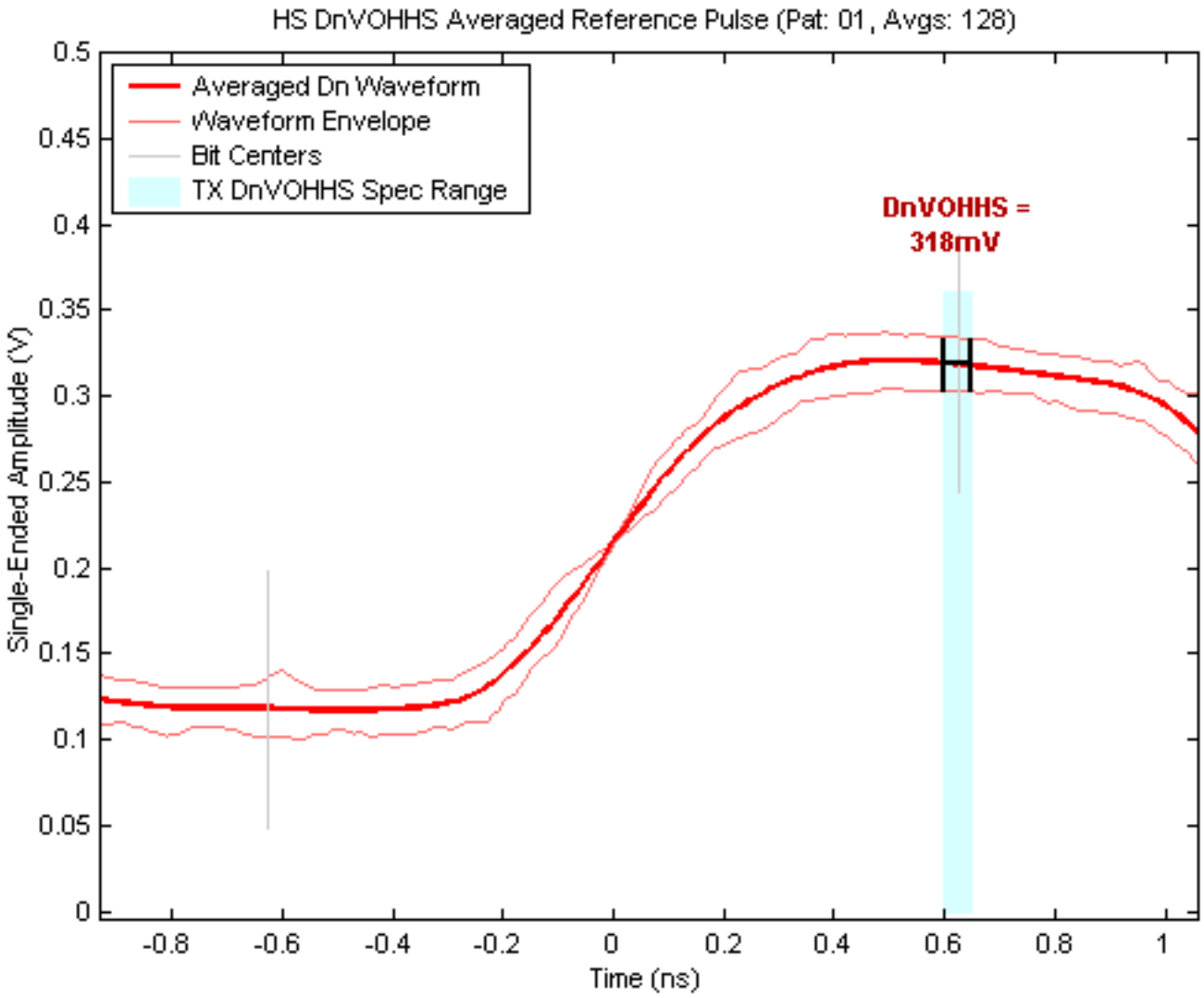

Figure 55: HS-TX Single-Ended Voltage Dp VOHHS (Clock Lane, ZID=125)

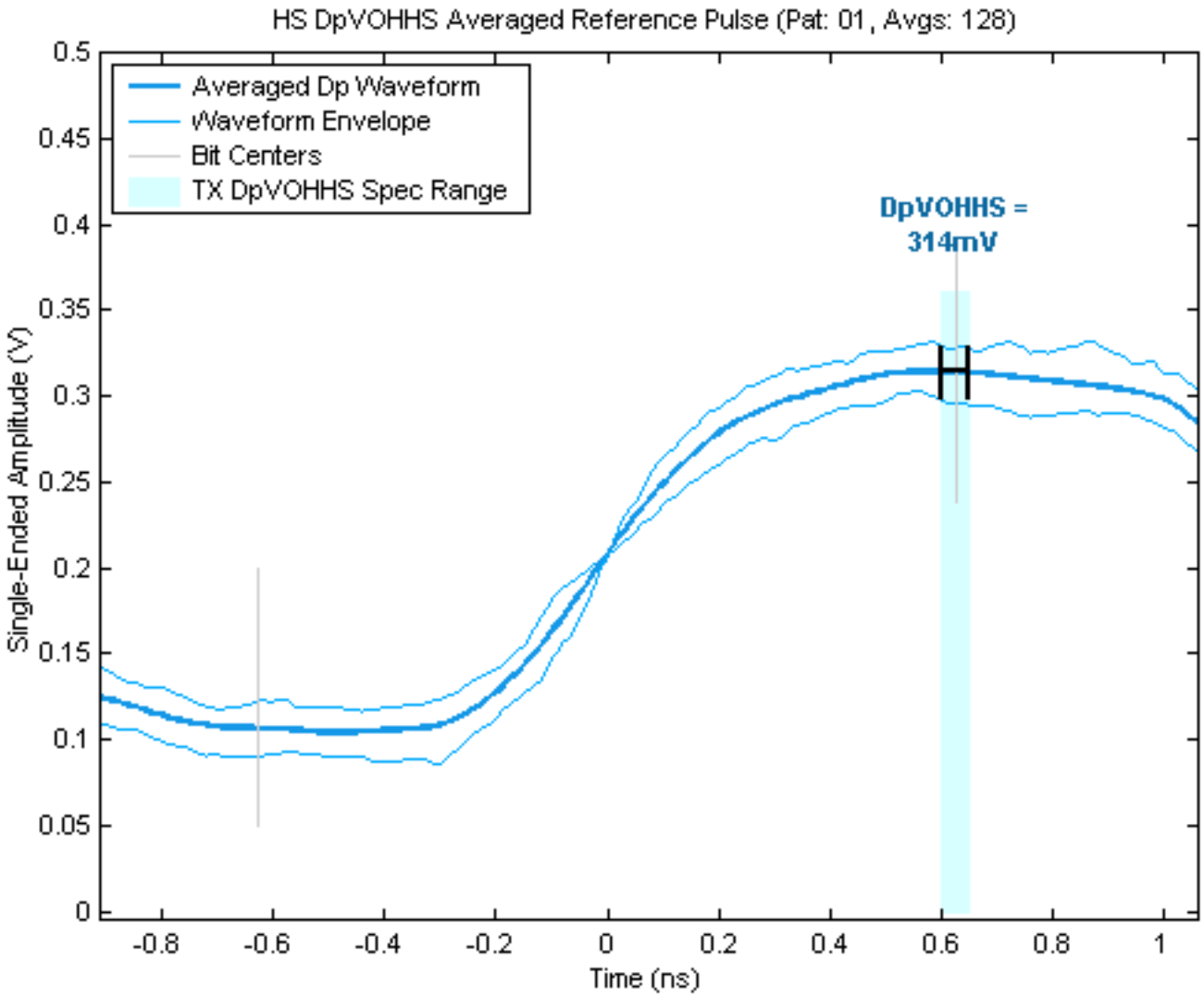

Figure 56: HS-TX Single-Ended Voltage Dn VOHHS (Clock Lane, ZID=125)

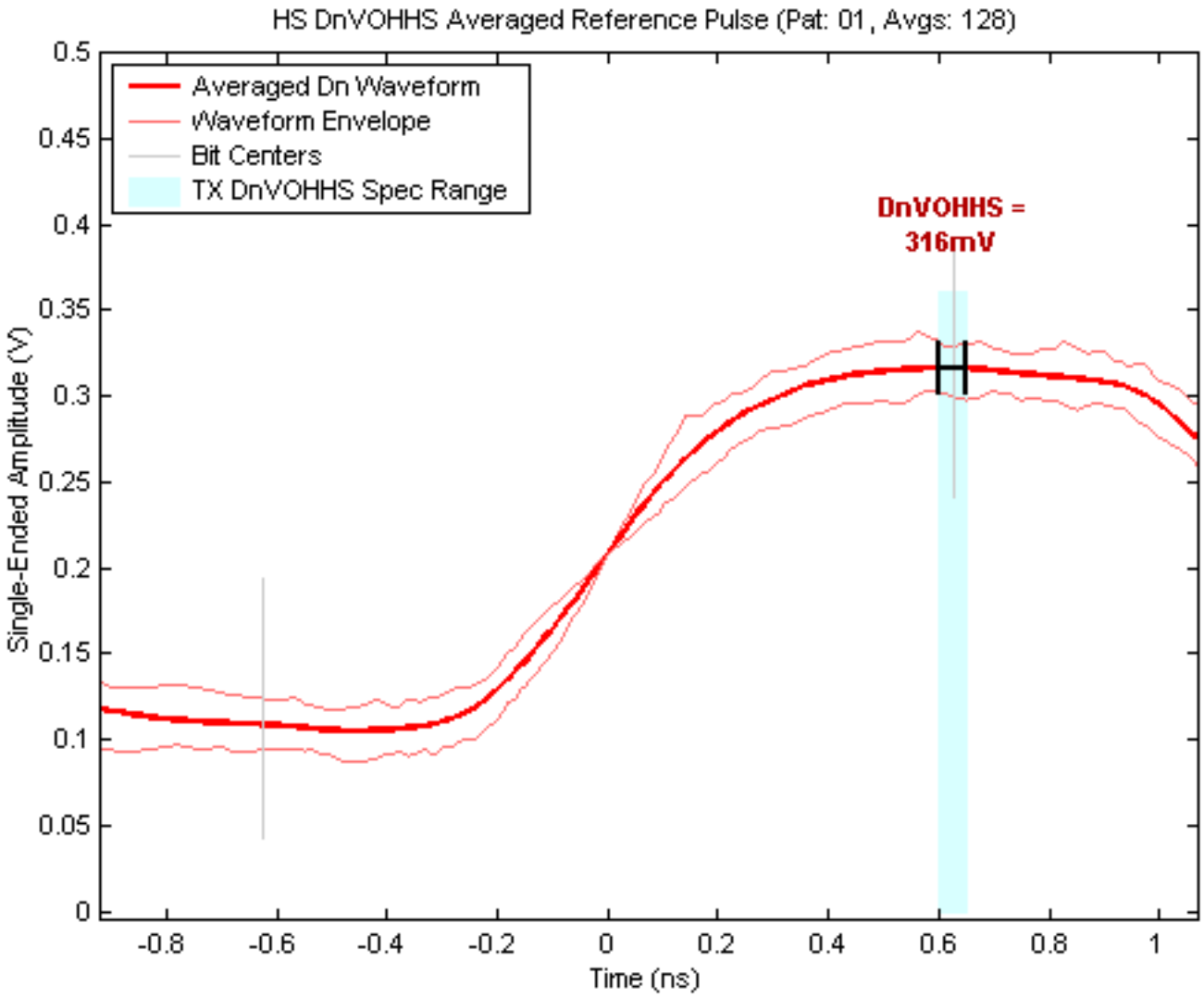

Figure 57: HS-TX Single-Ended Voltage Dp VOHHS (Clock Lane, ZID=80)

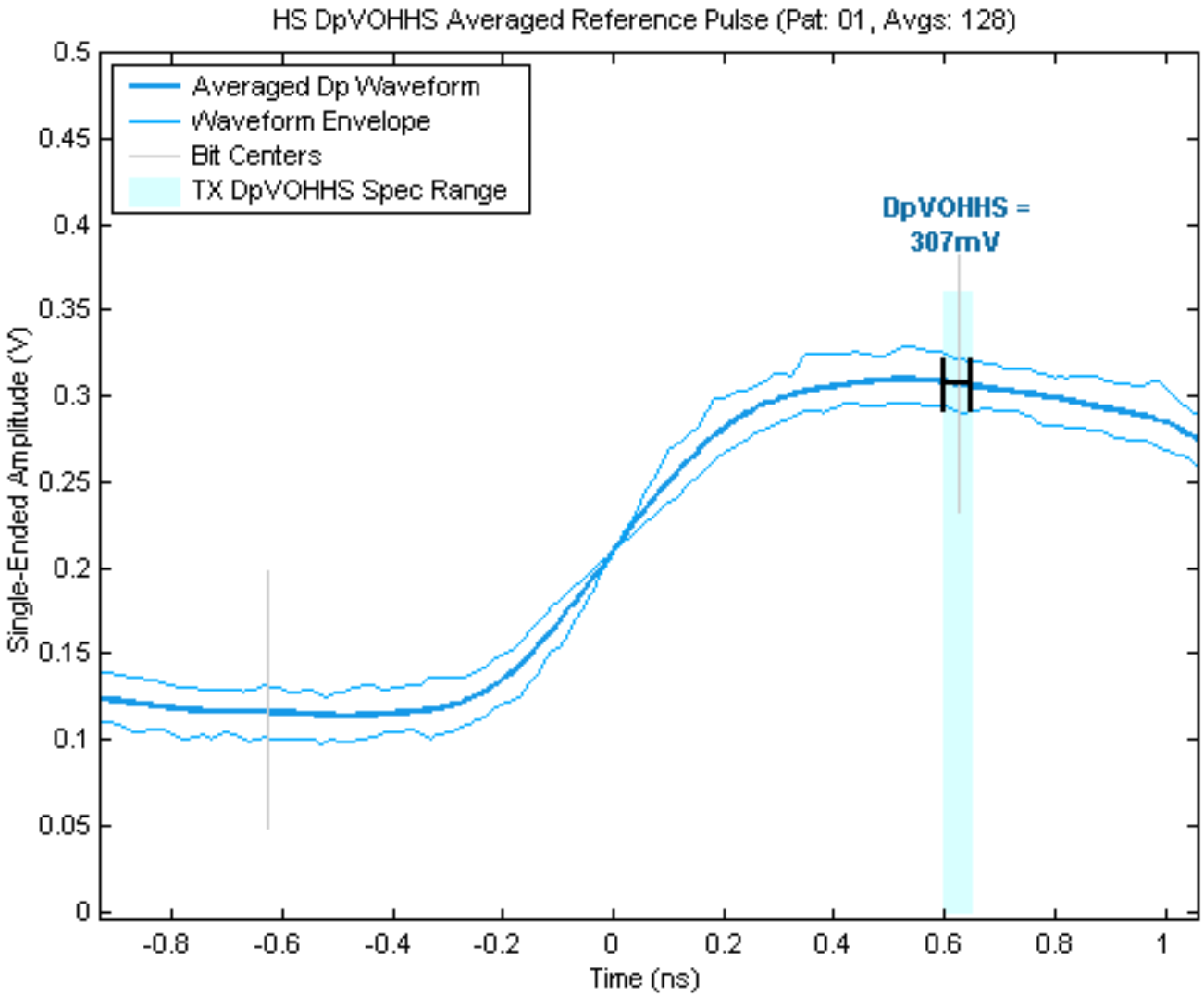

Figure 58: HS-TX Single-Ended Voltage Dn VOHHS (Clock Lane, ZID=80)

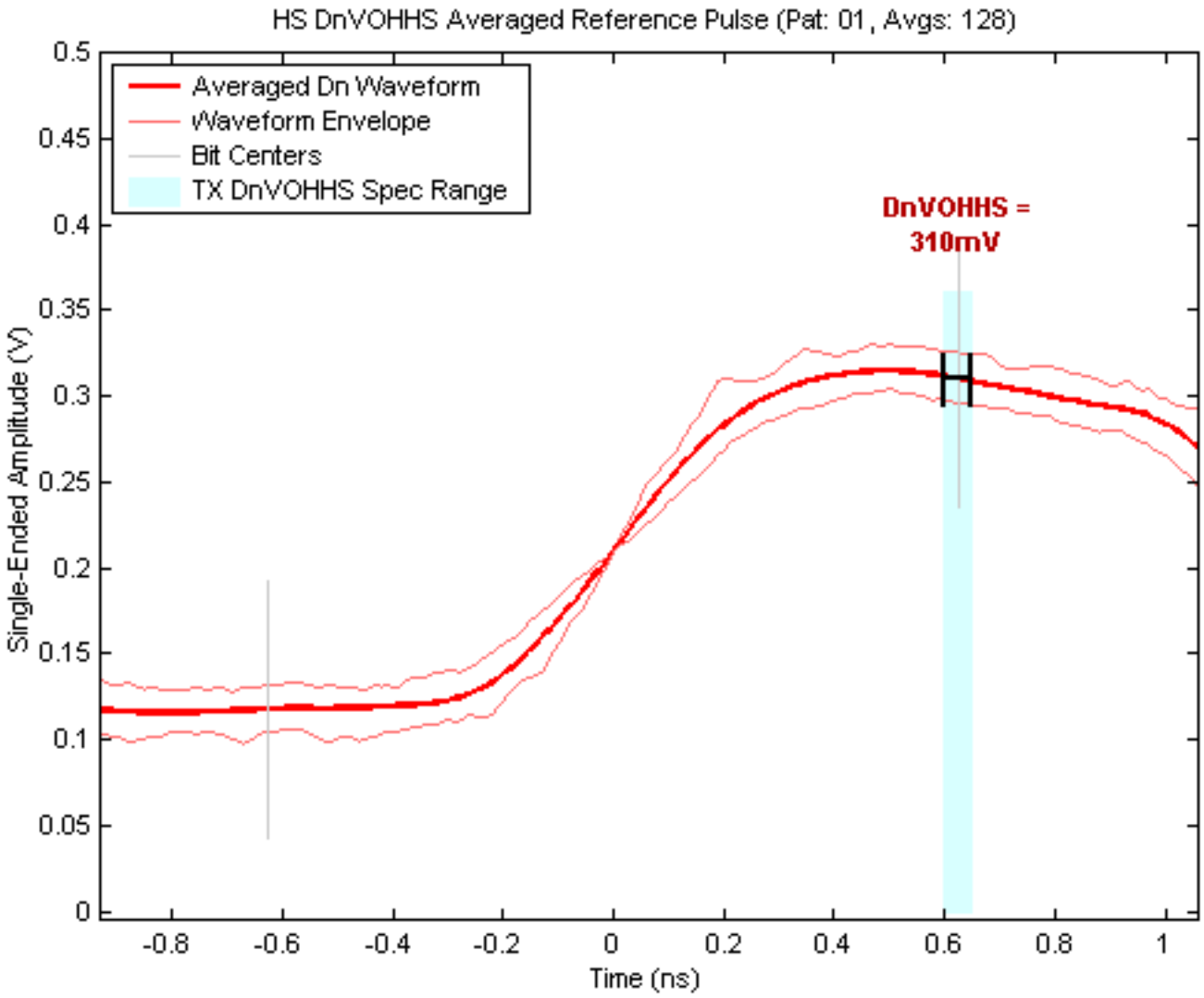

Figure 59: HS-TX Static Common-Mode Voltages, VCMTX (Clock Lane, ZID=100)

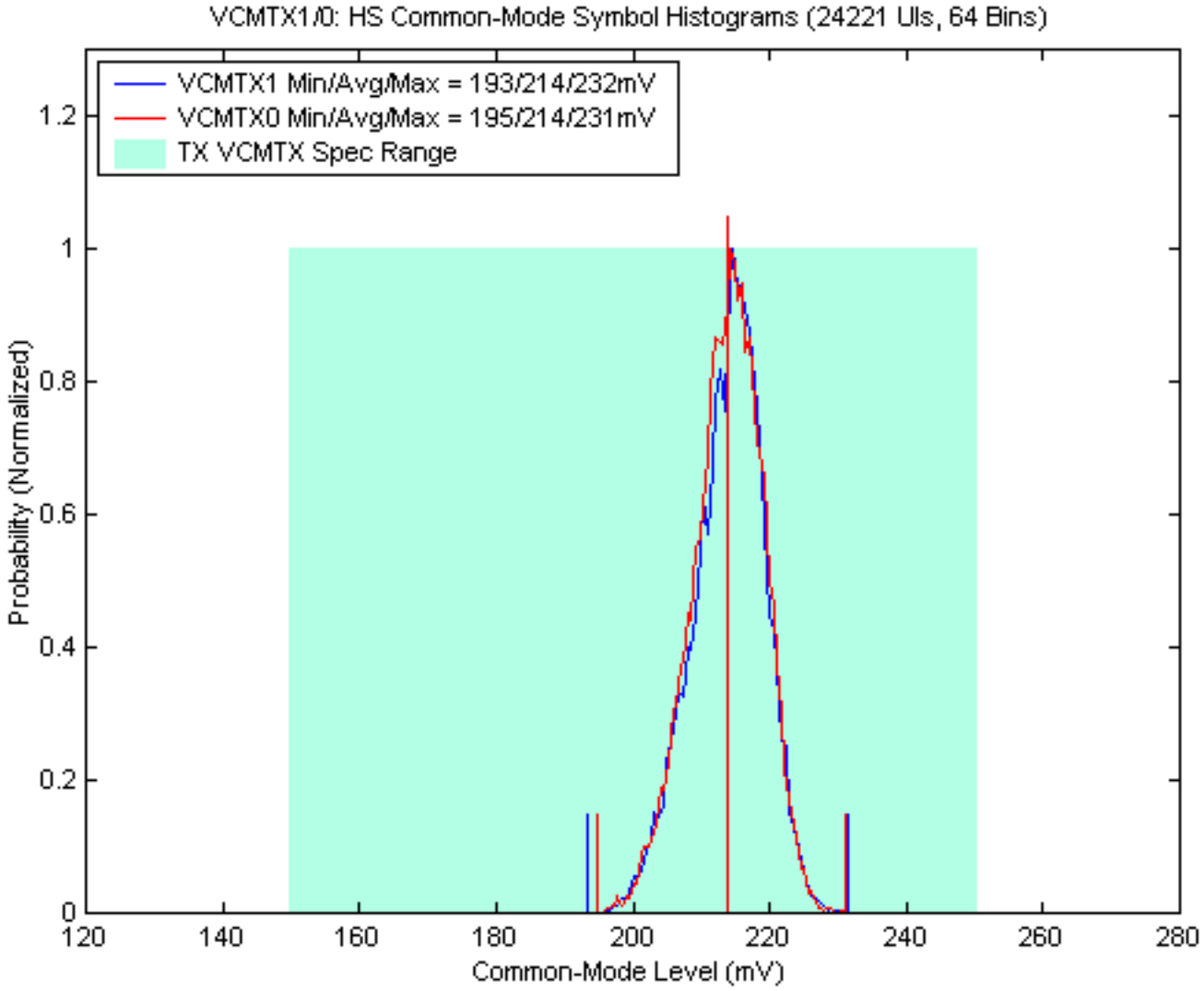

Figure 60: HS-TX Static Common-Mode Voltages, VCMTX (Clock Lane, ZID=125)

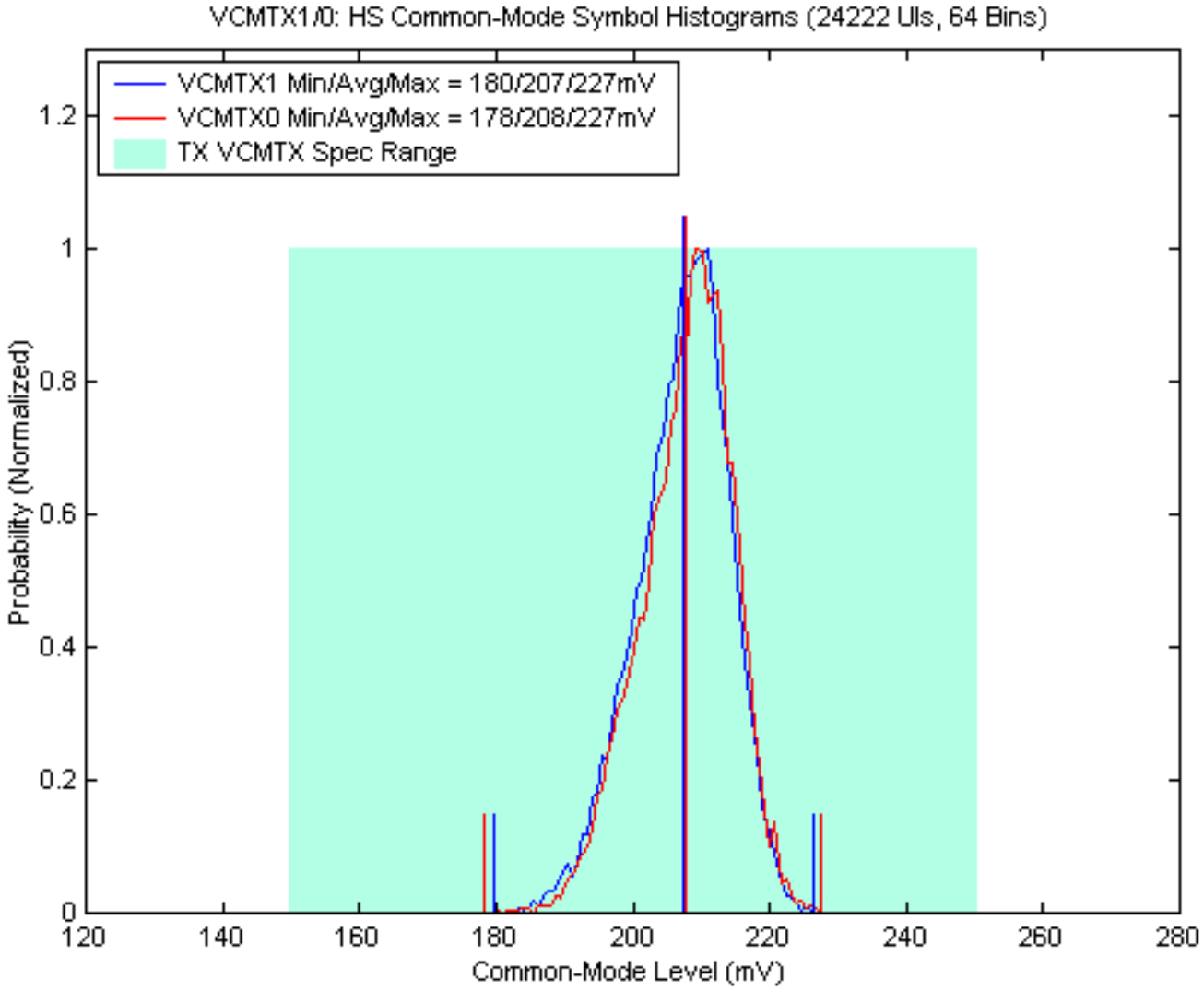

Figure 61: HS-TX Static Common-Mode Voltages, VCMTX (Clock Lane, ZID=80)

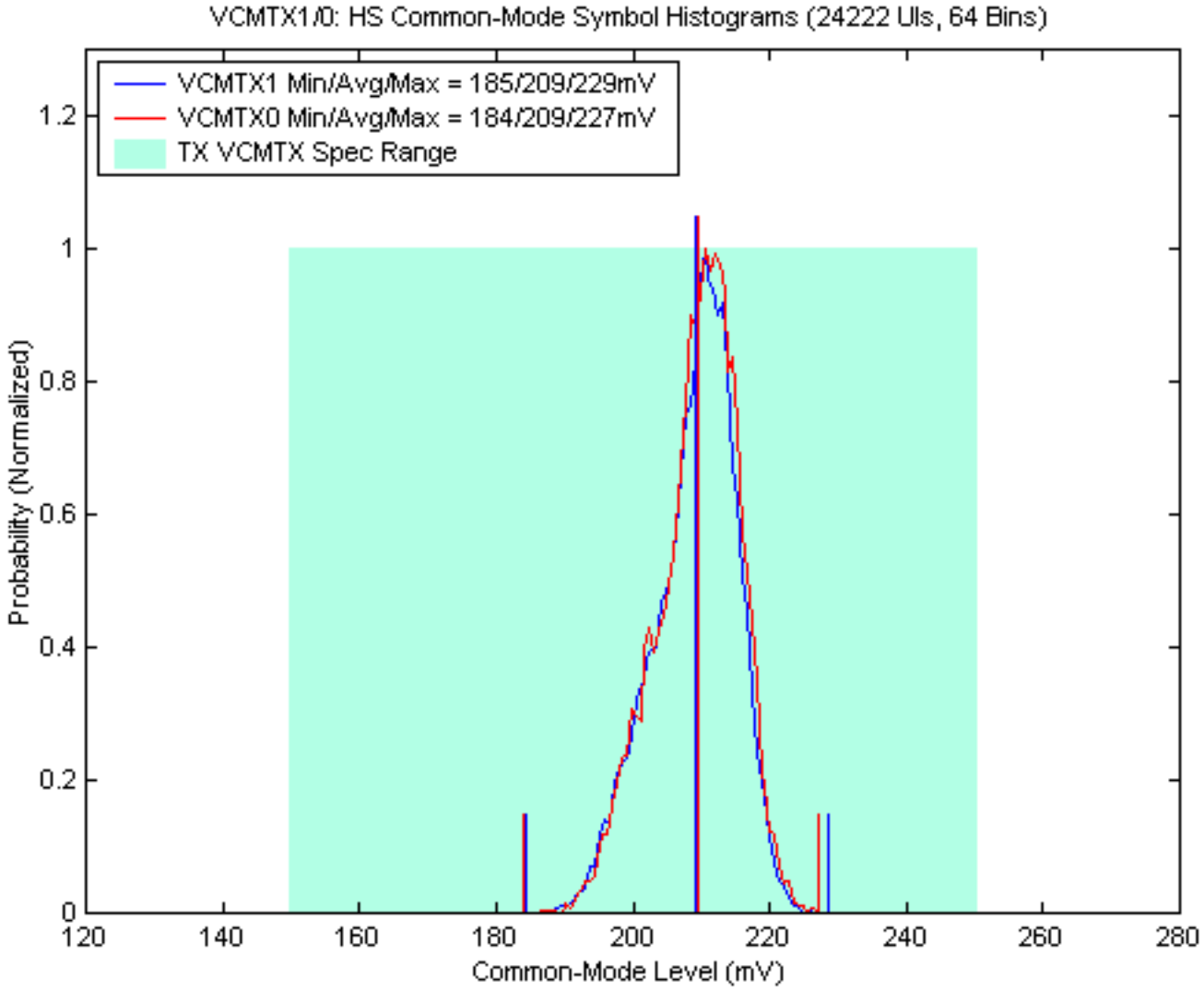

Figure 62: HF/LF Filtered HS-TX Common-Mode Waveforms (Clock Lane, ZID=100)

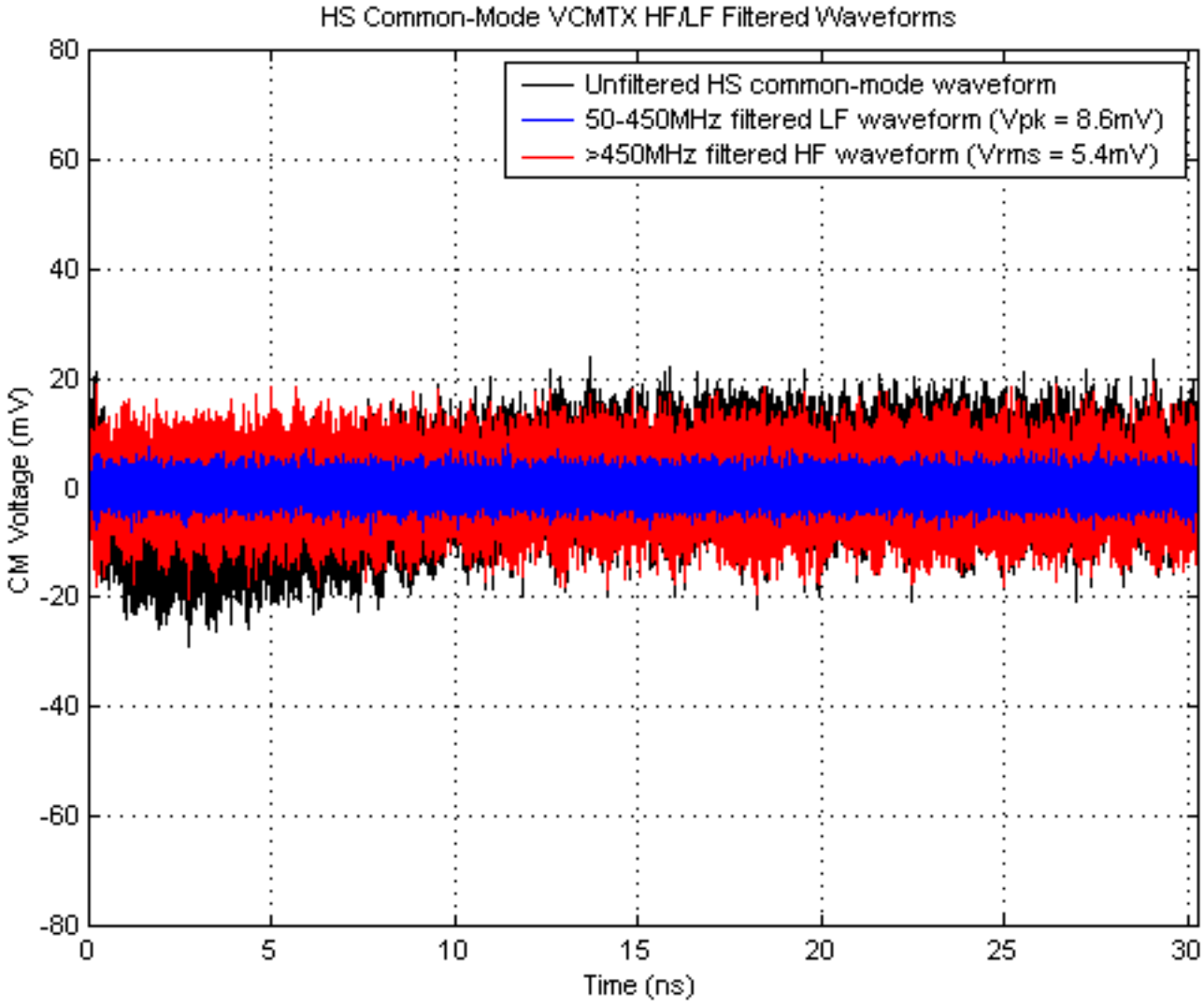

Figure 63: HS-TX 20%-80% Rise Time (Clock Lane, ZID=100)

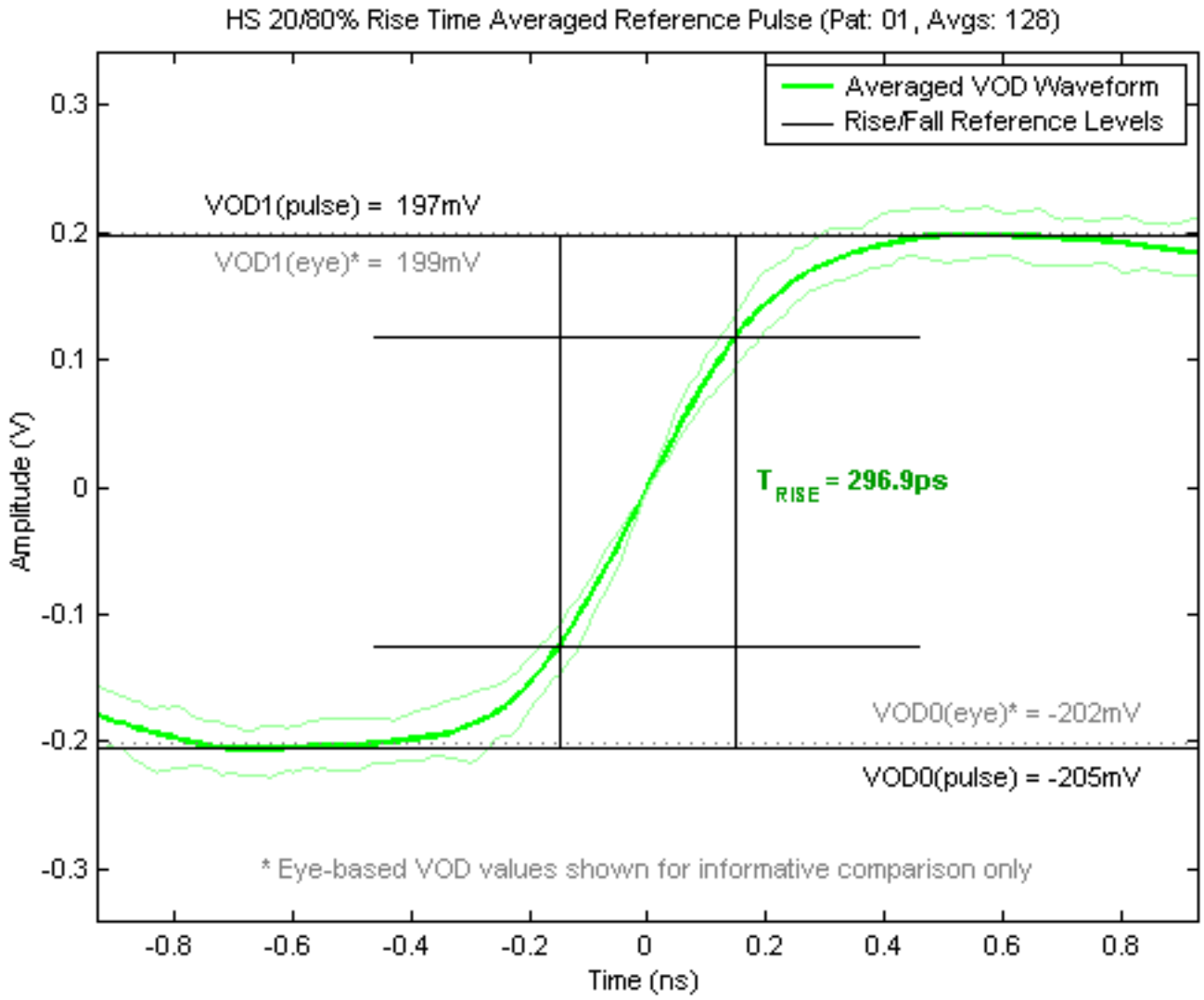

Figure 64: HS-TX 20%-80% Rise Time (Clock Lane, ZID=125)

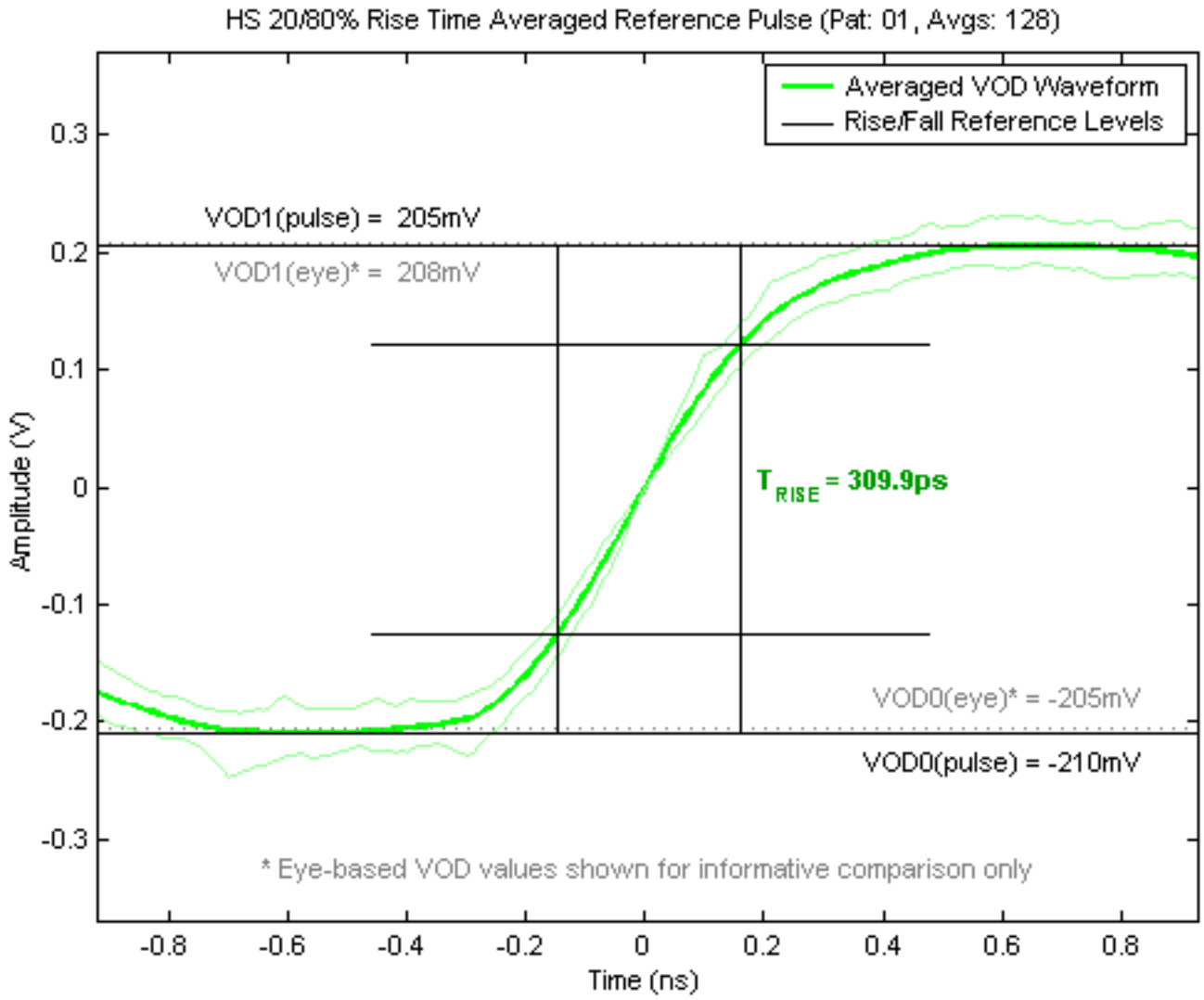

Figure 65: HS-TX 20%-80% Rise Time (Clock Lane, ZID=80)

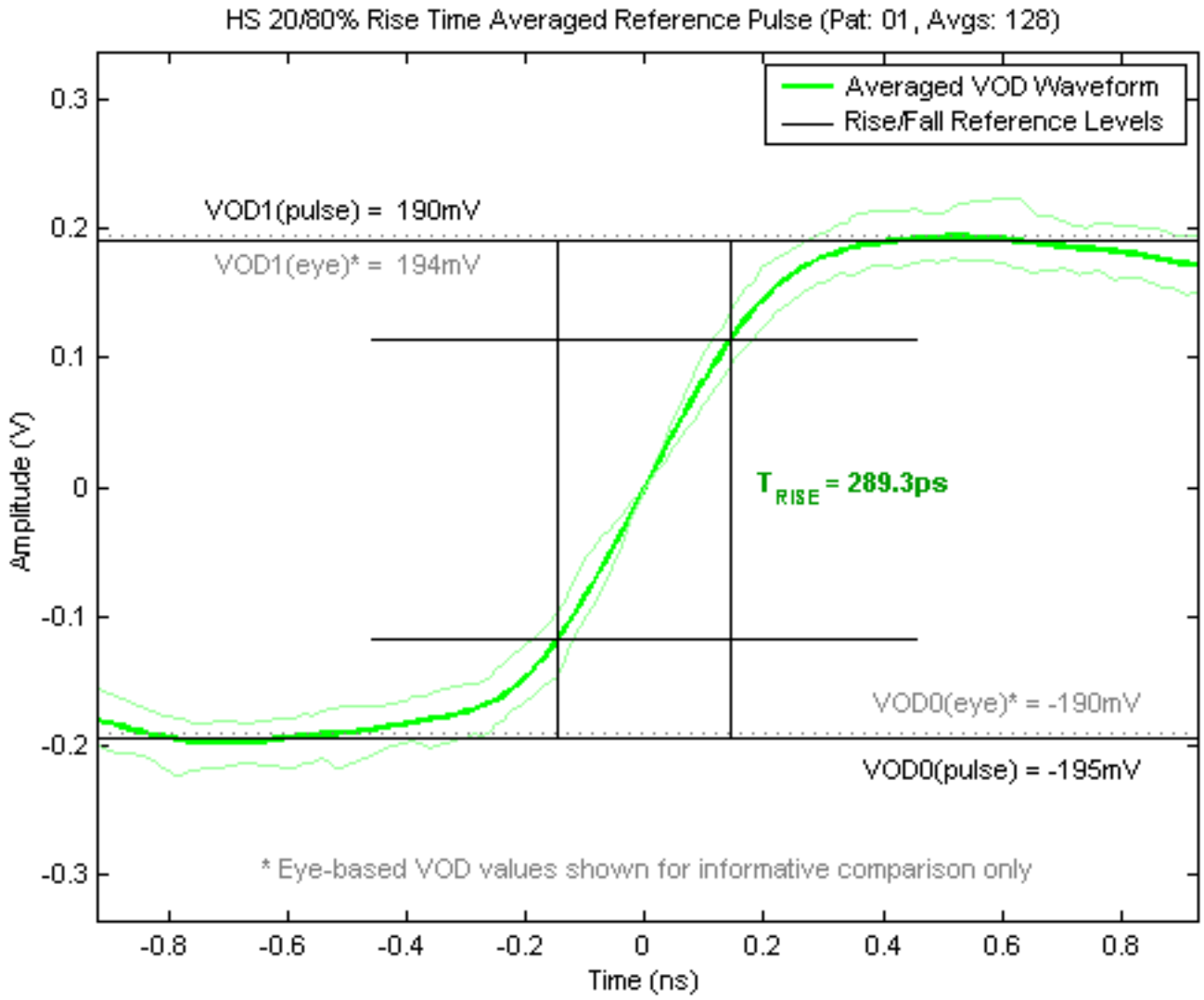

Figure 66: HS-TX 20%-80% Fall Time (Clock Lane, ZID=100)

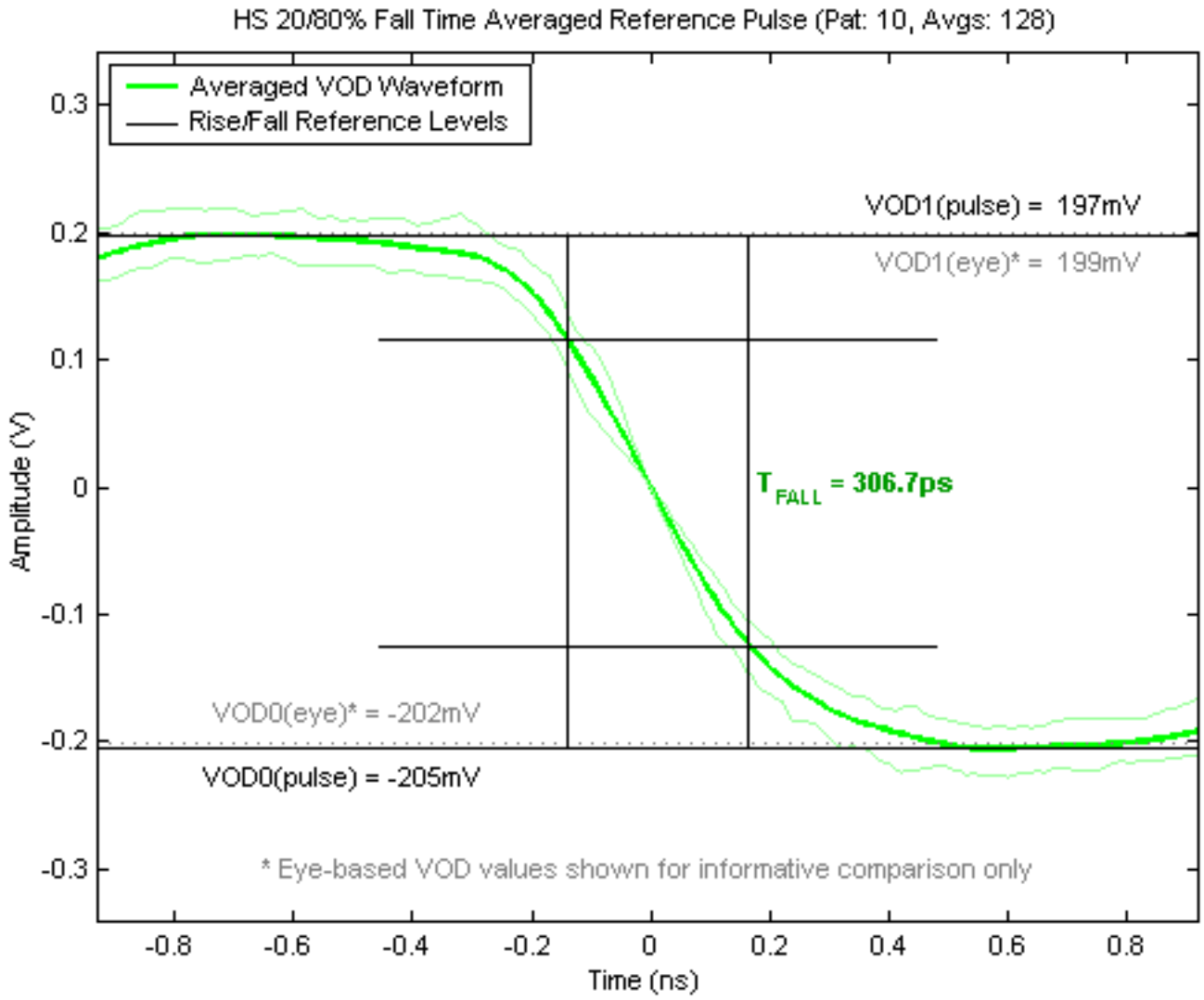

Figure 67: HS-TX 20%-80% Fall Time (Clock Lane, ZID=125)

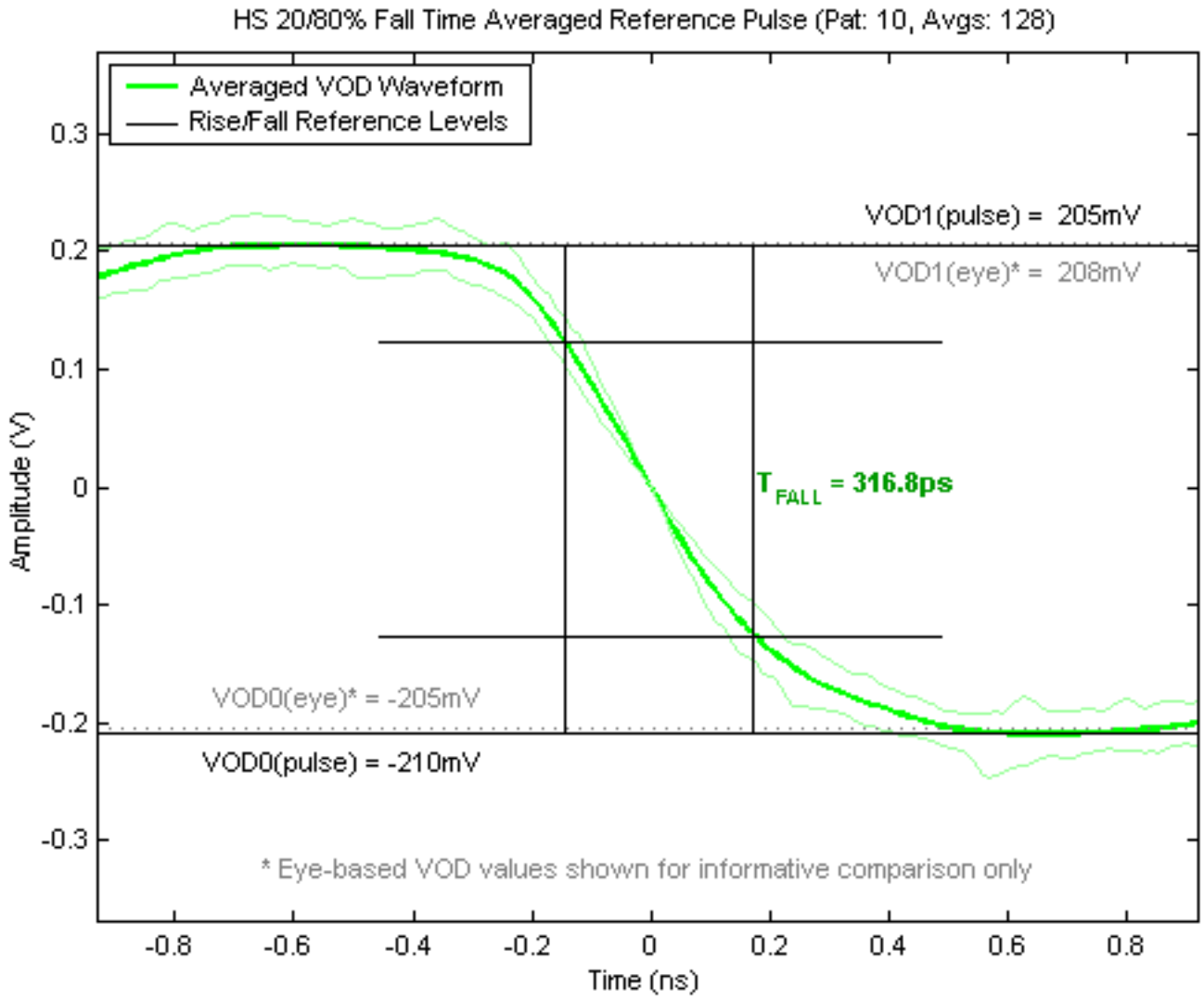

Figure 68: HS-TX 20%-80% Fall Time (Clock Lane, ZID=80)

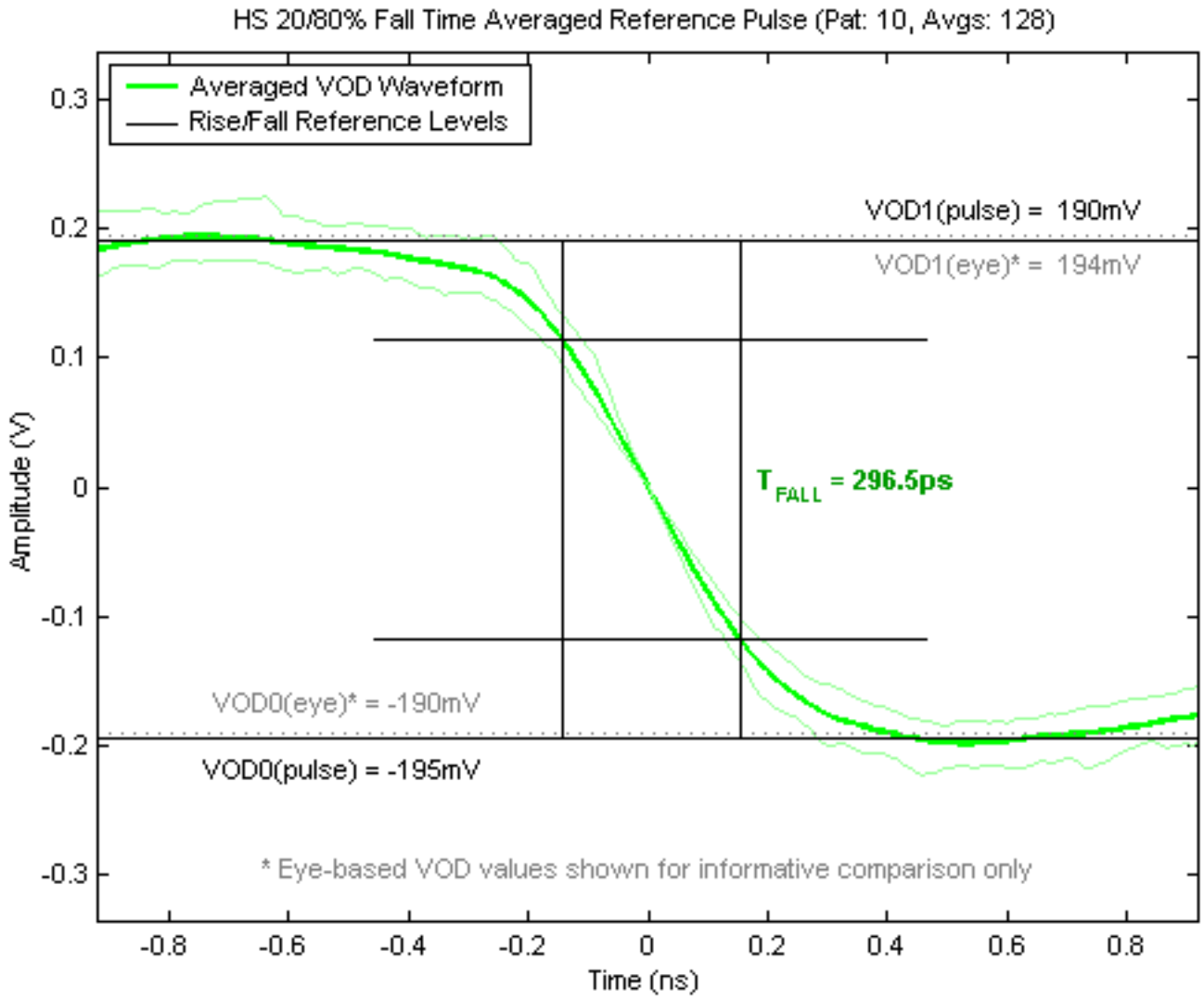

Figure 69: TCLK-TRAIL, TREOT, TEOT Intervals (Clock Lane, ZID=100)

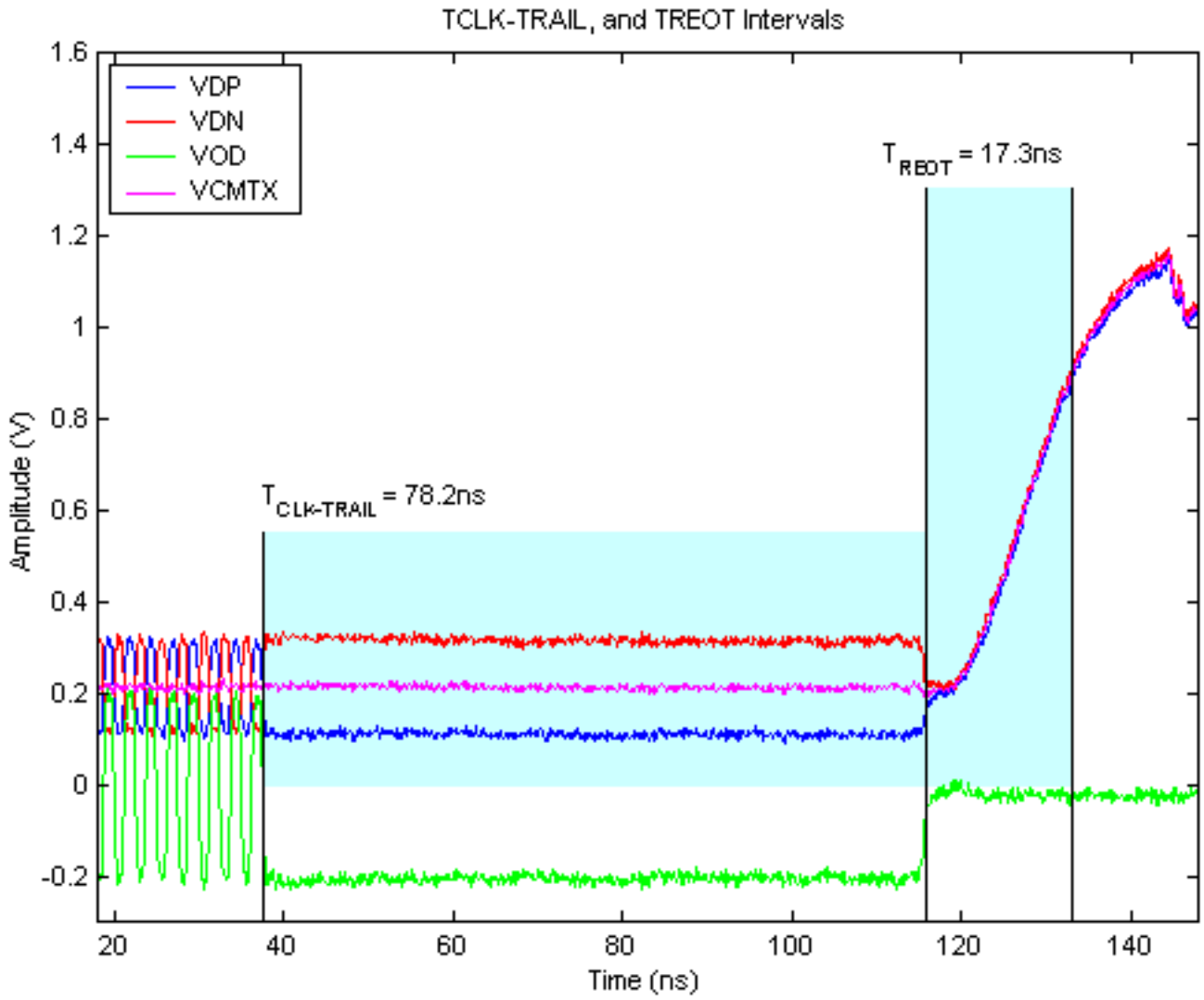

Figure 70: HS Eye Diagram (Clock Lane, ZID=100) (INFORMATIVE)

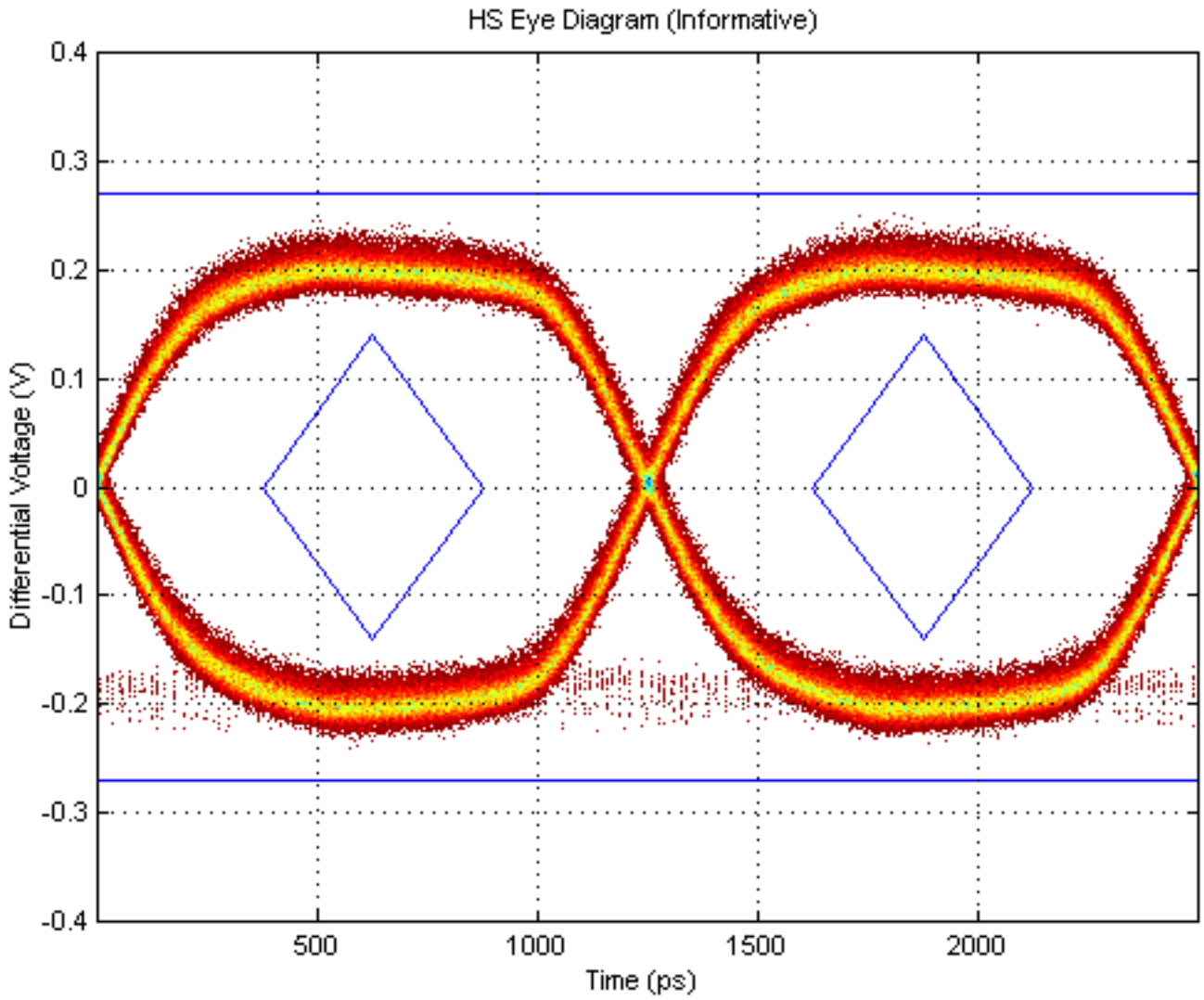

Figure 71: HS Eye Diagram (Clock Lane, ZID=125) (INFORMATIVE)

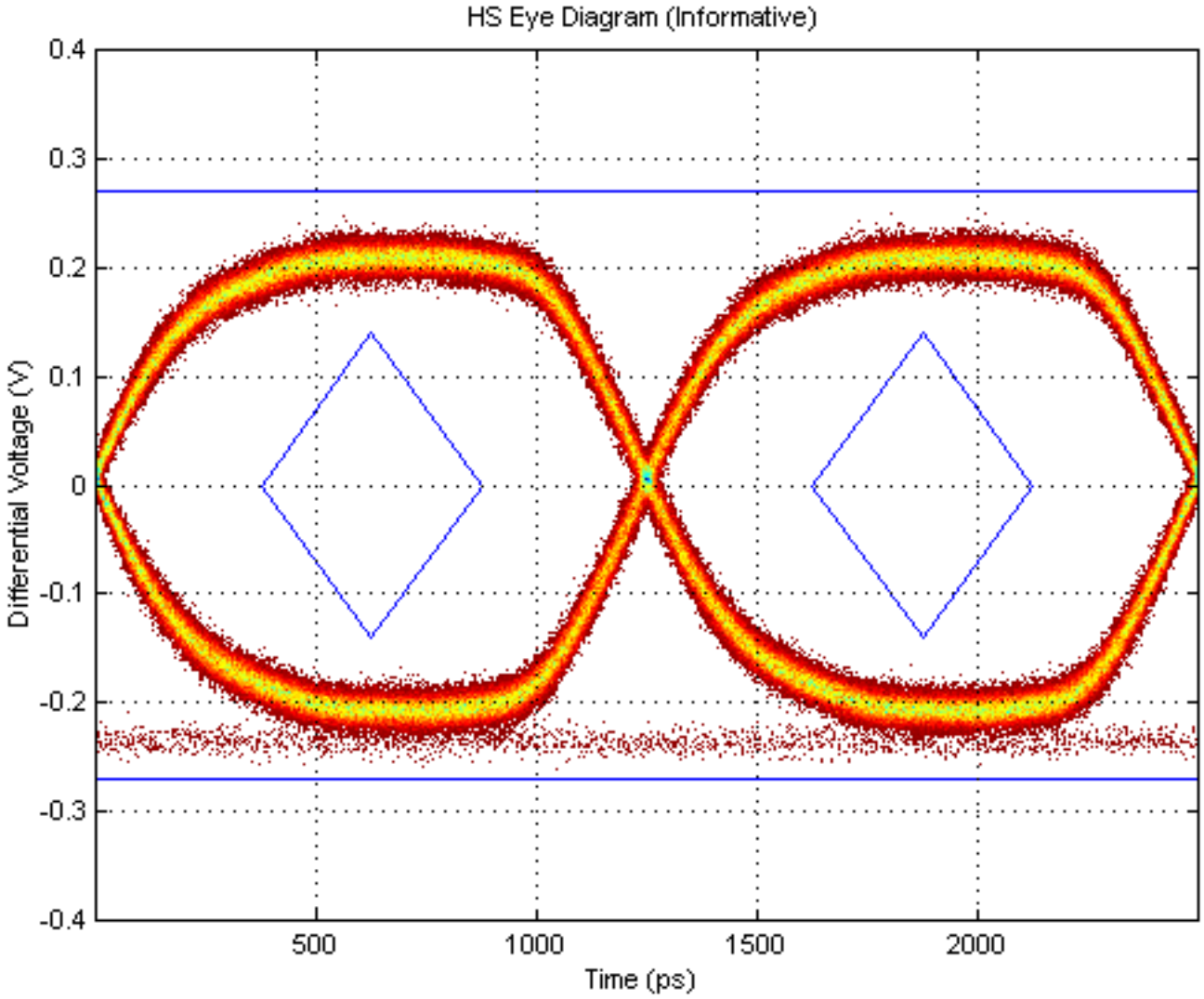

Figure 72: HS Eye Diagram (Clock Lane, ZID=80) (INFORMATIVE)

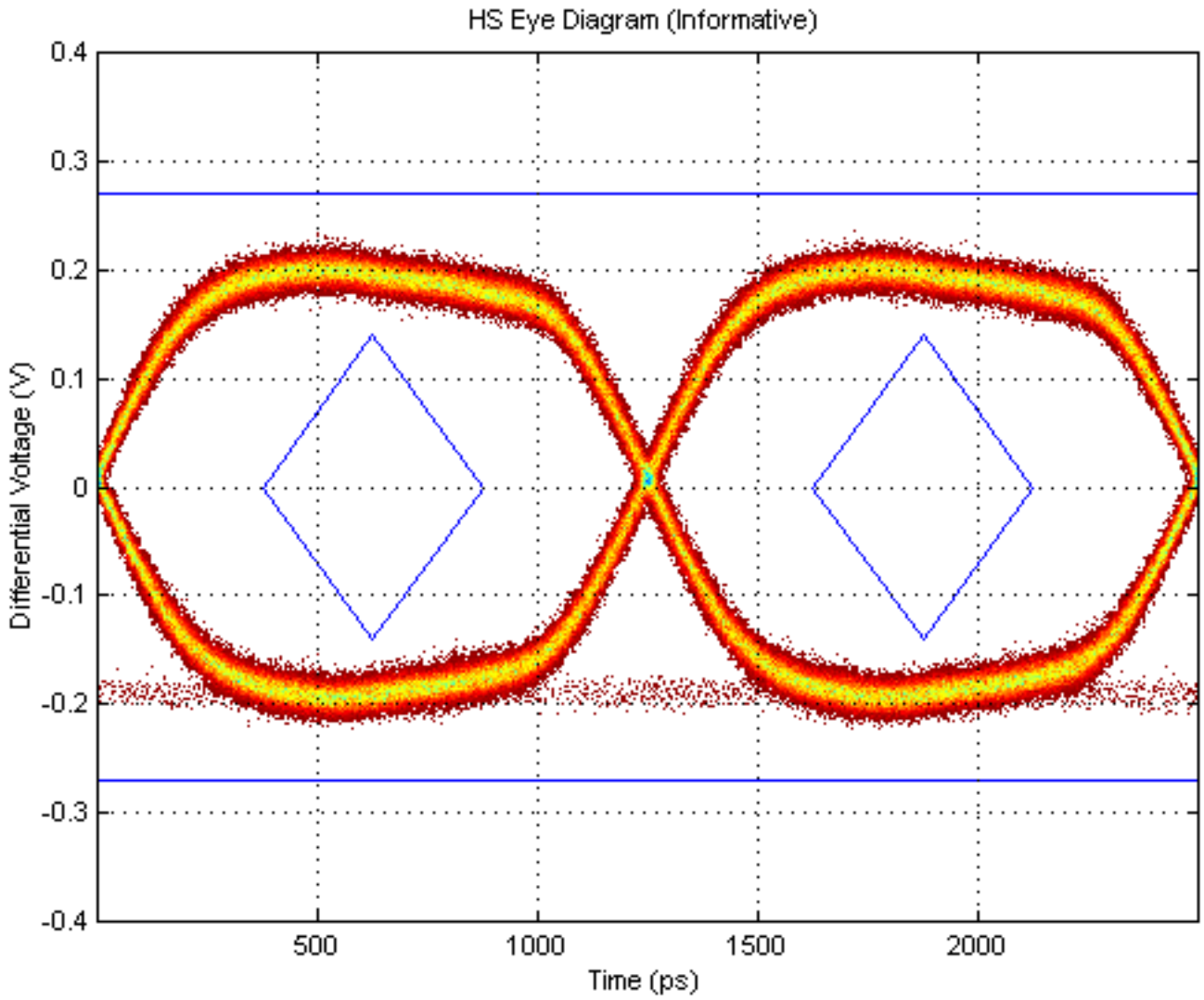

Figure 73: HS Clock Rising Edge Alignment to First Payload Bit (Data Lane 0, ZID=100)

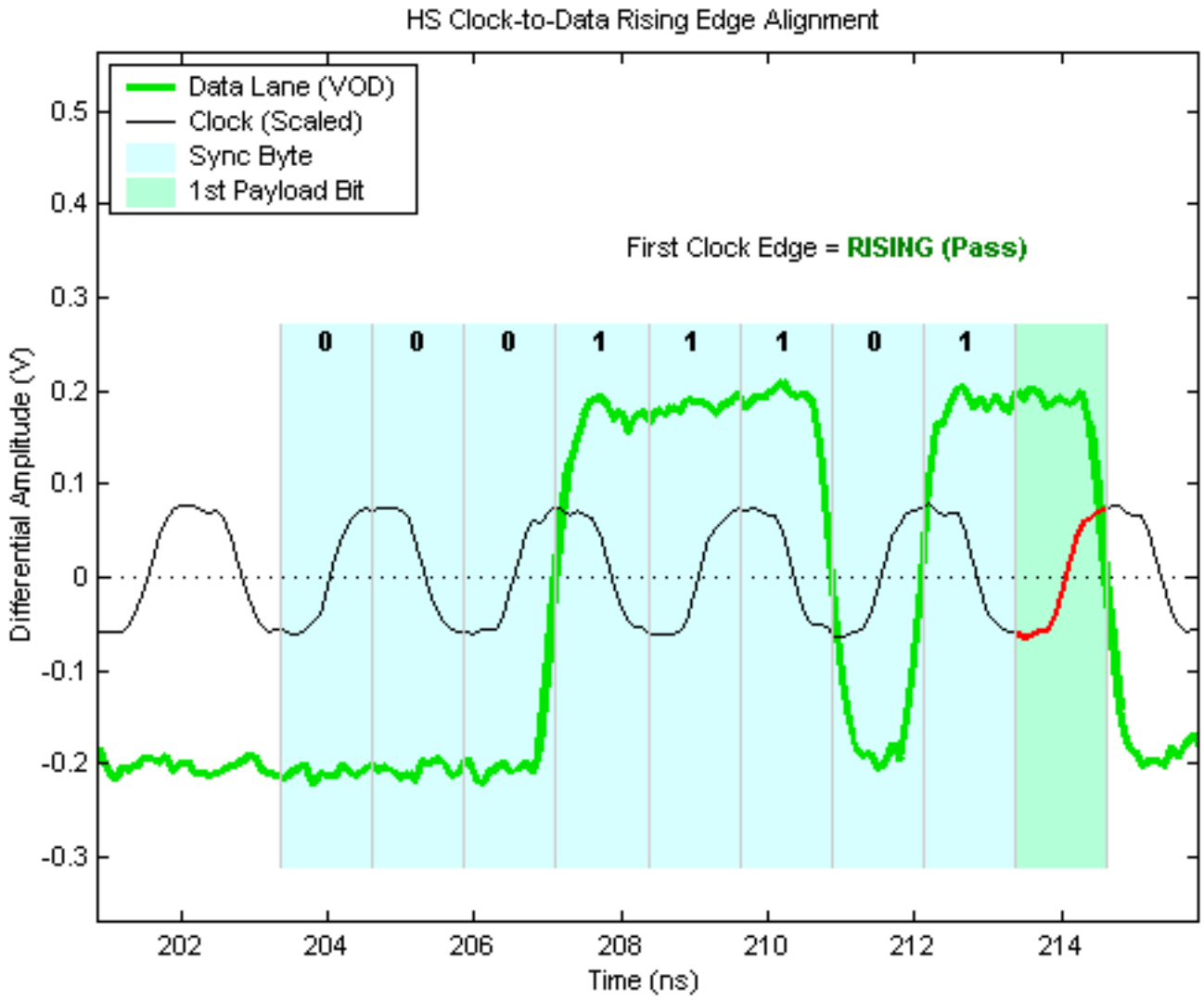

Figure 74: Data-to-Clock Skew (TSKEW(TX)) (Data Lane 0/Clock Lane, ZID=100)

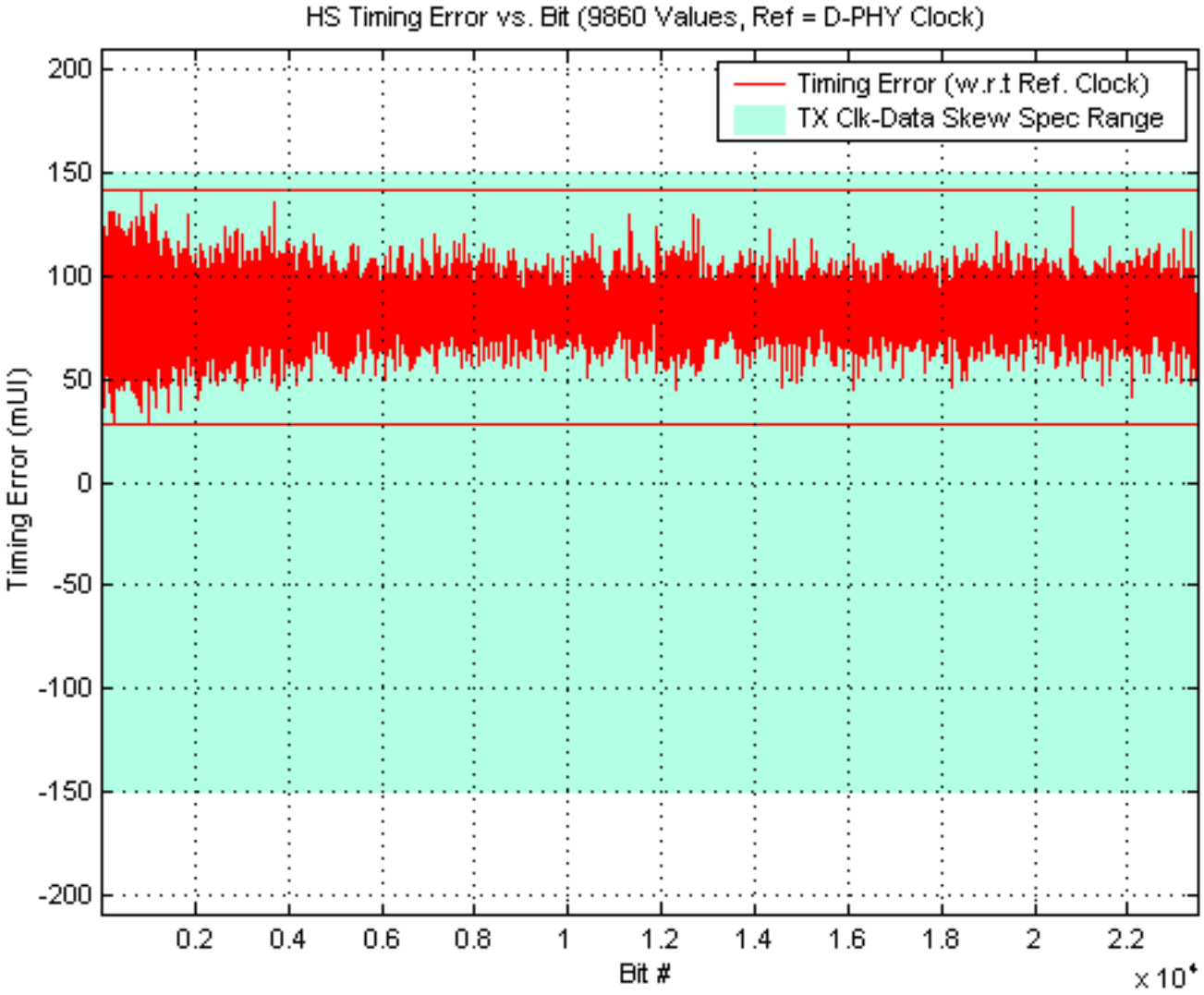

Figure 75: Data-to-Clock Skew Histogram (Data Lane 0/Clock Lane, ZID=100)