UNH-IOL MIPI Alliance Test Program
D-PHY RX Conformance Test Report

InterOperability Lab — 121 Technology Drive, Suite 2 — Durham, NH 03824 — (603) 862-3749

September 27, 2010

Engineer Name
Sample Company, Inc.
1010 Mobile Way
San Jose, CA 95101

Mr. Engineer:

Enclosed are the test results from the D-PHY RX Physical Layer Conformance testing performed on the:

Sample Company Model 4545 LCD Panel 1-Lane DSI Receiver

The testing was performed according to v0.98 of the MIPI Alliance D-PHY Conformance Test Suite, which is available to MIPI Alliance Members at:

https://members.mipi.org/mipi-testing/workspace/StartPage

Any issues observed during testing are listed below:

- **NO CONFORMANCE ISSUES WERE OBSERVED DURING TESTING**

Please feel free to contact me via email at aab@iol.unh.edu with any questions you may have regarding this report.

Sincerely,

Digitally signed by UNH-IOL
Date: 2010.09.23 00:26:53 -04'00'

Andy Baldman

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Table 1-0: Test Setup and DUT Configuration Information

DUT Details	
Week testing was performed	20100927
Manufacturer	Sample Company
Model	Model 4545 LCD Panel (1-Lane DSI Receiver)
Max. Supported HS Bit Rate	800 Mbps
Mfr. Serial Number	9876543210
Firmware Version	v1.0
Hardware Version	v0.10
Software Version	3.15
UNH-IOL ID Number	99999
Test System Hardware	
Real-time DSO	Agilent Infiniium DSA91304A, 13GHz, 40GS/s Real-time DSO
Signal Generator	Agilent ParBERT
Additional Comments/Notes	
All tests were performed using standard procedures as described in the test suite, on the DUT's Clock and Data0 Lanes.	

Table 2-1: (Section 2, Group 1): LP-RX Voltage and Timing Requirements

Test/Parameter	Conformance Range	Measured (Clock/Data 0)	Units
Test 2.1.1: LP-RX Logic 1 Input Voltage (V_{IH})			
Minimum voltage level where LP receiver consistently detects Logic 1	< 880	**624 / 653**	mV
Test 2.1.2: LP-RX Logic 0 Input Voltage, Non-ULP State (V_{IL})			
Maximum voltage level where non-ULP LP receiver consistently detects Logic 0	> 550	**625 / 638**	mV
Test 2.1.3: LP-RX Logic 0 Input Voltage, ULP State ($V_{IL-ULPS}$)			
Maximum voltage level where ULP-mode LP receiver consistently detects Logic 0	> 300	**325 / 338**	mV
Test 2.1.4: LP-RX Input Hysteresis (V_{HYST})			
Maximum Logic 1 hysteresis	> 25	**41 / 44**	mV
Test 2.1.5: LP-RX Minimum Pulse Width Response (T_{MIN-RX})			
Minimum detected LP pulse width	< 20	**11 / 12**	ns
Test 2.1.6: LP-RX Input Pulse Rejection (e_{SPIKE})			
Maximum tolerated $-e_{SPIKE}$ while in Logic 1 state	> 300	**332 / 345**	mV*ps
Maximum tolerated $+e_{SPIKE}$ while in Logic 0 state	> 300	**323 / 328**	mV*ps
Test 2.1.7: LP-RX Interference Tolerance (V_{INT} and f_{INT})			
Device tolerates all interference test cases	Pass/Fail	**PASS / PASS**	-
Test 2.1.8: LP-CD Logic Contention Thresholds (V_{IHCD} and V_{ILCD})			
Measured V_{IHCD} voltage	> 450	**554 / 553**	mV
Measured V_{ILCD} voltage	< 200	**179 / 188**	mV

Table 2-2: (Section 2, Group 2): LP-RX Behavioral Requirements

Test/Parameter	Conformance Range	Measured	Units
Test 2.2.1: LP-RX Initialization period (T_{INIT})			
Minimum T_{INIT} that causes the DUT to successfully receive data	> 1	**1.043**	ms
Test 2.2.2: ULPS Exit: LP-RX T_{WAKEUP} Timer Value			
Verify that the DUT can successfully receive image data following a 1ms T_{WAKEUP} interval	Pass/Fail	**PASS**	-
Test 2.2.3: Clock Lane LP-RX Invalid/Aborted ULPS Entry			
Verify that DUT operation is not affected by invalid Clock Lane ULPS Entry sequence #1 (LP-11/10/11)	Pass/Fail	**PASS**	-
Verify that DUT operation is not affected by invalid Clock Lane ULPS Entry sequence #2 (LP-11/10/01/11)	Pass/Fail	**PASS**	-
Test 2.2.4: Data Lane LP-RX Invalid/Aborted Escape Mode Entry			
Verify that DUT operation is not affected by invalid Escape Mode Entry sequence #1 (LP-11/10/00/01/11)	Pass/Fail	**PASS**	-
Verify that DUT operation is not affected by invalid Escape Mode Entry sequence #2 (LP-11/10/00/11/11)	Pass/Fail	**PASS**	-
Verify that DUT operation is not affected by invalid Escape Mode Entry sequence #3 (LP-11/10/11/11/11)	Pass/Fail	**PASS**	-
Test 2.2.5: Data Lane LP-RX Invalid/Aborted Escape Mode Command			
DUT successfully ignores Test Case #1	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #2	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #3	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #4	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #5	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #6	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #7	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #8	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #9	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #10	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #11	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #12	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #13	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #14	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #15	Pass/Fail	**PASS**	-
Test 2.2.6: Data Lane LP-RX Escape Mode Invalid Exit (INFORMATIVE)			
Observe DUT behavior for Test Case #1 (Mark-0/Stop)	(Informative)	**PASS**	-
Observe DUT behavior for Test Case #2 (Space/Stop)	(Informative)	**PASS**	-
Observe DUT behavior for Test Case #3 (Stop/Stop)	(Informative)	**PASS**	-
Test 2.2.7: Data Lane LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits			
DUT successfully ignores Test Case #1 (Reset-Trigger+ULPS)	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #2 (Unknown-3+ULPS)	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #3 (Unknown-4+ULPS)	Pass/Fail	**PASS**	-
DUT successfully ignores Test Case #4 (Unknown-5+ULPS)	Pass/Fail	**PASS**	-
Test 2.2.8: Data Lane LP-RX Escape Mode Unsupported/Unassigned Commands			
DUT successfully ignores all Test Cases (248 Unassigned codes, and also Undefined-1, Undefined-2, Unknown-3, Unknown-4, Unknown-5)	Pass/Fail	**PASS**	-

Table 2-3: (Section 2, Group 3): HS-RX Voltage and Timing Requirements

Test/Parameter	Conformance Range	Measured (Clk/Data0)	Units
Test 2.3.1: HS-RX Common Mode Voltage Tolerance ($V_{CMRX(DC)}$)			
DUT successfully receives Test Case #1 (70/360)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #2 (70/440)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #3 (70/140)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #4 (330/440)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #5 (330/520)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #6 (330/140)	Pass/Fail	**PASS/PASS**	-
Test 2.3.2: HS-RX Differential Input High Threshold (V_{IDTH})			
Minimum V_{IDTH} where the DUT does not indicate errors	< 70	**26 / 28**	mV
Test 2.3.3: HS-RX Differential Input Low Threshold (V_{IDTL})			
Maximum V_{IDTL} where the DUT does not indicate errors	> -70	**-27 / -31**	mV
Test 2.3.4: HS-RX Single-Ended Input High Voltage (V_{IHHS})			
DUT successfully receives Test Case #1 (325/540)	Pass/Fail	**PASS/PASS**	-
Test 2.3.5: HS-RX Single-Ended Input Low Voltage (V_{ILHS})			
DUT successfully receives Test Case #1 (95/540)	Pass/Fail	**PASS/PASS**	-
Test 2.3.6: HS-RX Common-Mode Interference 50MHz - 450MHz ($\Delta V_{CMRX(LF)}$)			
DUT successfully receives Test Case #1 (200/400)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #2 (200/140)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #3 (70/140)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #4 (330/140)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #5 (330/520)	Pass/Fail	**PASS/PASS**	-
Test 2.3.7: HS-RX Common-Mode Interference Beyond 450MHz ($\Delta V_{CMRX(HF)}$)			
DUT successfully receives Test Case #1 (200/400)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #2 (200/140)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #3 (70/140)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #4 (330/140)	Pass/Fail	**PASS/PASS**	-
DUT successfully receives Test Case #5 (330/520)	Pass/Fail	**PASS/PASS**	-
Test 2.3.8: HS-RX Setup/Hold and Jitter Tolerance			
(Minimum V_{OD}): DUT successfully receives minimum T_{HOLD}	Pass/Fail	**PASS**	-
(Minimum V_{OD}): DUT successfully receives minimum T_{SETUP}	Pass/Fail	**PASS**	-
(Nominal V_{OD}): DUT successfully receives minimum T_{HOLD}	Pass/Fail	**PASS**	-
(Nominal V_{OD}): DUT successfully receives minimum T_{SETUP}	Pass/Fail	**PASS**	-

Table 2-4: (Section 2, Group 4): HS-RX Timer Requirements

Test/Parameter	Conformance Range		Measured	Units
	Formula	Numeric		
Test 2.4.1: Data Lane HS-RX $T_{D\text{-}TERM\text{-}EN}$ Value				
(Data Lane 0): Minimum $T_{D\text{-}TERM\text{-}EN}$	< 35+4*UI	< 39	**18.0**	ns
(Data Lane 1): Minimum $T_{D\text{-}TERM\text{-}EN}$	< 35+4*UI	< 39	N/A	ns
(Data Lane 2): Minimum $T_{D\text{-}TERM\text{-}EN}$	< 35+4*UI	< 39	N/A	ns
(Data Lane 3): Minimum $T_{D\text{-}TERM\text{-}EN}$	< 35+4*UI	< 39	N/A	ns
Test 2.4.2: Data Lane HS-RX $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ Tolerance				
DUT successfully receives Test Case #1	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #2	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #3	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #4	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #5	-	Pass/Fail	**PASS**	-
Test 2.4.3: Data Lane HS-RX $T_{HS\text{-}SETTLE}$ Value				
Measured $T_{HS\text{-}SETTLE}$	> 85+6*UI	> 91	**109**	ns
Test 2.4.4: Data Lane HS-RX $T_{HS\text{-}TRAIL}$ Tolerance				
DUT successfully receives Test Case #1 (80ns+4*UI)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #2 (40ns+4*UI)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #3 (70ns+12*UI)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #4 (105ns+12*UI)	-	(Informative)	**PASS**	-
Test 2.4.5: Data Lane HS-RX $T_{HS\text{-}SKIP}$ Value				
Measured $T_{HS\text{-}SKIP}$	40 / 55+4*UI	40 / 59	**48.4**	ns
Test 2.4.6: Clock Lane HS-RX $T_{CLK\text{-}TERM\text{-}EN}$ Value				
Measured $T_{CLK\text{-}TERM\text{-}EN}$	-	< 38	**18.2**	ns
Test 2.4.7: Clock Lane HS-RX $T_{CLK\text{-}PREPARE}$ + $T_{CLK\text{-}ZERO}$ Tolerance				
DUT successfully receives Test Case #1 (70/300)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #2 (38/332)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #3 (38/262)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #4 (95/275)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #5 (95/205)	-	Pass/Fail	**PASS**	-
Test 2.4.8: Clock Lane HS-RX $T_{CLK\text{-}SETTLE}$ Value				
Measured $T_{CLK\text{-}SETTLE}$	-	> 95	**104**	ns
Test 2.4.9: Clock Lane HS-RX $T_{CLK\text{-}TRAIL}$ Tolerance				
DUT successfully receives Test Case #1 (80ns)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #2 (40ns)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #3 (70ns+12*UI)	-	Pass/Fail	**PASS**	-
DUT successfully receives Test Case #4 (105ns+12*UI)	-	(Informative)	**PASS**	-
Test 2.4.10: Clock Lane HS-RX $T_{CLK\text{-}MISS}$ Value				
Measured $T_{CLK\text{-}MISS}$	-	< 60	**28.9**	ns
Test 2.4.11: Clock Lane HS-RX $T_{CLK\text{-}PRE}$ and $T_{CLK\text{-}POST}$ Tolerance				
DUT successfully receives Test Case #1 (Minimum $T_{CLK\text{-}PRE/POST}$)	-	Pass/Fail	**PASS**	-