# Fast Ethernet Consortium
## Clause 25 PMD Conformance Test Suite v3.21 Report

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Report Rev. 1.0

Enclosed are the results from the Clause 25 PMD Conformance testing performed on:

| | |
|---|---|
| Device Under Test (DUT): | Semiconductor Corporation ABC evaluation board |
| Hardware Version: | V1.2 |
| Firmware Version: | Not Available |
| Software Version: | Not Available |
| Miscellaneous: | Port 1 tested. |

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL25_PMD/PMD_Test_Suite_v3.21.pdf

| Issues Observed While Testing |
|---|
| **25.1.1 – Differential Output Voltage:** The positive differential output voltage was observed to be 1054 mV. |
| **25.1.4 – Transmitter Jitter:** The peak-to-peak total jitter was observed to be 1.64 ns. |
| **25.1.8 – Transmitter Clock Frequency:** The transmitter clock frequency was observed to be 7.6 KHz greater than 125 Mhz. |
| **25.2.3 – Baseline Wander Correction:** The DUT was observed to drop more than 7 packets out of 20,000 for bidirectional baseline wander packets over 75 m and 100 m simulated cable length with 3 and 5 ns rise time. |

For specific details regarding issues please see the corresponding test result.

Testing Completed: 02/10/2005

Review Completed: 02/10/2005

Digitally signed by UNH-IOL
Date: 2005.01.31 10:16:34 - 05'00'

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## Table 1: Hardware Information

| **1000BASE-T PHY** | |
|---|---|
| Manufacturer | Seminconductor Corporation |
| Model | ABC |
| Version | 1.2 |
| | |
| **Magnetics** | |
| Manufacturer | Transformer |
| Model | AM423 |
| Version | Not Available |
| | |
| **Test System Hardware** | |
| Real-time DSO | TEKTRONIX,TDS7104,B041940,CF:91.1CT FV:2.2.0 |
| Vector Network Analyzer | HEWLETT-PACKARD,4395A,MY41100156,REV1.05 |
| Arbitrary Waveform Genearator | SONY/TEK,AWG2041,0,CF:91.1CT FV:1.26 |

## Test Setup

All tests in this report were performed using the test setup specified in the 100BASE-TX PMD Test Suite in the Test Setup section of each test.

## Report Key

Table 1 contains setup and configuration information for the Device Under Test (DUT), as well as the test system hardware. A best effort is made to record as much information as possible about the DUT, including hardware, software, and firmware versions, in addition to specific information regarding PHY IC and magnetics packages. The test system hardware information fields display the GPIB device identification strings for each piece of system hardware. These identifiers generally include the manufacturer, model number, serial number, and firmware revision information for the particular piece of equipment, however the amount of detail can vary depending on the instrument.

Table 2 summarizes the electrical conformance requirements and results, listed by IOL test number. A brief description is given for each parameter, along with the range of conformant values and the values measured during testing. There is also a convenient link to the figure that is relevant to the specific test. (Complete test descriptions can be found in the 100BASE-TX TP-PMD test suite.)

Table 3 summarizes the packet-based receiver testing conformance requirements and results, listed by IOL test number.

The remainder of the report contains graphical supplements to the tabulated results. Most of these supplements are informative, and are included to provide insight into the measurement methodologies used to generate the numerical results. A brief explanation of each figure is provided here:

Figure 1 contains the MLT-3 eye pattern for the DUT. It is a persistence waveform generated in MATLAB from the actual waveform data acquired during the jitter test. It is shown along with the eye mask specified in ANSI-X3.263. It should be noted that the eye mask is considered informative by ANSI-X3.263, and no part of the eye pattern or mask is used for generating numerical results. It is intended to serve as a 'feel good' measure to show overall signal shape.

Figure 2 contains statistical information pertaining to jitter. During the jitter measurement, sufficient timing information is gathered such that the timing error on each edge of the reference pattern waveform is observed for a minimum of 1000 observations. The max, min, mean, and sigma values are tracked for each edge of the reference pattern. Figure 2 shows the final values of the mean timing error per edge of the reference pattern. The peak-to-peak value of this distribution is taken to be the Deterministic Jitter (DJ) component, and is ultimately combined with the Random Jitter (RJ) component (discussed below) to determine the peak-to-peak Total Jitter (TJ). The numerical value of the peak-to-peak DJ is displayed in the plot legend.

Figure 3 is similar to Figure 2, however this figure shows the final sigma values for the jitter on each edge of the reference pattern. This information relates to the amount of Random Jitter (RJ) present in the signal. If RJ is modeled as a purely Gaussian phenomenon, and DJ is modeled as a pair of delta functions (as is the case in the simplest jitter models, such as the one presented in Appendix 25.B of the Test Suite), all edges, in theory, would be equally impacted by the effects of RJ, resulting in the same sigma value being observed for every edge. Because real-world jitter does not perfectly adhere to the dual-Dirac jitter model (particularly in the case of DJ, which can often be multi-modal), the sigma distribution generally tends to span some range (although the distribution shown in Figure 3 generally appears to be fairly uniform). Thus, the question arises as to which sigma value to use when computing the Total Jitter computation. Since true RJ should affect all edges equally, the smallest sigma value is chosen, as its value is effectively contained in every edge of the pattern. Figure 3 shows a vertical red line at the location of the minimum sigma value, and also displays the sigma value itself in the plot legend. The peak-to-peak Total Jitter reported in the table of results is then computed as the sum of the peak-to-peak DJ from Figure 2, plus 10 times the sigma value shown in Figure 3. The 10x multiplier corresponds to +/- 5 standard deviations, which corresponds to a BER of approximately 1E-7.

Figure 4 (informative) shows another statistical view of jitter through a combined DJ/TJ histogram. In addition to accumulating the max, min, mean, and sigma values, and additional array is accumulated during the jitter test, which contains all of the timing error values for all observed edges. The histogram of this array produces the

Total Jitter histogram shown in blue in Figure 4. Histogramming the DJ values of Figure 2 with the same bin values as the TJ histogram generates the DJ histogram, shown as a red stem plot in Figure 4. In theory, the convolution of the DJ stem plot with a Gaussian having sigma equal to the value obtained from Figure 3 should produce the blue Total Jitter histogram of Figure 4. The DJ histogram is represented as a stem plot purely for visualization purposes, and helps in visually 'extracting' the DJ distribution from the blue Total Jitter histogram.

Figure 5 (informative) shows yet another view of jitter, namely in the frequency domain. For a single 8188-UI-long block of waveform data, one can construct a 'jitter waveform' by plotting the timing error on each edge versus the UI offset for that edge. The magnitude of the FFT of this waveform produces the power spectrum shown in Figure 5. In theory, the 'noise floor' of this spectrum corresponds to RJ, while prominent spikes are attributable to DJ. Because the spectrum shown in Figure 5 is generated using only a single block of data (i.e., no averaging applied), the spectrum is only a rough estimate, however it is usually sufficient to reveal large DJ spikes which are often prevalent at the harmonics of the base oscillator frequency of the transmitter IC.

Figures 6 and 7 (both informative) show sample captures of the Differential Output Voltage (DOV) reference waveform sourced by the DUT. They are one of the 128 observations made for both the positive and negative DOV waveforms that are used to calculate the Vout, Overshoot, and DOV values. On each plot, the horizontal red and pink lines indicate the Vout and overshoot values respectively, as measured for that particular waveform trace.

Figure 8 and 9 (both informative) show the positive and negative Rise/Fall Time (RFT) reference waveforms, indicating the 10% and 90% voltage levels (relative to the Vout values of the DOV waveforms), as well as the crossing times for these voltages. These plots often show the impact an overdamped response can have on rise/fall times. Again, they are one of 128 observations, whose measured values are averaged to produce the final RFT results.

Figure 10 (informative) shows the Duty Cycle Distortion (DCD) reference waveform, along with the 50% levels and crossing times used to compute the DCD error values (see test suite for details). Note: Unlike the DOV and RFT waveforms, the DCD measurement does not involve an inverse-polarity waveform.

Figures 11 and 13 (both normative) show the TX and RX return loss curves for the DUT. Each plot shows the return loss response based on 85 and 115 ohm source impedances, both of which must fall completely above the limit line in order to be deemed conformant. The minimum distance between either of these curves and the limit line is reported as the Return Loss Margin, and must be at least 0dB or greater.

Figures 12 and 14 (both informative) show the output and input impedances of the transmitter and receiver ports respectively, in ohms. These plots are ultimately derived from the return loss measurement data, and provide an alternative perspective on the return loss characteristics (for those not accustomed to thinking in terms of dB's of return loss.) In general, the closer the impedance is to 100 ohms, the higher the return loss will be. Impedance values that are skewed to either side of 100 ohms will tend to show a higher return loss curve for that source impedance (85 or 115 ohms), at the expense of a poorer curve at the alternate source impedance. A perfectly matched 100-ohm port would have a desirable 'high loss', in that none of the incident signal would be reflected back to the source.

## Table 2: Summary of Electrical Requirements and Results

| Parameter | Min | Max | Measured | Units | Figure |
|---|---|---|---|---|---|
| **25.1.1 – Differential Output Voltage** | | | | | |
| Peak Positive Amplitude, $+V_{out}$ | 950 | 1050 | 1054 | mV | 6 |
| Peak Negative Amplitude, $-V_{out}$ | -1050 | -950 | -1048 | mV | 7 |
| Signal Amplitude Symmetry | 98 | 102 | 100.5 | % | |
| | | | | | |
| **25.1.2 – Rise and Fall Times** | | | | | |
| Signal Rise, Baseline to $+V_{out}$ | 3 | 5 | 3.75 | ns | 8 |
| Signal Fall, $+V_{out}$ to Baseline | 3 | 5 | 3.39 | ns | 8 |
| Signal Rise, Baseline to $-V_{out}$ | 3 | 5 | 3.72 | ns | 9 |
| Signal Fall, $-V_{out}$ to Baseline | 3 | 5 | 3.30 | ns | 9 |
| Rise and Fall Time Symmetry | 0 | 0.5 | 0.45 | ns | |
| | | | | | |
| **25.1.3 – Duty Cycle Distortion** | | | | | |
| Peak-to-Peak DCD | 0 | 0.5 | 0.11 | ns | 10 |
| | | | | | |
| **25.1.4 – Transmitter Jitter** | | | | | |
| Peak-to-Peak Total Jitter (DJ + 5 sigma) | 0 | 1.4 | (1.64) | ns | 1,2,3,4,5 |
| | | | | | |
| **25.1.5 – Waveform Overshoot** | | | | | |
| Excursion Beyond $+V_{out}$ | 0 | 5 | 0.0 | % | 6 |
| Excursion Beyond $-V_{out}$ | 0 | 5 | 0.0 | % | 7 |
| | | | | | |
| **25.1.6 – Transmitter Return Loss** | | | | | |
| The impedance of the transmitter shall be such that the return loss is greater than 16dB from 2 to 30MHz, greater than $(16-20\log_{10}(f/30MHz))$ from 30 to 60MHz, and greater than 10dB from 60 to 80MHz for all differential signals incident upon the transmitter from an 85 or 115 ohm source. The minimum difference between the limit line and the return loss curve will be indicated as the Return Loss Margin. | 0 | +Inf | 0.4 | dB | 11,12 |
| | | | | | |
| **25.1.7 – Transmitter Open Circuit Inductance** | | | | | |
| OCL with DC Bias Current = 8mA | 350 | +Inf | 576 | uH | |
| | | | | | |
| **25.1.8 – Transmitter Clock Frequency** | | | | | |
| Mean clock frequency minus 125MHz | -6.25 | 6.25 | 7.6 | kHz | |
| | | | | | |
| **25.1.9 – Differential Input Impedance** | | | | | |
| The return loss limits specified in Test 25.1.6 shall also be applicable to the receiver. | 0 | +Inf | 2.2 | dB | 13,14 |

## Table 3: Summary of Packet-based Receiver Testing Requirements and Results

**Test Parameter**

**25.2.2 – Adaptive Equalization**

**Requirements**: The receiver shall maintain a bit error rate better than $10^{-8}$ over test channels representing 5% to 100% (5% increments) of the worst-case cable attenuation. This implies that no more than 7 out of 500,000 64-byte packets may be received in error.

**Results:**

| Cable Length (m) | Loss at 16 MHz (dB) | Errors (tr = 3 ns) | Errors (tr = 5 ns) |
|---|---|---|---|
| 5 | 1.3 | 0 | 0 |
| 10 | 1.8 | 0 | 0 |
| 15 | 2.2 | 0 | 0 |
| 20 | 2.7 | 0 | 0 |
| 25 | 3.2 | 0 | 0 |
| 30 | 3.7 | 0 | 0 |
| 35 | 4.1 | 0 | 0 |
| 40 | 4.6 | 0 | 0 |
| 45 | 5.1 | 0 | 0 |
| 50 | 5.6 | 0 | 0 |
| 55 | 6.1 | 0 | 0 |
| 60 | 6.5 | 0 | 0 |
| 65 | 7.0 | 0 | 0 |
| 70 | 7.5 | 0 | 0 |
| 75 | 8.0 | 0 | 0 |
| 80 | 8.4 | 0 | 0 |
| 85 | 8.9 | 0 | 0 |
| 90 | 9.4 | 0 | 0 |
| 95 | 9.9 | 0 | 0 |
| 100 | 10.4 | 0 | 0 |

**25.2.3 – Baseline Wander Correction**

**Requirements**: The receiver shall maintain a bit error rate better than $10^{-8}$ in the presence of worst-case uni- and bi-directional baseline wander events over test channels representing 0%, 75%, and 100% of the worst-case cable attenuation. This implies that no more than 7 out of 20,000 1,518-byte packets may be received in error.

**Results: Uni-Directional**

| Cable Length (m) | Loss at 16 MHz (dB) | Errors (tr = 3 ns) | Errors (tr = 5 ns) |
|---|---|---|---|
| 0 | 0.8 | 0 | 0 |
| 75 | 8.0 | 0 | 0 |
| 100 | 10.4 | 0 | 0 |

**Results: Bi-Directional**

| Cable Length (m) | Loss at 16 MHz (dB) | Errors (tr = 3 ns) | Errors (tr = 5 ns) |
|---|---|---|---|
| 0 | 0.8 | 0 | 0 |
| 75 | 8.0 | 20000 | 20000 |
| 100 | 10.4 | 20000 | 20000 |

**25.2.4 – Bit Error Rate Verification**

**Requirements**: The receiver shall maintain a bit error rate better than $10^{-11}$ over test channels representing 75% and 100% of the worst-case cable attenuation. This implies that no more than 7 out of 20,000,000 1,518-byte packets may be received in error.

**Results:**

| Cable Length (m) | Loss at 16 MHz (dB) | Errors (tr = 3 ns) | Errors (tr = 5 ns) |
|---|---|---|---|
| 75 | 8.0 | 0 | 0 |
| 100 | 10.4 | 0 | 0 |

Figure 1: MLT−3 Eye Diagram (Informative)

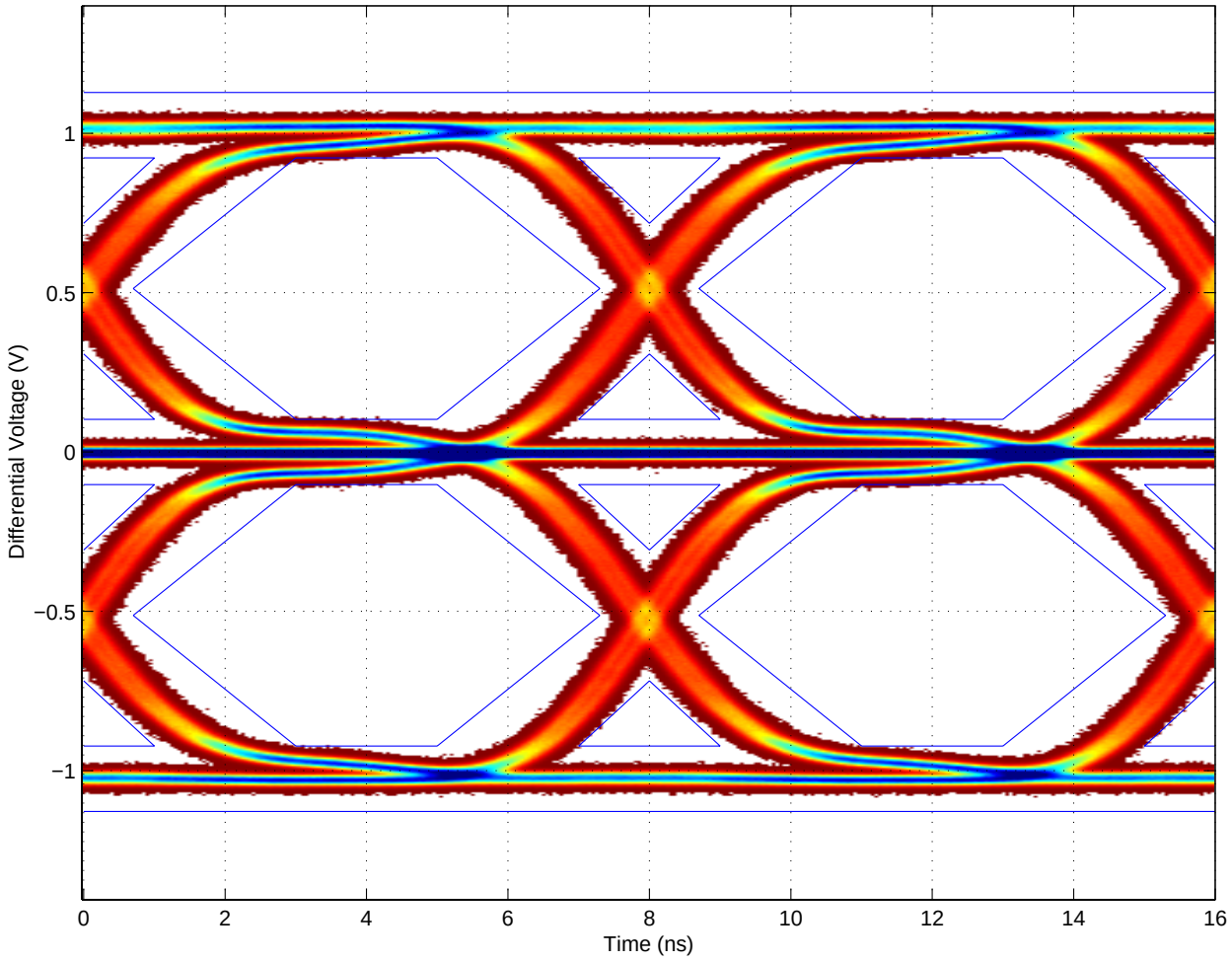

Figure 2: Mean Jitter vs. Edge (Informative)

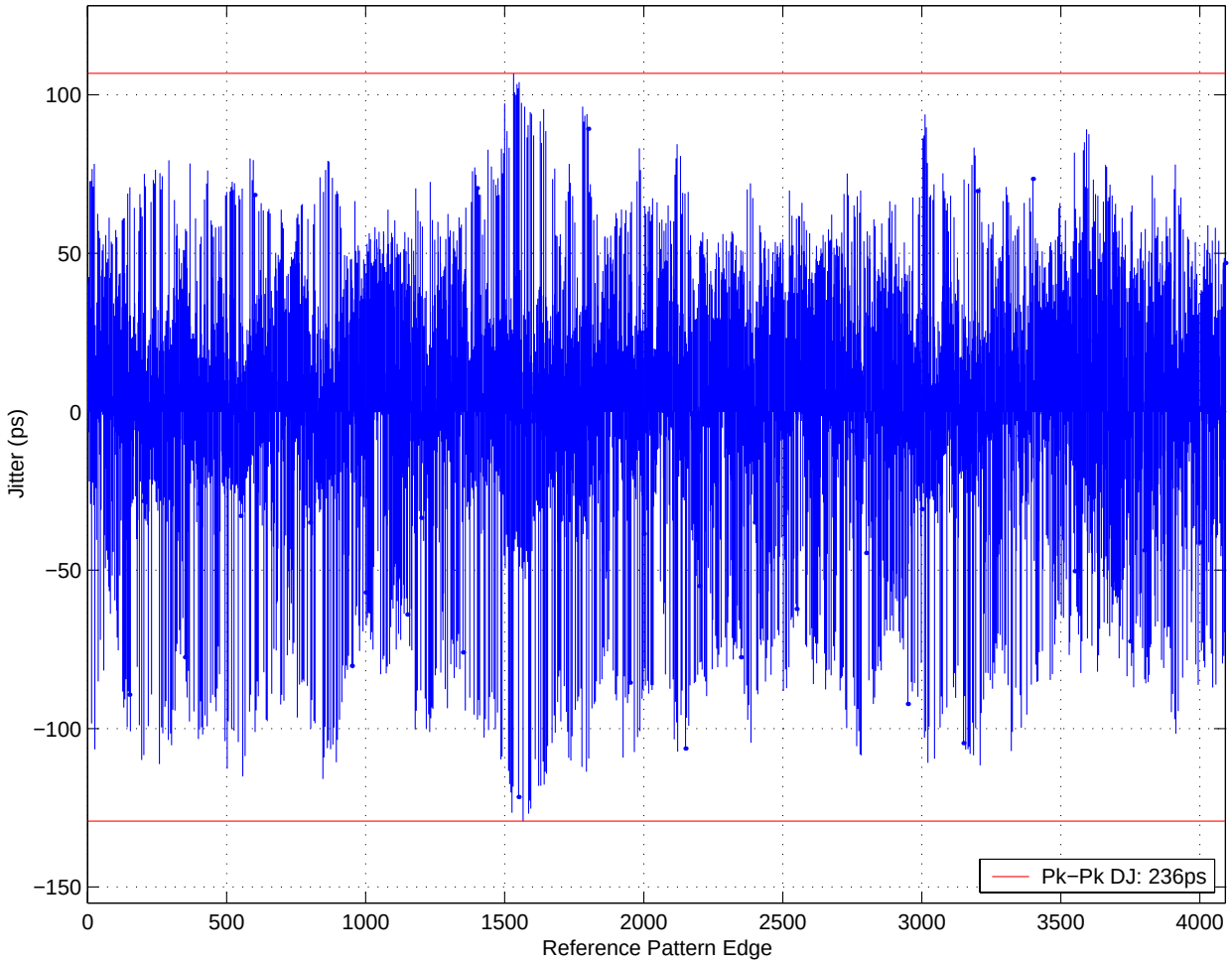

Figure 3: Jitter Sigma vs. Edge (Informative)

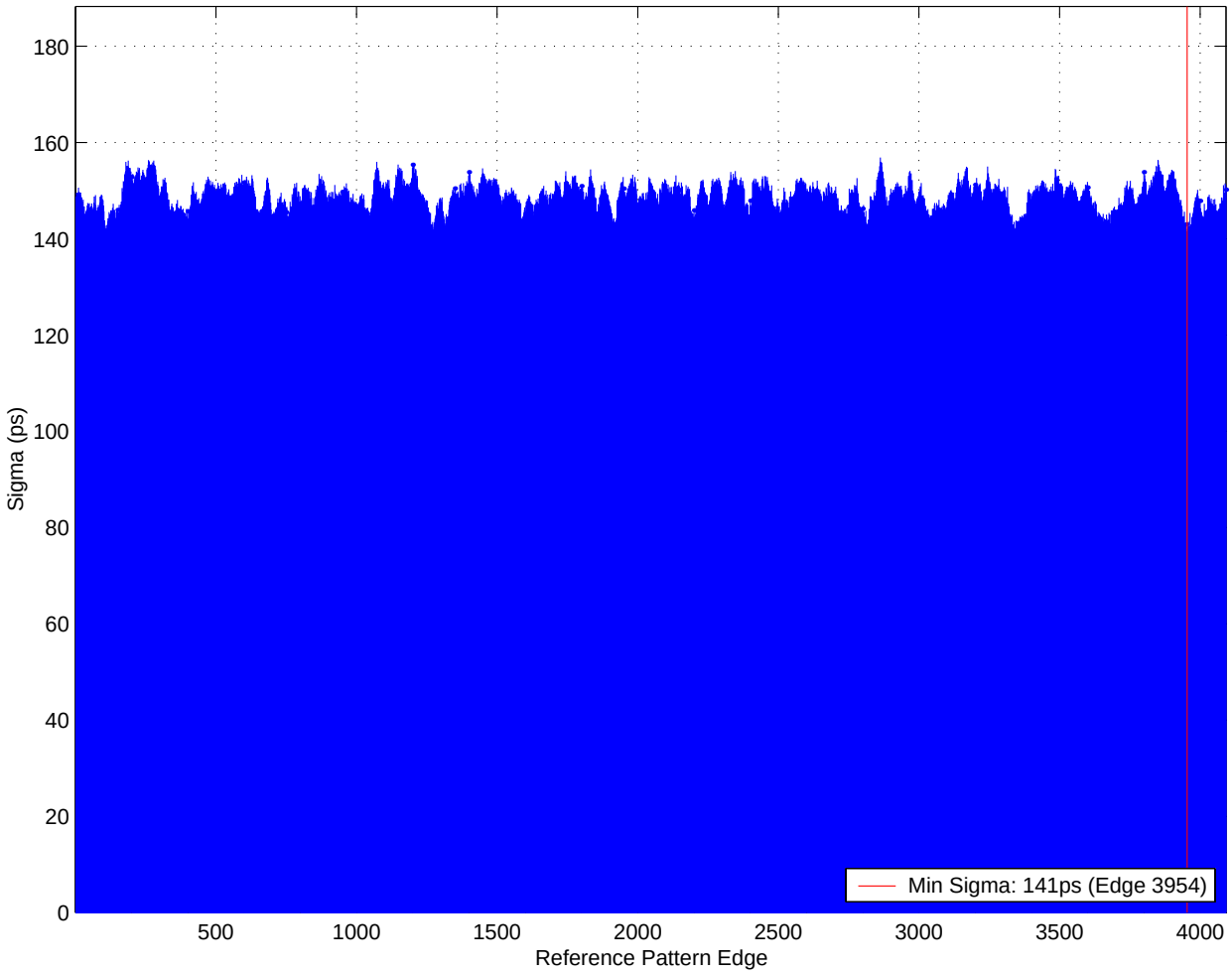

Figure 4: DJ/TJ Jitter Histogram (Informative)

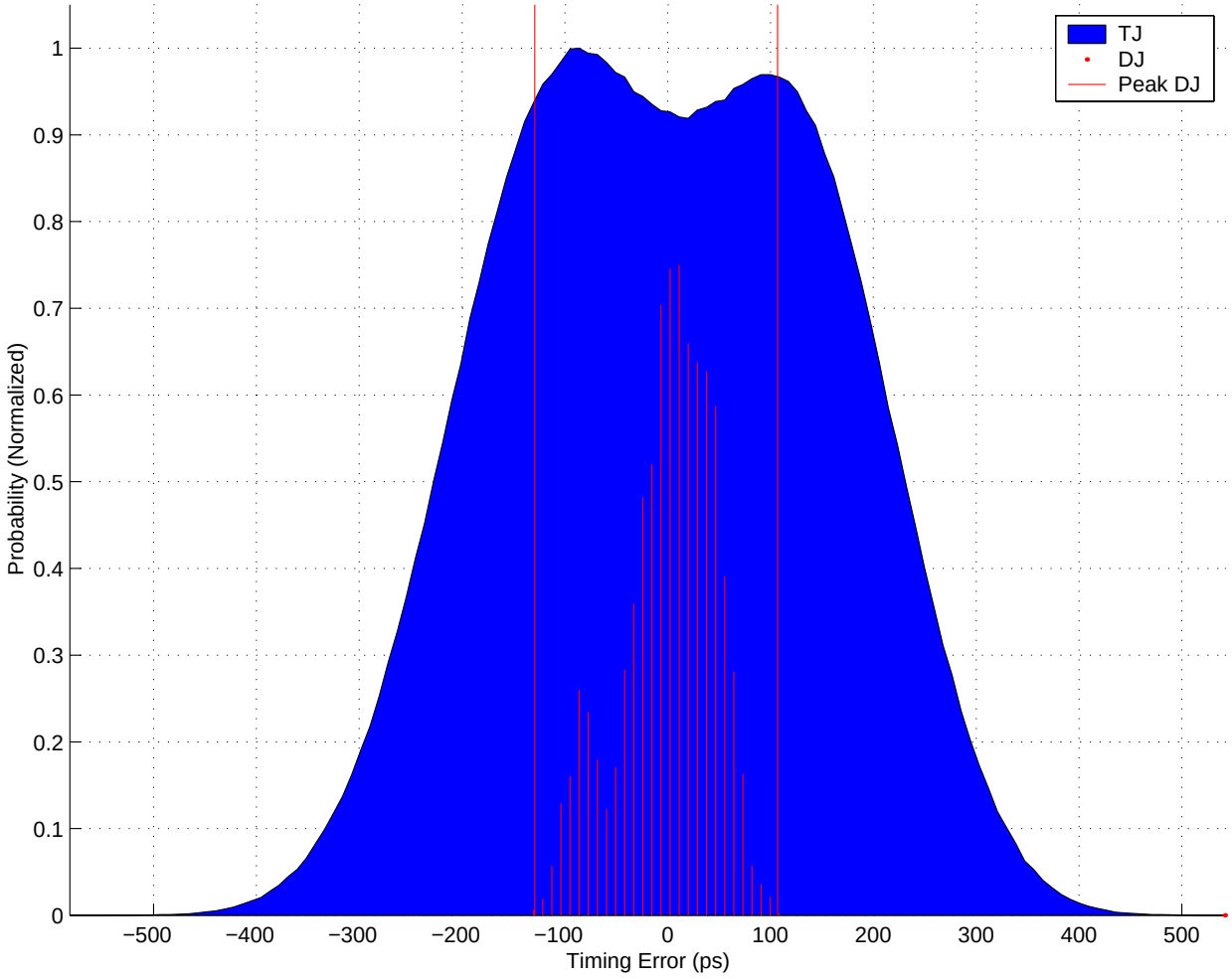

Figure 5: Sample Jitter PSD (Informative)

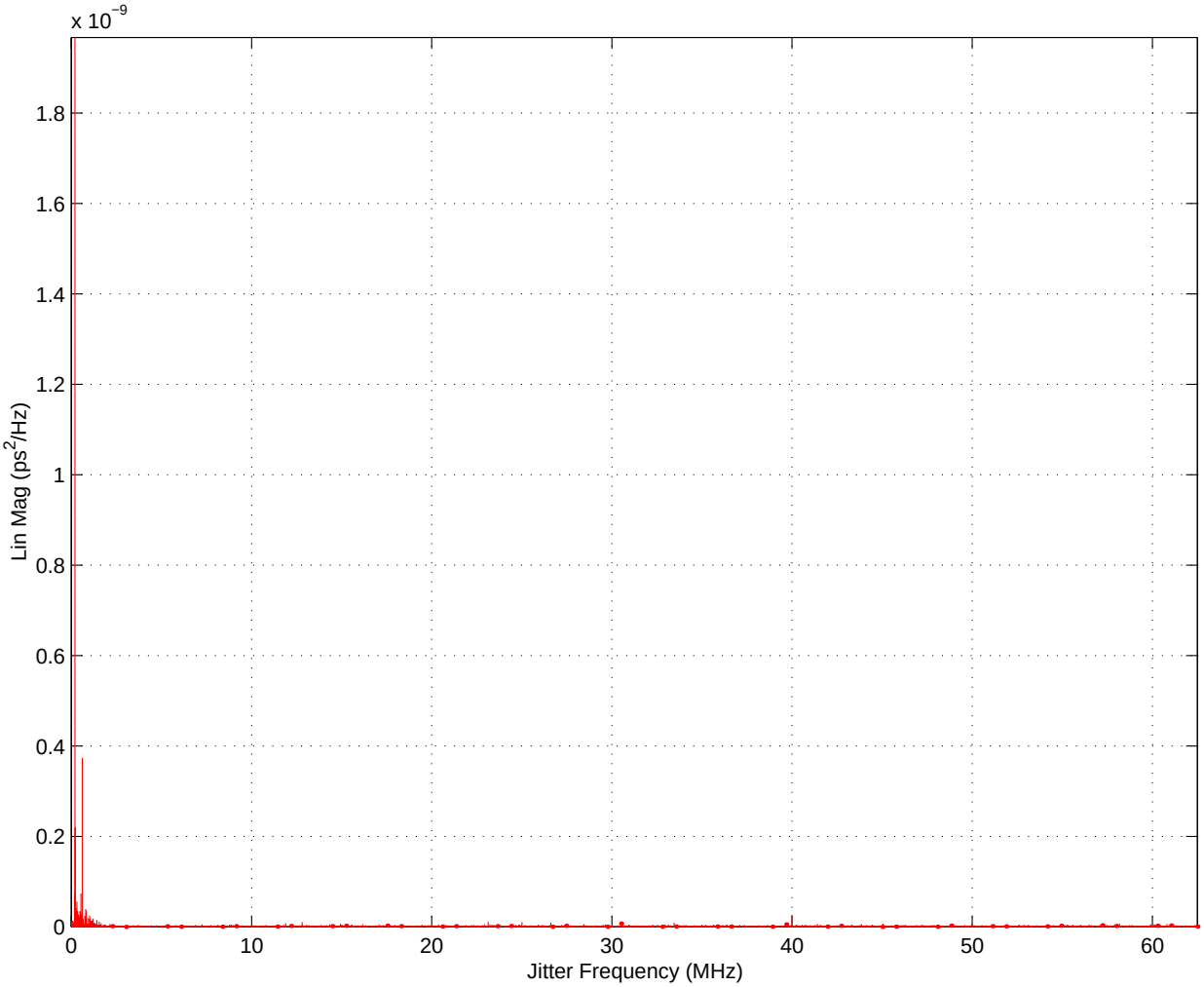

Figure 6: Sample +Vout Reference Waveform (Informative)

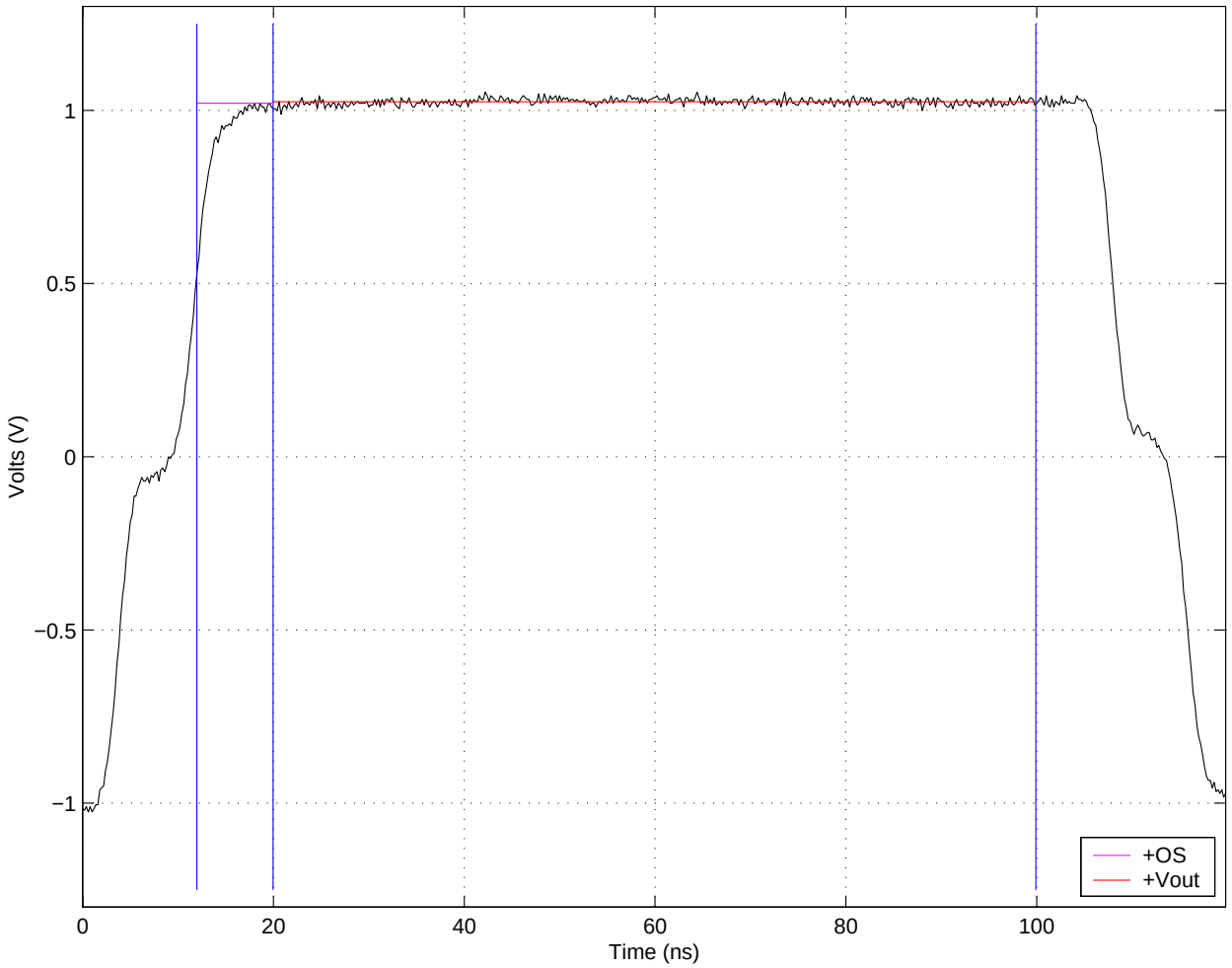

Figure 7: Sample −Vout Reference Waveform (Informative)

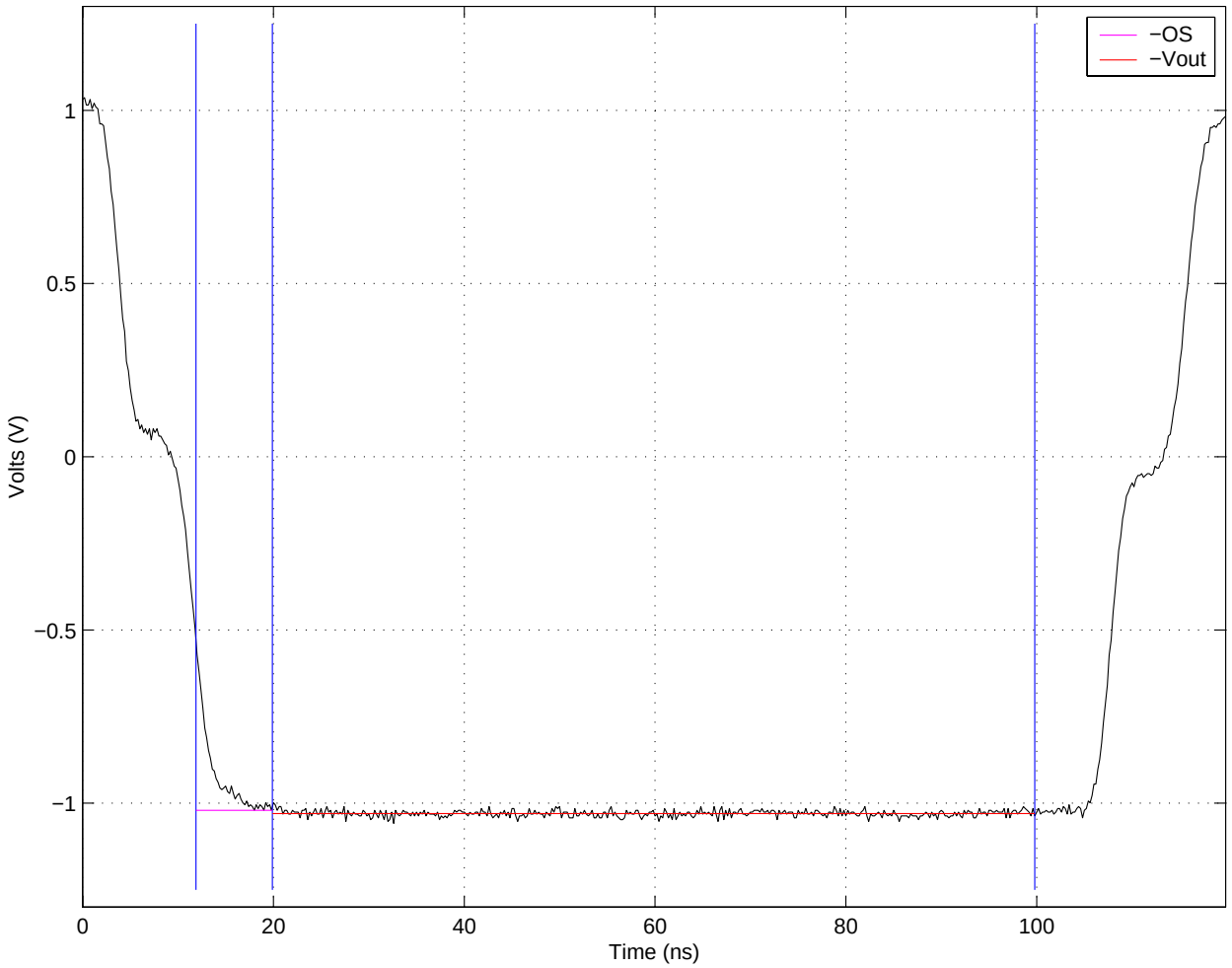

Figure 8: Sample +RFT Reference Waveform (Informative)

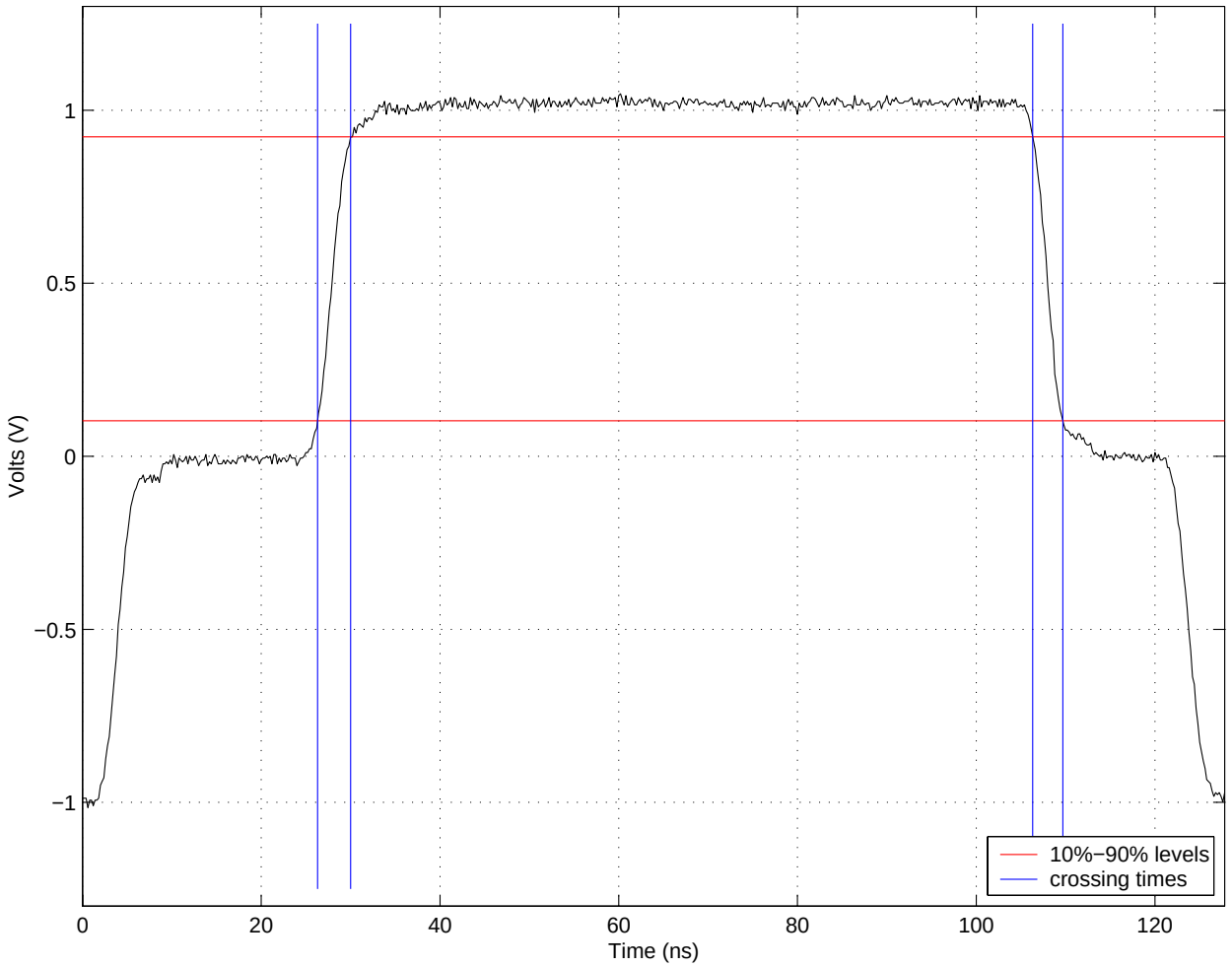

Figure 9: Sample −RFT Reference Waveform (Informative)

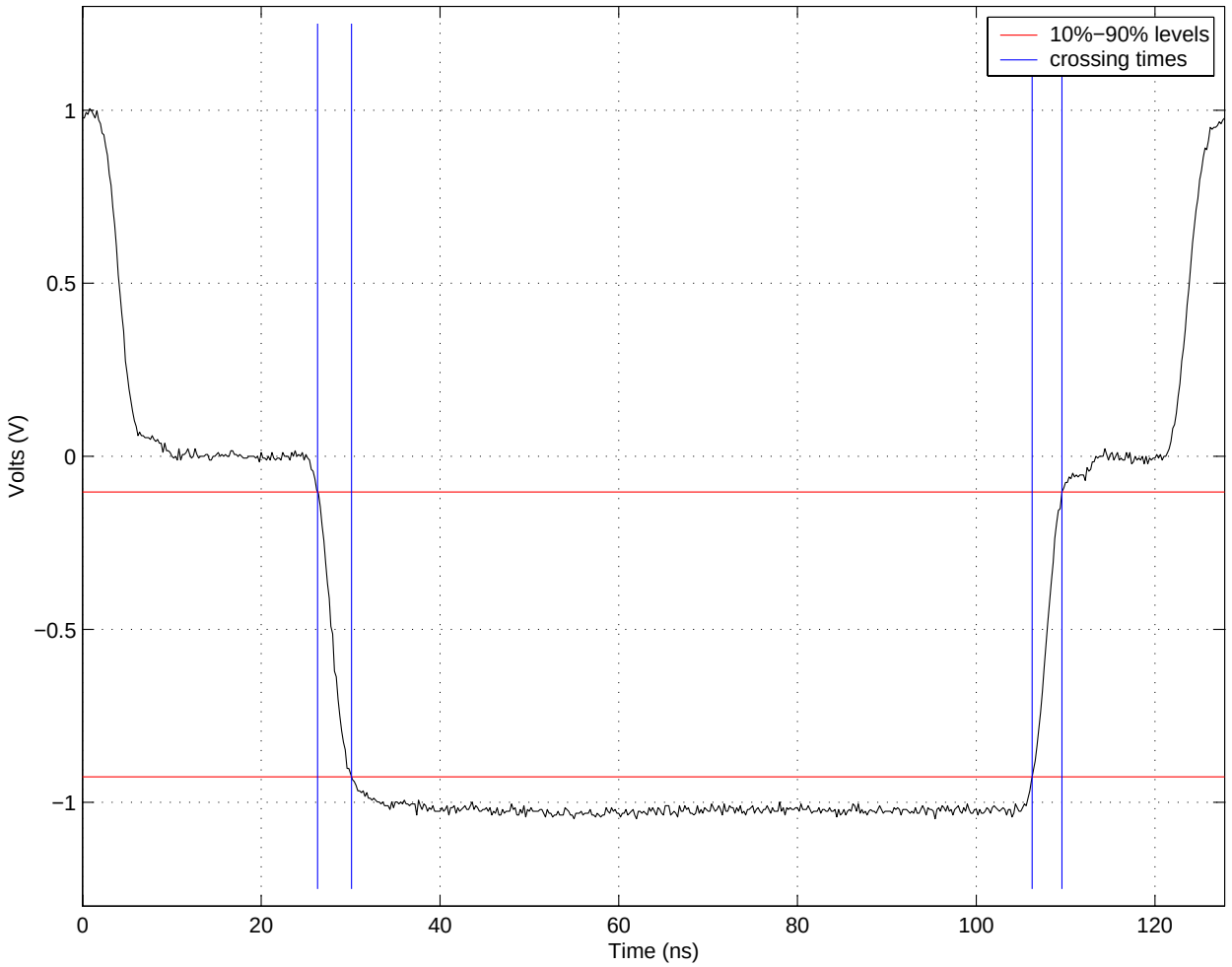

Figure 10: Sample DCD Reference Waveform (Informative)

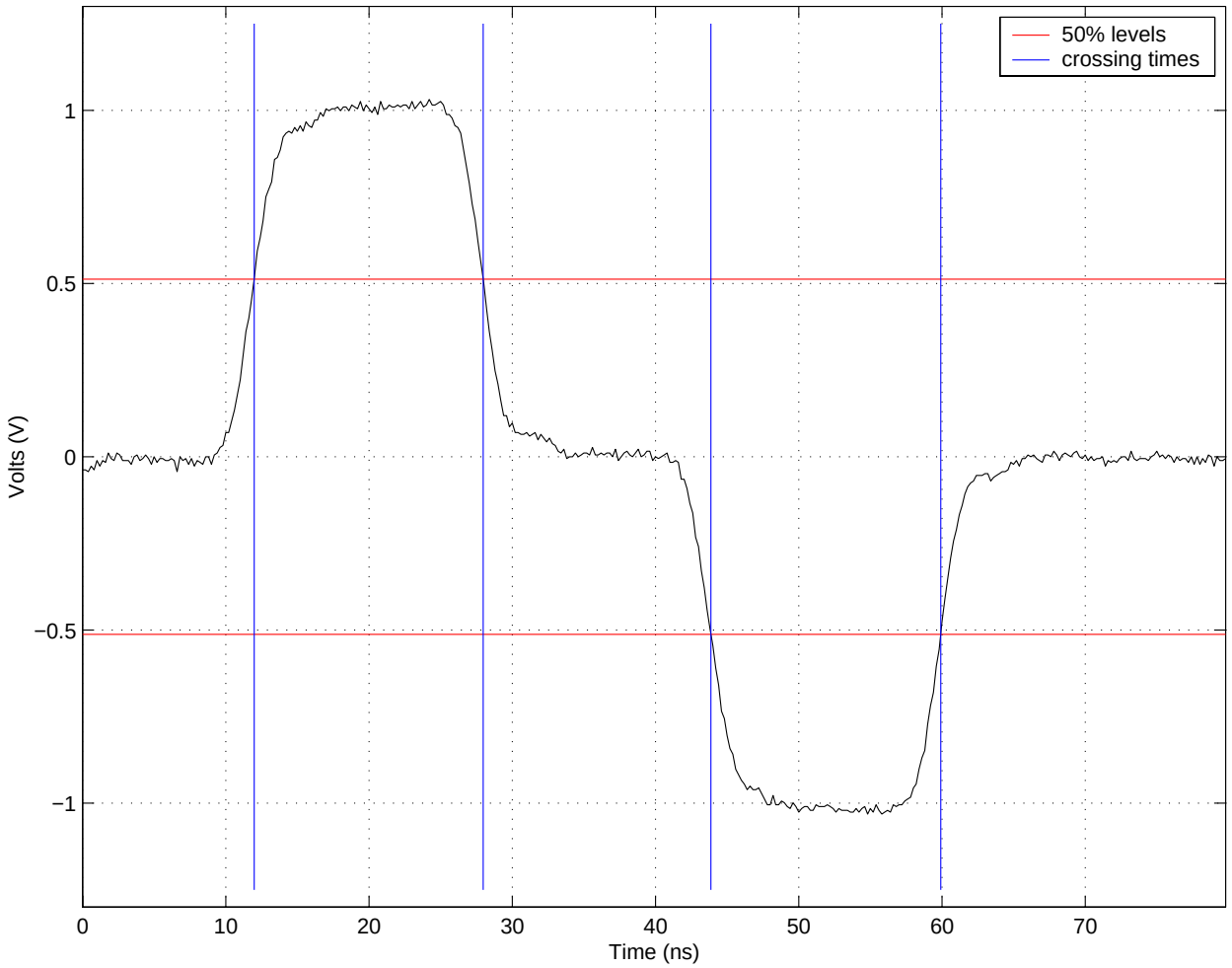

Figure 11: Transmitter Return Loss vs. Frequency

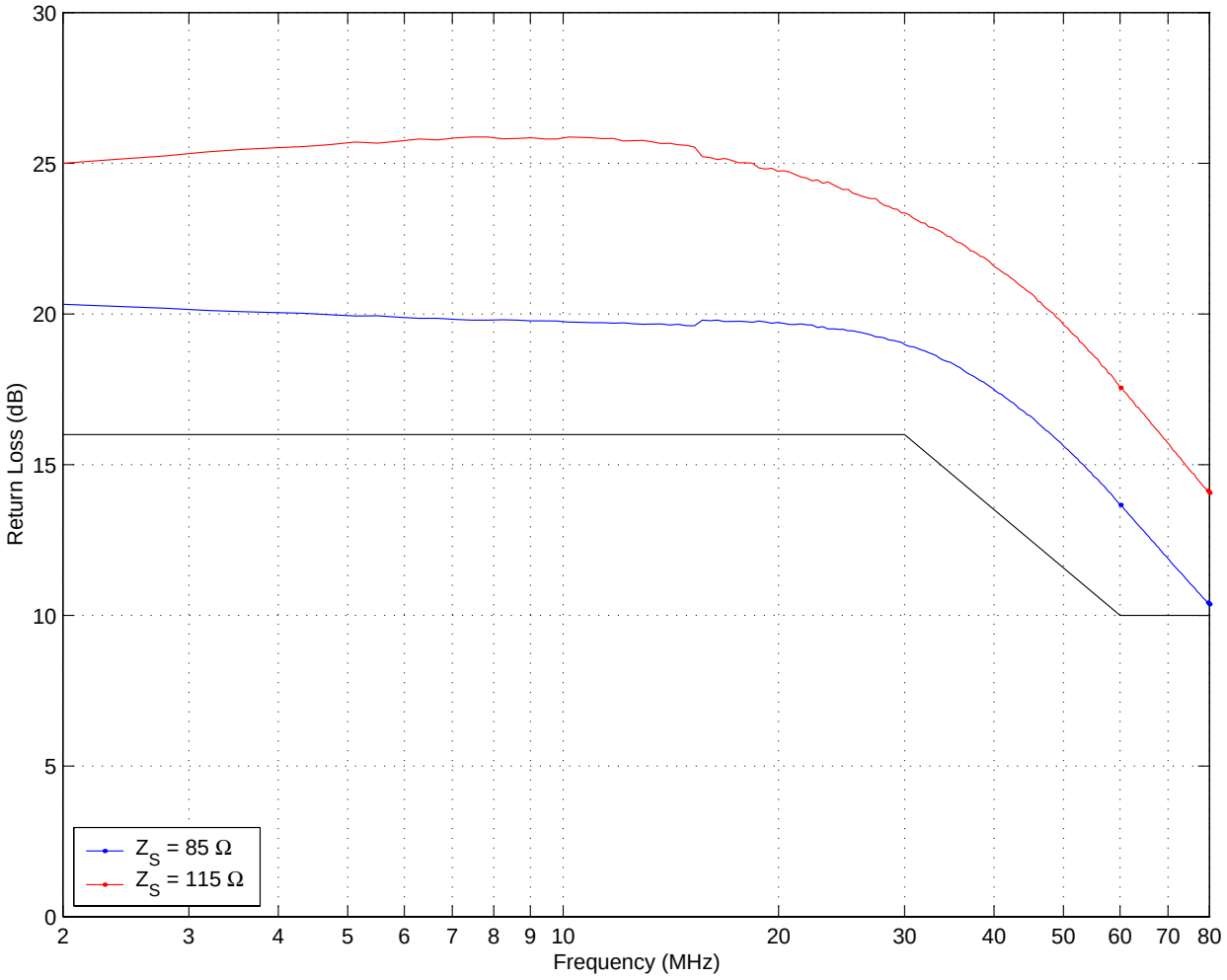

Figure 12: Transmitter Impedance vs. Frequency (Informative)

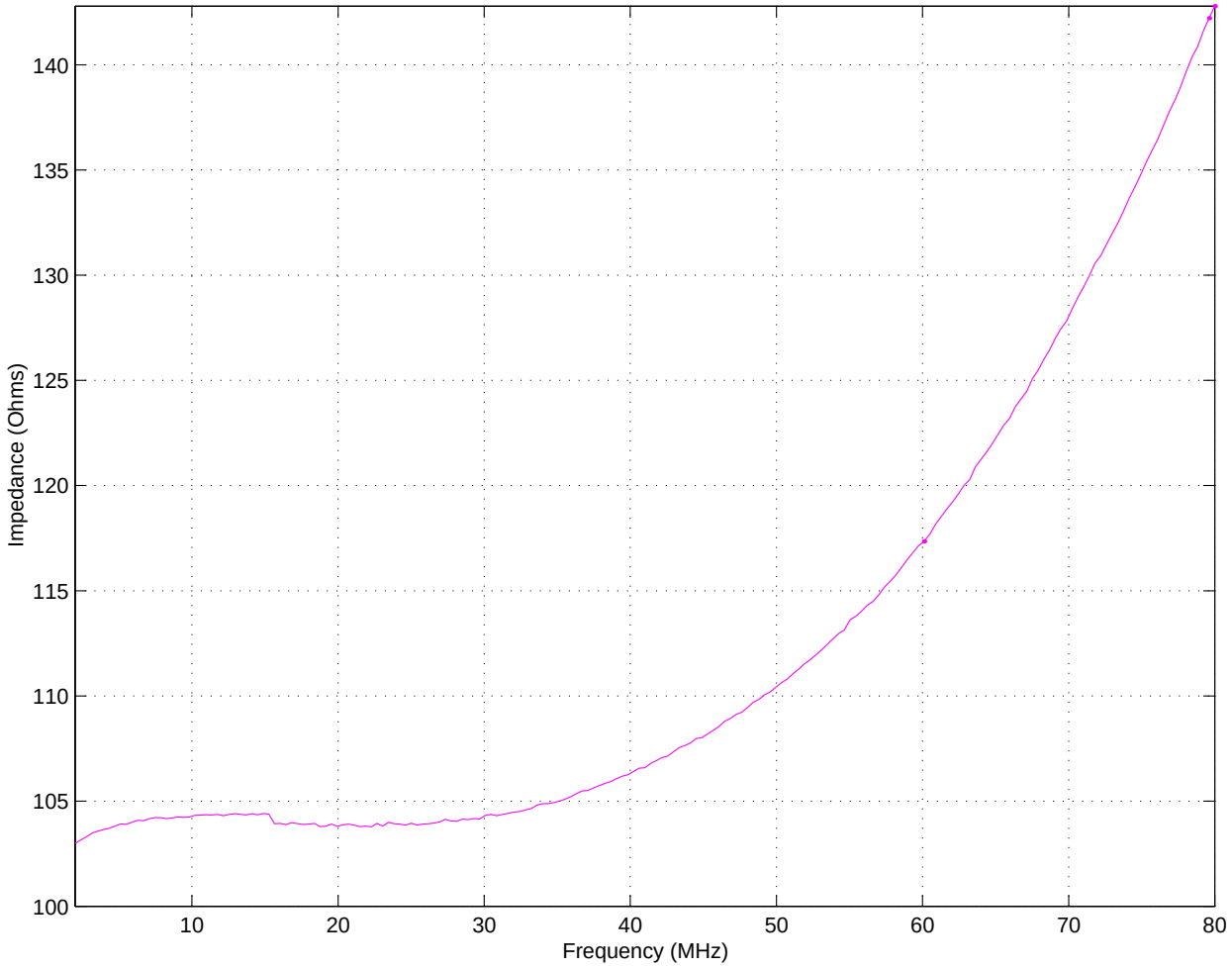

Figure 13: Receiver Return Loss vs. Frequency

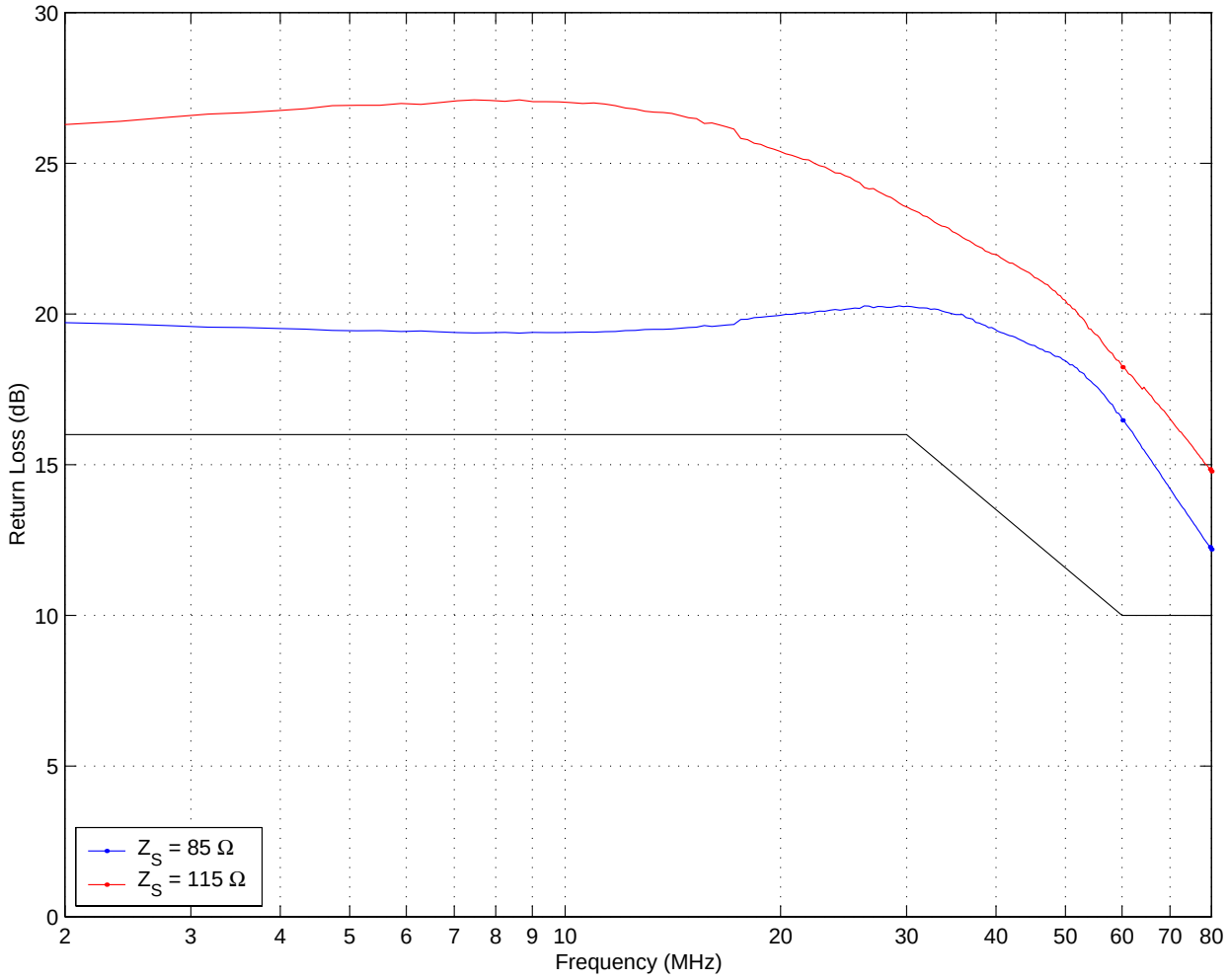

Figure 14: Receiver Impedance vs. Frequency (Informative)