Fast Ethernet Consortium
Clause 25 PMD-EEE Conformance Test Suite v1.1 Report

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Report Rev. 1.0

Enclosed are the results from the Clause 25 PMD-EEE Conformance testing performed on:

Device Under Test (DUT):	CompanyCom DUT 3000
Hardware Version:	Not Available
Firmware Version:	Not Available
Software Version:	Not Available
Miscellaneous:	Port 1 tested
IOL ID:	123456

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL25_PMD/CL25_PMD_EEE_v1.1.pdf

The Following Tests Were Either Not Performed Or Have Additional Comments	
25.1.5 – Transmit Wake Time	These tests were not run as they have not been implemented.
25.2.1 – Adaptive Equalization with Fast Wakeup	
25.2.2 – Clock Tolerance	
25.2.3 – Long Term Frequency Stability	

For specific details regarding issues please see the corresponding test result.

Testing Completed 02/10/2012
Joe Tester
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Digitally signed by UNH-IOL
Date: 2012.02.10 12:55:44 -05'00'

Review Completed 02/10/2012
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Table 1: Hardware Information

100BASE-Tx PHY	
Manufacturer	Not Available
Model	Not Available
Version	Not Available
Magnetics	
Manufacturer	Not Available
Model	Not Available
Version	Not Available
Test System Hardware	
Real-time DSO	TEKTRONIX,TDS7104,B041940,CF:91.1CT FV:2.5.5
Arbitrary Waveform Genearator	SONY/TEK,AWG2041,0,CF:91.1CT FV:1.26

Revision History

The following table contains a revision history for this report:

Rev	**Comments**
1.0	Initial release

Test Setup

All tests in this report were performed using the test setup specified in the 100BASE-TX PMD-EEE Test Suite in the Test Setup section of each test.

Report Key

Table 1 contains setup and configuration information for the Device Under Test (DUT), as well as the test system hardware. A best effort is made to record as much information as possible about the DUT, including hardware, software, and firmware versions, in addition to specific information regarding PHY IC and magnetics packages. The test system hardware information fields display the GPIB device identification strings for each piece of system hardware. These identifiers generally include the manufacturer, model number, serial number, and firmware revision information for the particular piece of equipment, however the amount of detail can vary depending on the instrument.

Table 2 summarizes the electrical conformance requirements and results, listed by IOL test number. A brief description is given for each parameter, along with the range of conformant values and the values measured during testing. There is also a convenient link to the figure that is relevant to the specific test. (Complete test descriptions can be found in the 100BASE-TX PMD-EEE test suite).

Table 3 summarizes the packet-based receiver testing conformance requirements and results, listed by IOL test number.

The remainder of the report contains graphical supplements to the tabulated results. Most of these supplements are informative, and are included to provide insight into the measurement methodologies used to generate the numerical results. A brief explanation of each figure is provided here:

Figure 1 contains the MLT-3 eye pattern for the DUT. It is a persistence waveform generated in MATLAB from the actual waveform data acquired during the jitter test. It is shown along with the eye mask specified in ANSI-X3.263. It should be noted that the eye mask is considered informative by ANSI-X3.263, and no part of the eye pattern or mask is used for generating numerical results. It is intended to serve as a 'feel good' measure to show overall signal shape.

Figure 2 contains statistical information pertaining to jitter. During the jitter measurement, sufficient timing information is gathered such that the timing error on each edge of the reference pattern waveform is observed for a minimum of 6107 observations, which translates to 100ms. The max, min, mean, and sigma values are tracked for each edge of the reference pattern. Figure 2 shows the final values of the mean timing error per edge of the reference pattern. The peak-to-peak value of this distribution is taken to be the Deterministic Jitter (DJ) component, and is ultimately combined with the Random Jitter (RJ) component (discussed below) to determine the peak-to-peak Total Jitter (TJ). The numerical value of the peak-to-peak DJ is displayed in the plot legend.

Figure 3 is similar to Figure 2, however this figure shows the final sigma values for the jitter on each edge of the reference pattern. This information relates to the amount of Random Jitter (RJ) present in the signal. If RJ is modeled as a purely Gaussian phenomenon, and DJ is modeled as a pair of delta functions (as is the case in the simplest jitter models, such as the one presented in Appendix 25.B of the Test Suite), all edges, in theory, would be equally impacted by the effects of RJ, resulting in the same sigma value being observed for every edge. Because real-world jitter does not perfectly adhere to the dual-Dirac jitter model (particularly in the case of DJ, which can often be multi-modal), the sigma distribution generally tends to span some range (although the distribution shown in Figure 3 generally appears to be fairly uniform). Thus, the question arises as to which sigma value to use when computing the Total Jitter computation. Since true RJ should affect all edges equally, the smallest sigma value is chosen, as its value is effectively contained in every edge of the pattern. Figure 3 shows a vertical red line at the location of the minimum sigma value, and also displays the sigma value itself in the plot legend. The peak-to-peak Total Jitter reported in the table of results is then computed as the sum of the peak-to-peak DJ from Figure 2, plus 10 times the sigma value shown in Figure 3. The 10x multiplier corresponds to +/- 5 standard deviations, which corresponds to a BER of approximately 1E-7.

Figure 4 (informative) shows another statistical view of jitter through a combined DJ/TJ histogram. In addition to accumulating the max, min, mean, and sigma values, and additional array is accumulated during the jitter

test, which contains all of the timing error values for all observed edges. The histogram of this array produces the Total Jitter histogram shown in blue in Figure 4. Histogramming the DJ values of Figure 2 with the same bin values as the TJ histogram generates the DJ histogram, shown as a red stem plot in Figure 4. In theory, the convolution of the DJ stem plot with a Gaussian having sigma equal to the value obtained from Figure 3 should produce the blue Total Jitter histogram of Figure 4. The DJ histogram is represented as a stem plot purely for visualization purposes, and helps in visually 'extracting' the DJ distribution from the blue Total Jitter histogram.

Figure 5 (informative) shows yet another view of jitter, namely in the frequency domain. For a single 8188-UI-long block of waveform data, one can construct a 'jitter waveform' by plotting the timing error on each edge versus the UI offset for that edge. The magnitude of the FFT of this waveform produces the power spectrum shown in Figure 5. In theory, the 'noise floor' of this spectrum corresponds to RJ, while prominent spikes are attributable to DJ. Because the spectrum shown in Figure 5 is generated using only a single block of data (i.e., no averaging applied), the spectrum is only a rough estimate, however it is usually sufficient to reveal large DJ spikes which are often prevalent at the harmonics of the base oscillator frequency of the transmitter IC.

Figure 6 shows a sample capture of the Sleep signaling when measuring Sleep time.

Figure 7 shows a sample capture of the Quiet period between Refresh signaling.

Figure 8 shows a sample capture of the Refresh signaling when measuring Refresh time.

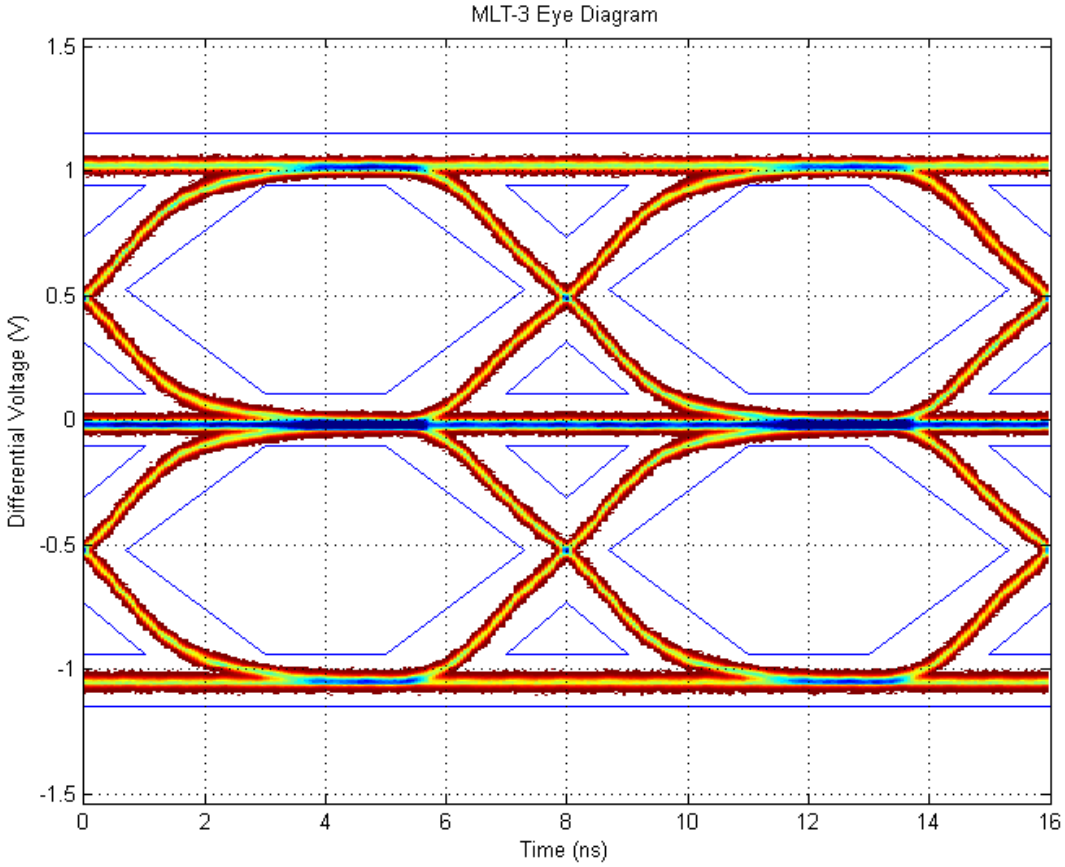
Table 2: Summary of Electrical Requirements and Results

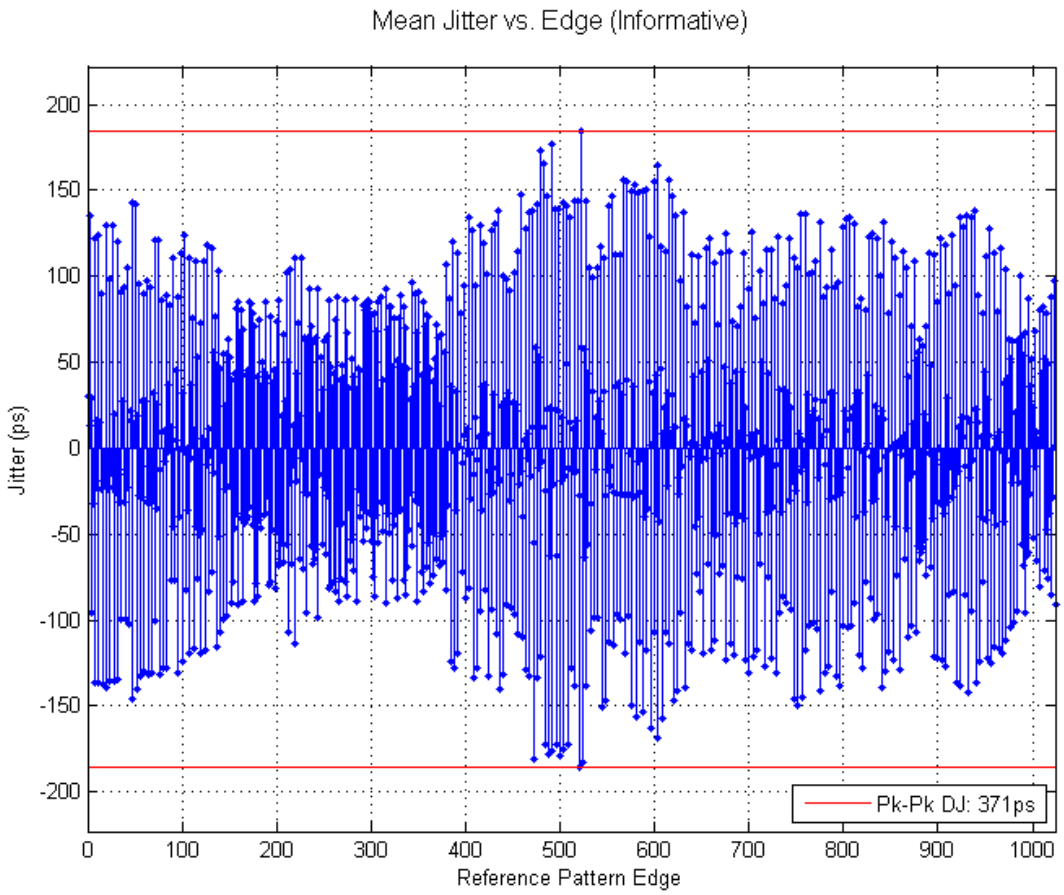
Parameter	Min	Max	Min (measured)	Max (measured)	Units	Figure
25.1.1 – Transmitter Timing Jitter						
Peak-to-peak total jitter (TJ)	N/A	1.4	N/A	0.66	ns	1,2,3,4,5
25.1.2 – Sleep Time						
Sleep signal time	200	220	209.86	209.88	us	6
25.1.3 – Quiet Time						
Time between Sleep and Refresh	20	22	21.00	21.00	ms	7
25.1.4 – Refresh Time						
Refresh signal time	200	220	209.80	210.04	us	8
25.1.5 – Transmit Wake Time						
Amount of time IDLE is transmitted before a frame	25	Inf	N/A*	N/A*	us	

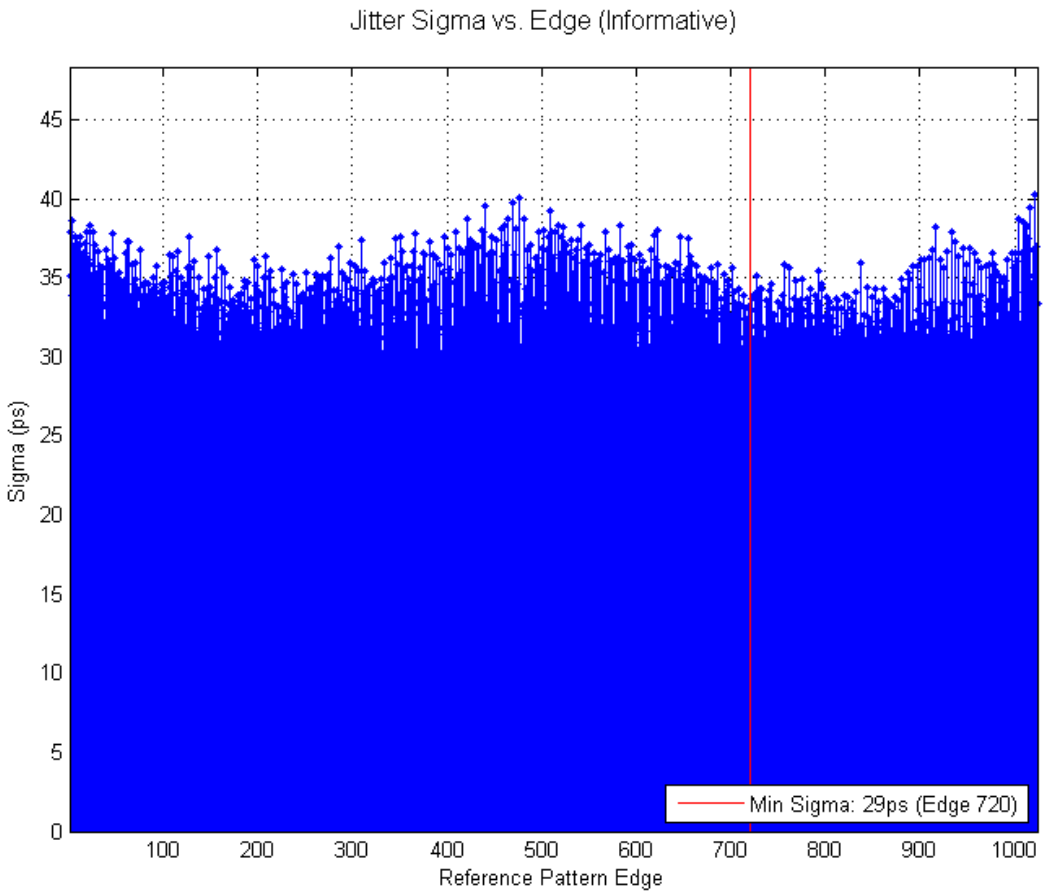
*This test is currently in development.

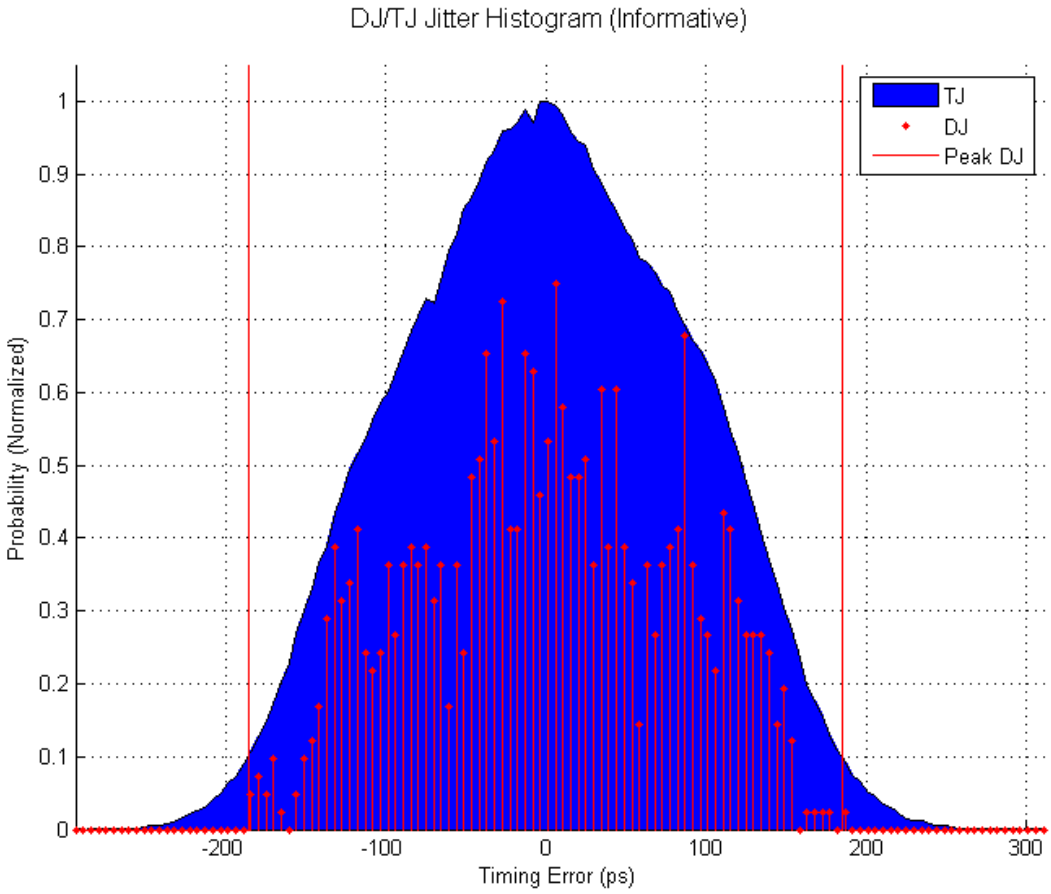
Table 3: Summary of Packet-based Receiver Testing Requirements and Results

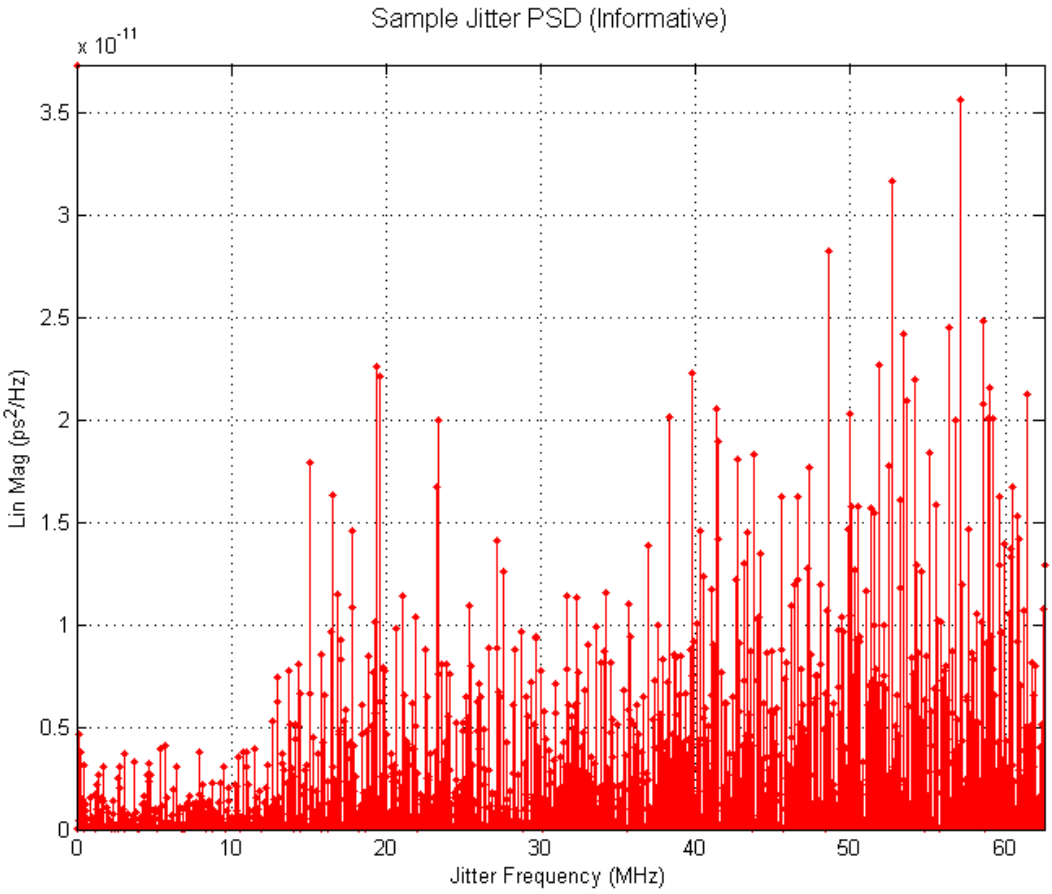
Test Parameter	
25.2.1 – Adaptive Equalization with Fast Wakeup	
Requirements	The receiver shall maintain a bit error rate better than 10^{-8} over test channels representing 20% to 100% (20% increments) of the worst-case cable attenuation while operating in Energy Efficient Ethernet mode. This implies that no more than 7 out of 500,000 64-byte packets may be received in error.
Results:	N/A*
	*This test is currently in development.
25.2.2 – Clock Tolerance	
Requirements	The receiver shall maintain a bit error rate better than 10^{-8} while tracking a varying clock source over test channels representing 0%, 75%, and 100% of the worst-case cable attenuation. This implies that no more than 7 out of 20,000 1,518-byte packets may be received in error.
Results:	N/A*
	*This test is currently in development.
25.2.3 – Long Term Frequency Stability	
Requirements	The receiver shall maintain a bit error rate better than 10^{-8} while operating in Low Power Idle mode for extended periods of time over test channels representing 75% and 100% of the worst-case cable attenuation. This implies that no more than 7 out o500,000 64-byte packets may be received in error.
Results:	N/A*
	*This test is currently in development.

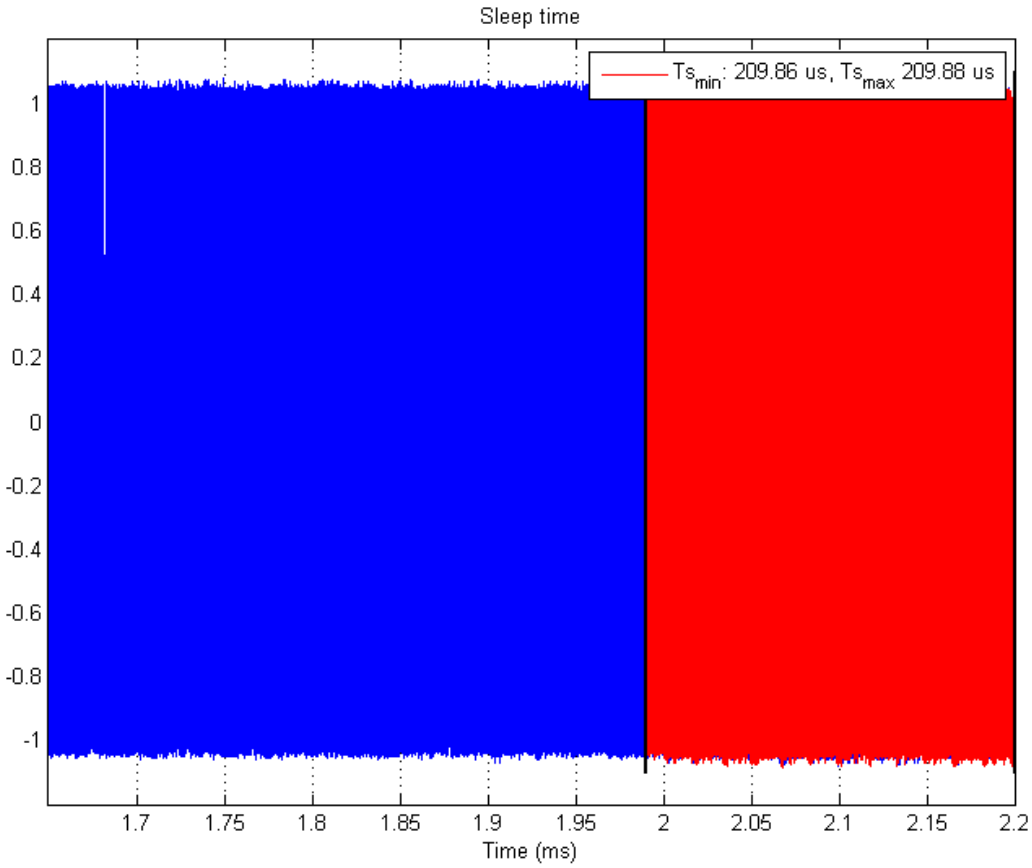

MLT-3 Eye Diagram
Differential Voltage (V)
Time (ns)
1.5
1
0.5
0
-0.5
-1
-1.5
0
2
4
6
8
10
12
14
16

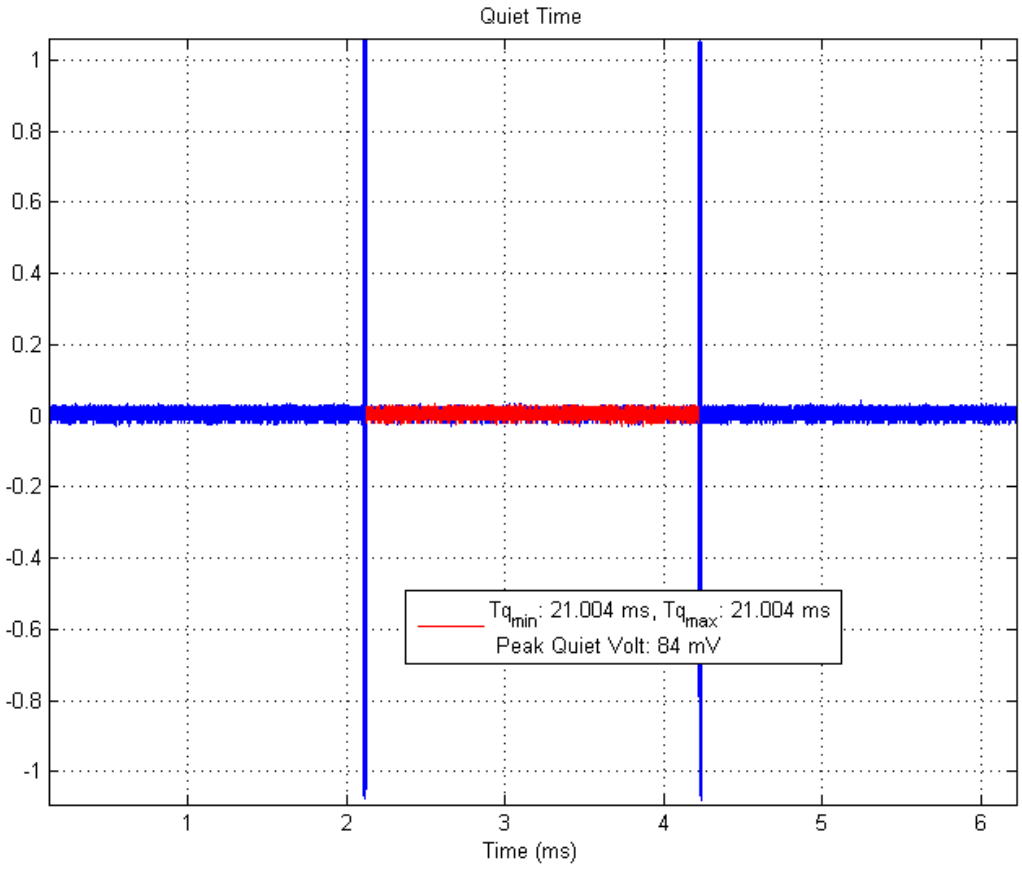

Mean Jitter vs. Edge (Informative)
Jitter (ps)
Reference Pattern Edge
Pk-Pk DJ: 371ps
200
150
100
50
0
-50
-100
-150
-200
0
100
200
300
400
500
600
700
800
900
1000

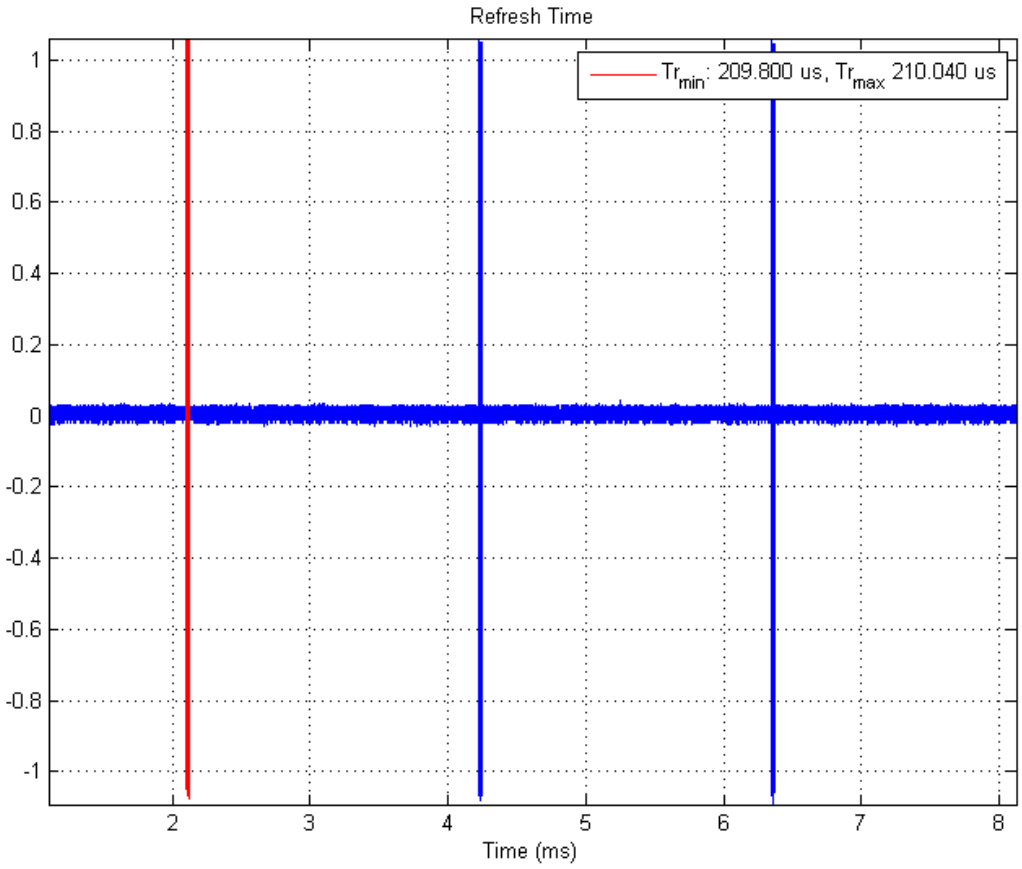

Jitter Sigma vs. Edge (Informative)
Sigma (ps)
Reference Pattern Edge
Min Sigma: 29ps (Edge 720)
0
5
10
15
20
25
30
35
40
45
100
200
300
400
500
600
700
800
900
1000


DJ/TJ Jitter Histogram (Informative)
TJ
DJ
Peak DJ
Probability (Normalized)
Timing Error (ps)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
-200
-100
0
100
200
300


Sample Jitter PSD (Informative)
x 10^-11
Lin Mag (ps^2/Hz)
Jitter Frequency (MHz)
0
0.5
1
1.5
2
2.5
3
3.5
0
10
20
30
40
50
60


Sleep time
Ts_min: 209.86 us, Ts_max 209.88 us
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
1.7
1.75
1.8
1.85
1.9
1.95
2
2.05
2.1
2.15
2.2
Time (ms)


Quiet Time
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
1
2
3
4
5
6
Time (ms)
Tq_min: 21.004 ms, Tq_max: 21.004 ms
Peak Quiet Volt: 84 mV


Refresh Time
Tr_min: 209.800 us, Tr_max 210.040 us
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
2
3
4
5
6
7
8
Time (ms)