Backplane Ethernet Consortium
Clause 72 PMD Conformance Test Suite v1.0 Report

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Report Rev. 1.0

Enclosed are the results from the Clause 72 PMD Conformance testing performed on:

Device Under Test (DUT):	SuperDUT 23
Hardware Version:	Not Available
Miscellaneous:	Port 42 tested
IOL ID:	N/A

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL72_PMD/CL72_PMD_Test_Suite_v1.0.pdf

Issues Observed While Testing
72.1.3 – Differential Output Amplitude – The DUT was observed to have a peak-to-peak voltage with transmitter disabled value that is higher than 30mV.
72.1.7 – Transmitter Output Waveform Requirements Related to Coefficient Status – The DUT was observed to R_{pre} and R_{pst} values outside the conformant range.

For specific details regarding issues please see the corresponding test result.

Note: This is a sample report and the values included in table 2 may not reflect those seen in the figures.

Testing Completed: 9/12/2009

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Digitally signed by UNH-IOL
Date: 2011.08.01 14:47:36 -04'00'

Review Completed: 10/3/2009

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Table 1 – Hardware Information

Test Setup Information	
SMA cables	Huber-Suhner
Test System Hardware	
Real-time DSO	Agilent MSO81403A
Sampling DSO	Tektronix CSA8000B
Vector Network Analyzer	Agilent 8720ES
Test System Software	UNH-IOL Matlab 10GBASE-KR Test System v0.1

Test Setup

All tests in this report were performed using the test setup specified in the 10GBASE-KR PMD Test Suite in the Test Setup section of each test. Diagrams showing physical connections and measurement planes are shown below.

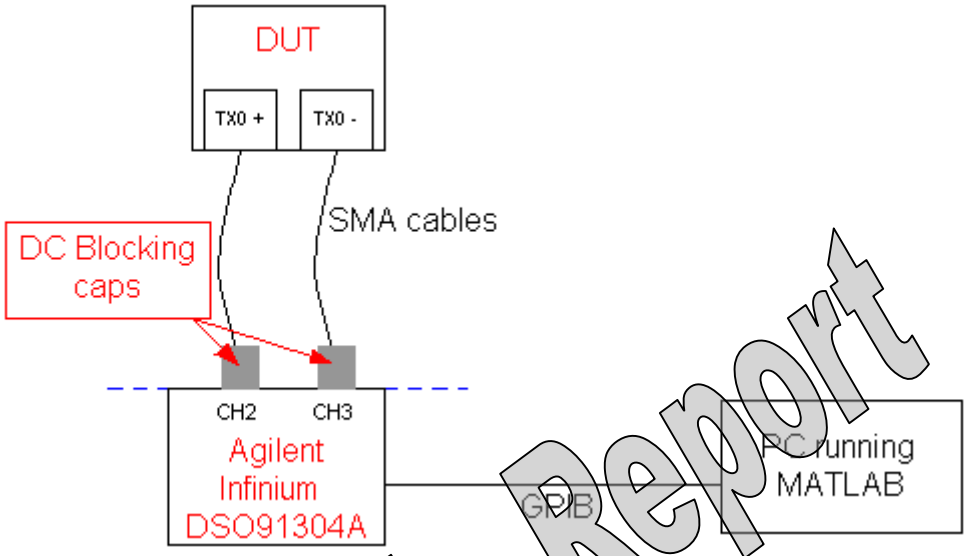

Figure A: Real-Time scope setup for 10GBASE-KR PMD Tests

This setup was used to perform the signaling speed, jitter, and coefficient update tests

Report Key

Table 1 contains setup and configuration information for the Device Under Test (DUT), as well as the test system hardware and software. A best effort is made to record as much information as possible about the DUT, including hardware, software, and firmware versions, in addition to specific information regarding PHY IC and magnetics packages. The test system hardware information fields display the GPIB device identification strings for each piece of system hardware. These identifiers generally include the manufacturer, model number, serial number, and firmware revision information for the particular piece of equipment, however the amount of detail can vary depending on the instrument.

Tables 2, 2a, and 2b summarize the transmit electrical conformance requirements and results, listed by IOL number. A brief description of each test parameter is given, along with the conformant values and values measured during testing. Table 2a summarizes the requirements for the coefficient update process, while table 3 shows the results. Table 3 gives the requirements and results for the tests performed in section 2, relating to impedance at TP1.

Figure 1 shows a sample waveform (containing 8 1's and 8 0's) that was used to make coefficient update measurements on

Figures 2-4 show statistics related to the coefficient update process. Figure 2 shows the difference between each update for v1, v2, and v3 for tests #1-6 in table 3, and the maximum difference between v1, v2, and v3 for each update. Figure 3 shows symmetry values between v1/v4, v2/v5, and v3/v6 for tests #1-10 in table 3. Figure 4 shows both the value of v2 for all coefficient update tests, as well as the Δv2 and Δv5 values.

Figure 5 shows histograms of measured rising and falling times on a data pattern containing 8 1's and 8 0's, with coefficients configured for [Disabled, Maximum, Disabled]. Figure 6 shows a sample waveform for this measurement.

Figure 7 shows jitter statistics gathered on a PRBS31 waveform, and figure 8 shows the pulse width over time for the same waveform.

Figure 8 shows the Tx/Rx Differential and Common Mode Return Loss measurement.

GROUP 1 – PMD Electrical Specifications

Table 2 – Test Requirements and results

Parameter				Min	Max	Measured	Units	Figure
72.1.1 – Signaling Speed								
Signaling speed minus 10.3125 Gbaud				-1.03125	1.03125	-0.08218	MBd	
72.1.2 – Common Mode Output Voltage								
Common-Mode Output Voltage				0	1.9	0.24	V	
72.1.3 – Differential Output Amplitude								
Maximum peak-to-peak differential output voltage				0	1200	946.10	mV	
Maximum peak-to-peak differential output voltage, transmitter disabled				0	30	(58.2)	mV	
72.1.4 – Transition Time								
20% to 80% rising edge transition time				24	47	35.4	ps	1, 2
80% to 20% falling edge transition time				24	47	32.5	ps	
72.1.5 – Transmit Jitter								
Peak-to-peak Random Jitter				0	0.15	0.02	UI	3, 4
Peak-to-peak Deterministic Jitter				0	0.15	0.05	UI	
Peak-to-peak Duty Cycle Distortion				0	0.035	0.021	UI	
Peak-to-peak Total Jitter				0	0.3	0.21	UI	
72.1.6 – Transmitter Output Waveform Requirements Related to Coefficient Update								
Pre and post update voltage levels				Table 2a		Table 2b		5, 6, 7, 8
Magnitude in changes of v_1, v_2, and v_3 for 1 update (max)				0	5	4.27	mV	
v_2 (min)				40	--	67	mV	
Peak-to-peak Δv_2 (max)				0	40	22.36	mV	
Peak-to-peak Δv_5 (max)				0	40	16.94	mV	
v_1/v_4 symmetry (max magnitude)				0	0.05	0.012		
v_2/v_5 symmetry (max magnitude)				0	0.05	0.034		
v_3/v_6 symmetry (max magnitude)				0	0.05	0.022		
72.1.7 – Transmitter Output Waveform Requirements Related to Coefficient Status								
Rpre	Disabled	Minimum	Disabled	0.90	1.10	1.02		5, 6, 7, 8
	Disabled	Maximum	Disabled	0.95	1.05	(1.33)		
	Disabled	Minimum	Minimum	1.54	--	2.36		
Rpst	Disabled	Minimum	Disabled	0.90	1.10	1.01		
	Disabled	Maximum	Disabled	0.95	1.05	0.98		
	Minimum	Minimum	Disabled	4	--	(3.52)		
v2	Disabled	Minimum	Disabled	220	330	300	mV	
	Disabled	Maximum	Disabled	400	600	472	mV	

Table 2a – Coefficient Update Test Requirements

c(-1)	c(0)	c(1)	v_1 diff	v_2 diff	v_3 diff
Increment	Hold	Hold	–20 to –5	5 to 20	5 to 20
Decrement	Hold	Hold	5 to 20	–20 to –5	–20 to –5
Hold	Increment	Hold	5 to 20	5 to 20	5 to 20
Hold	Decrement	Hold	–20 to –5	–20 to –5	–20 to –5
Hold	Hold	Increment	5 to 20	5 to 20	–20 to –5
Hold	Hold	Decrement	–20 to –5	–20 to –5	5 to 20

Table 2b – Coefficient Update Test Results

Test	c(-1)	c(0)	c(1)	v_1	v_2	v_3	v_1 diff	v_2 diff	v_3 diff	v_n diff mag	Δv_2	R_{pre}	R_{pst}
0				193	173	225	N/A	N/A	N/A	N/A	25.8	1.3	1.41
1	Inc	Hold	Hold	232	**211**	333	**-6.59**	**8.25**	**7.86**	**1.66**	**25.05**	1.29	1.31
2	Dec	Hold	Hold	223	**113**	125	**6.51**	**-9.8**	**-7.74**	**1.37**	**25.75**	1.31	1.41
3	Hold	Inc	Hold	151	**321**	233	**8.34**	**7.93**	**7.94**	**0.41**	**26.59**	1.29	1.39
4	Hold	Dec	Hold	241	**253**	225	**-8.26**	**-7.96**	**-8.06**	**0.30**	**25.70**	1.30	1.41
5	Hold	Hold	Inc	251	**181**	417	**10.4**	**8.69**	**-8.57**	**0.65**	**25.60**	1.19	1.38
6	Hold	Hold	Dec	243	**173**	225	**-8.09**	**-12.6**	**8.55**	**0.58**	**25.70**	1.30	1.41
7	Dis	Min	Dis	297	**271**	276	53.9	98.6	76.5	48.05	**24.93**	**1.02**	**1.09**
8	Dis	Max	Dis	501	**501**	414	214	230	239	24.78	**44.36**	**1.33**	**1.02**
9	Min	Min	Dis	473	**66**	46	-53.4	-431	-443	390	**33.46**	0.99	**3.52**
10	Dis	Min	Min	179	**147**	348	-294	100	331	356	**25.64**	**2.36**	1.21

Test	c(-1)	c(0)	c(1)	v_4	v_5	v_6	Δv_5	$(v_1+v_4)/ v_1$	$(v_2+v_5)/ v_2$	$(v_3+v_6)/ v_3$
0				-241	-174	-227	25.72	8.24	-5.65	-7.53
1	Inc	Hold	Hold	-235	-182	-235	**24.89**	**7.58**	**-5.21**	**-8.43**
2	Dec	Hold	Hold	-240	-174	-227	**25.69**	**8.34**	**-5.56**	**-7.43**
3	Hold	Inc	Hold	-249	-182	-235	**26.54**	**7.72**	**-5.68**	**-7.96**
4	Hold	Dec	Hold	-241	-174	-227	**25.69**	**8.29**	**-5.82**	**-7.73**
5	Hold	Hold	Inc	-249	-182	-219	**25.59**	**7.33**	**-6.02**	**-8.84**
6	Hold	Hold	Dec	-241	-174	-227	**25.69**	**7.59**	**-5.87**	**-7.88**
7	Dis	Min	Dis	-295	-272	-278	**24.88**	**5.05**	**-4.75**	**-8.19**
8	Dis	Max	Dis	-512	-504	-519	**26.94**	**-2.17**	**-4.92**	**-8.39**
9	Min	Min	Dis	-471	-49	-48	**36.85**	**3.83**	**-29.27**	**-25.97**
10	Dis	Min	Min	-177	-148	-351	**25.64**	**11.12**	**-6.19**	**-9.22**

Shaded cells indicate a pass/fail requirement

GROUP 2 – Impedance Requirements

Table 3 – Test Requirements and results

Parameter	Min	Max	Measured	Units	Figure
72.2.1 – Differential Output Return Loss					
The Differential Output Return Loss shall be greater than or equal to 9 for 50 MHz <= f < 2500 MHz, and greater than or equal to 9 – 12*$\log_{10}$(f / 2500MHz) for 2500 MHz <= f <= 7500 MHz. The measured value shows the minimum margin over the entire frequency range.	0	+Inf	1.9	dB	9
72.2.2 – Common-Mode Output Return Loss					
The Common-Mode Output Return Loss shall be greater than or equal to 6 for 50 MHz <= f < 2500 MHz, and greater than or equal to 6– 12*$\log_{10}$(f / 2500MHz) for 2500 MHz <= f <= 7500 MHz. The measured value shows the minimum margin over the entire frequency range.	0	+Inf	5.3	dB	9
72.2.3 – Differential Input Return Loss					
The Differential Input Return Loss shall be greater than or equal to 9 for 50 MHz <= f < 2500 MHz, and greater than or equal to 9 – 12*$\log_{10}$(f / 2500MHz) for 2500 MHz <= f <= 7500 MHz. The measured value shows the minimum margin over the entire frequency range.	0	+Inf	2.6	dB	9

Annex A – Supplemental figures

Figure 1: Rising and falling time histogram

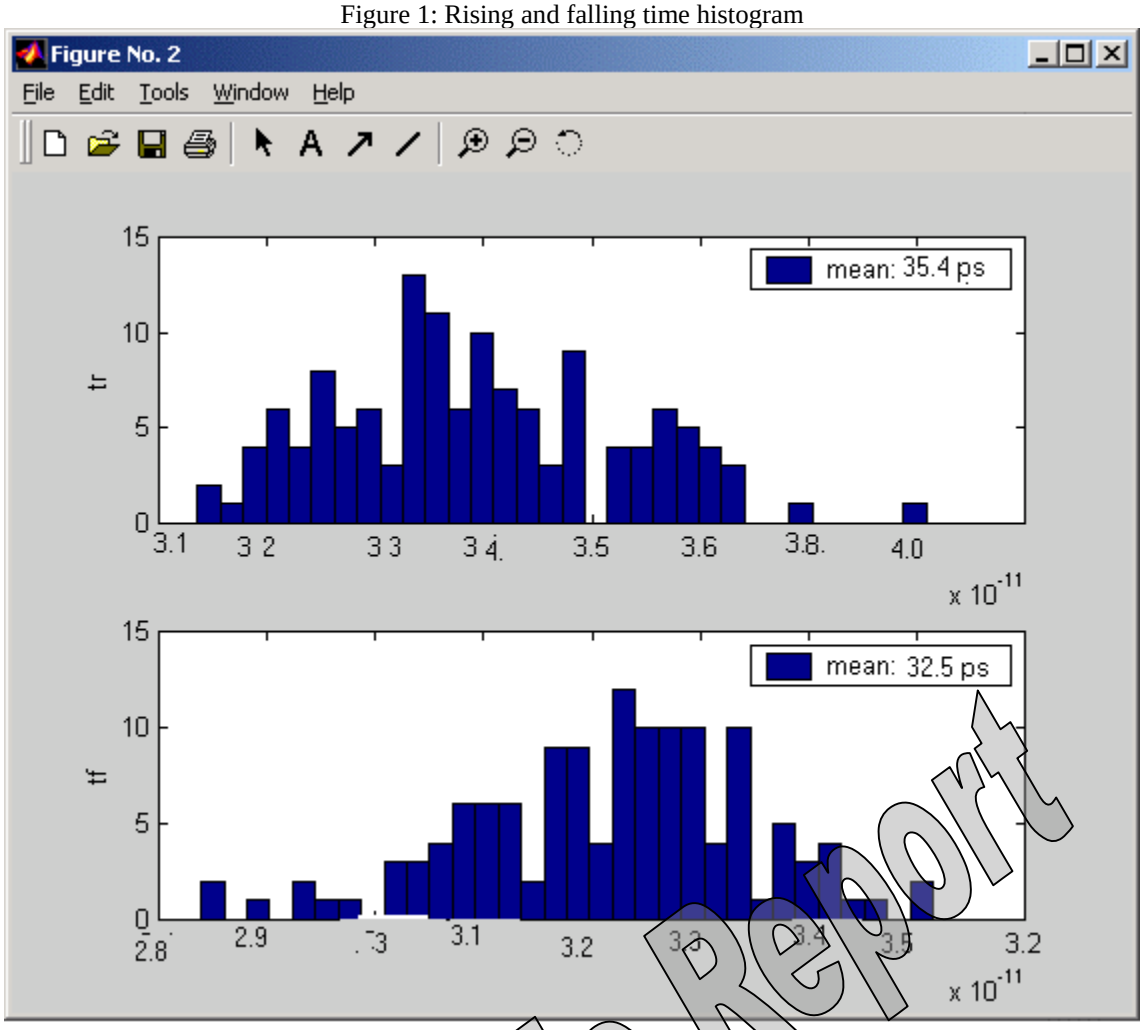

Figure 2: Sample rise/fall time measurement

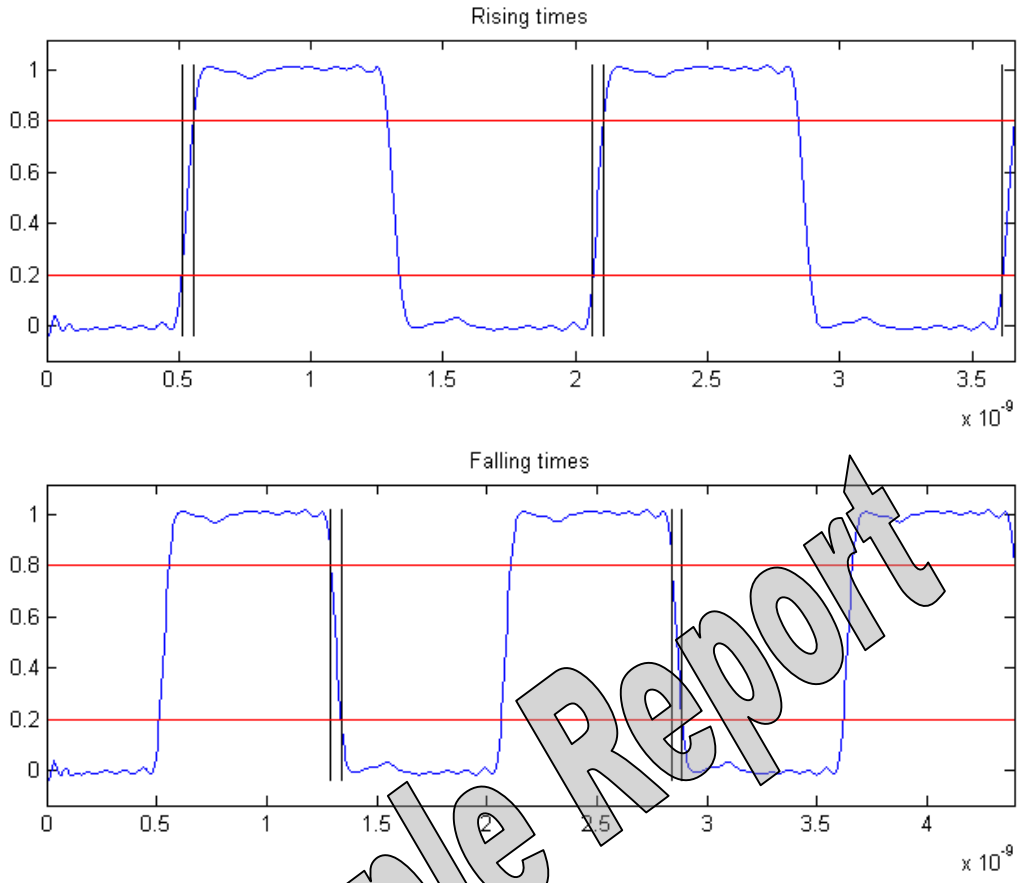

Figure 3: Jitter Statistics

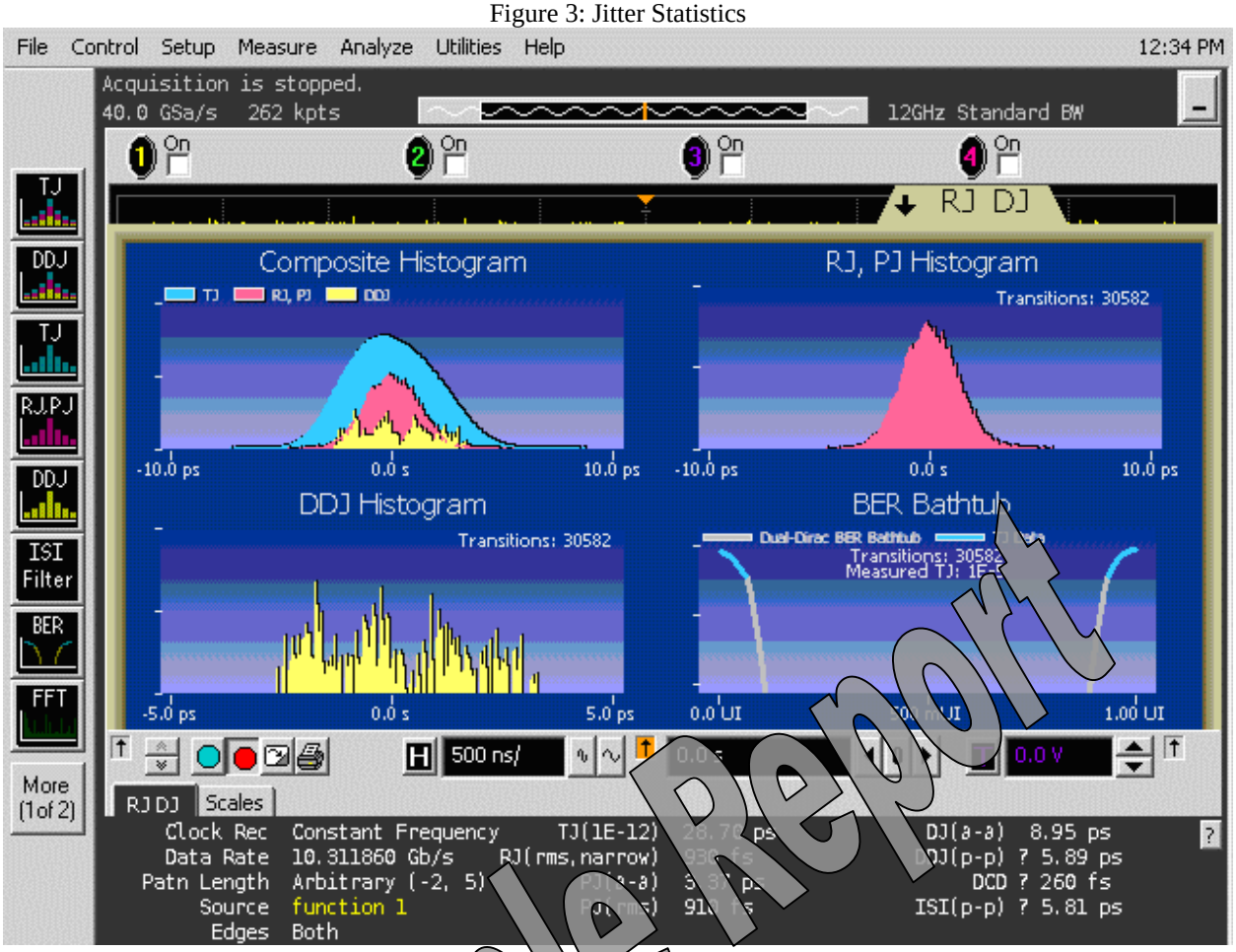

Figure 4: DCD vs. index

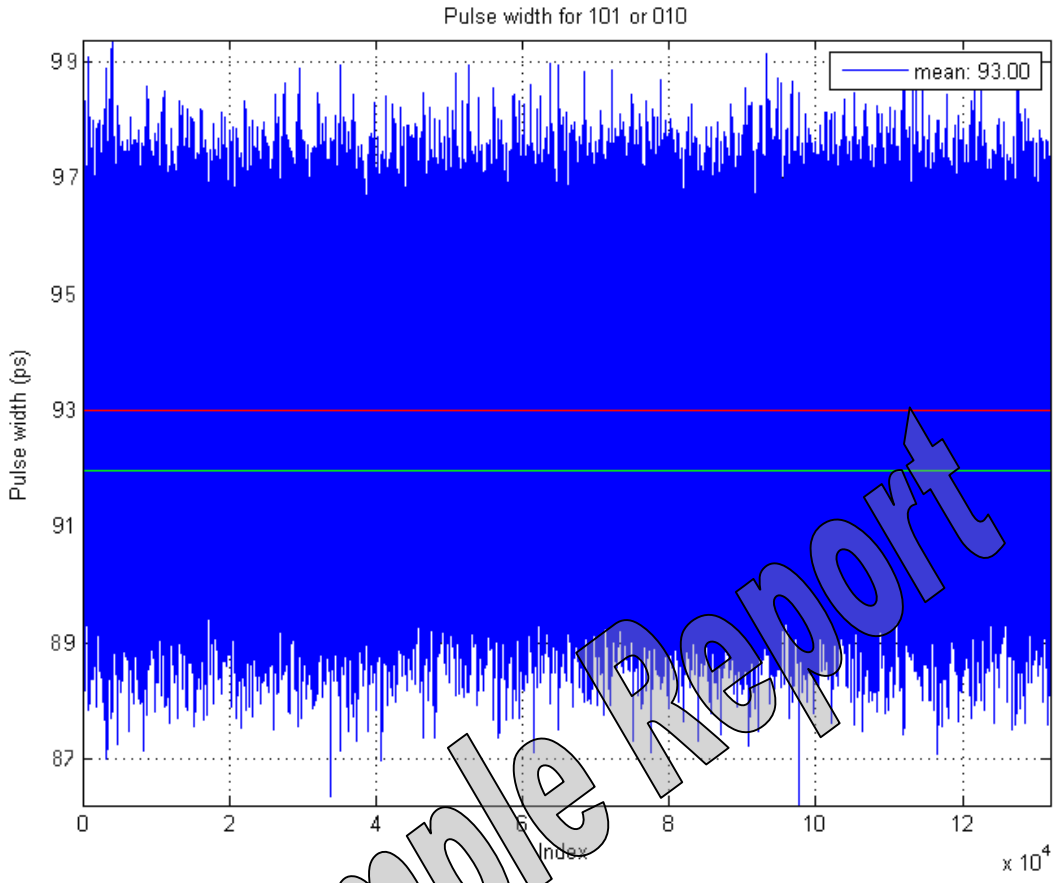

Figure 5: Sample Coefficient Waveform

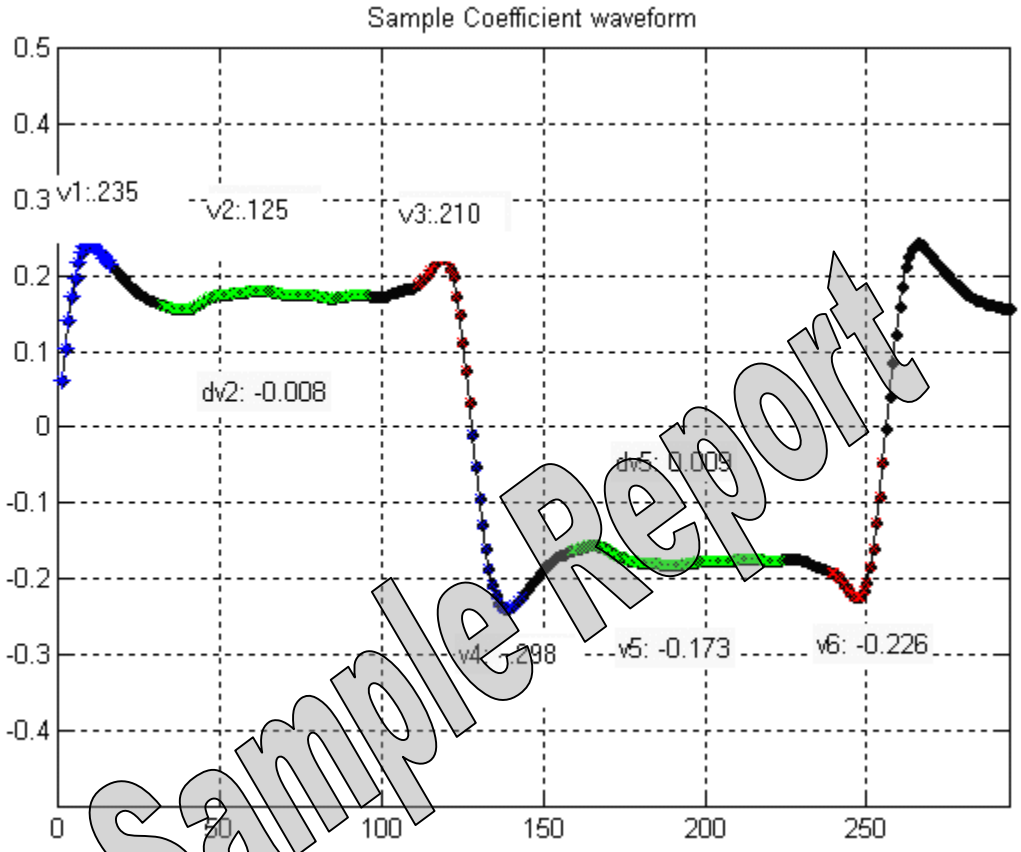

Figure 6: Coefficient statistics (1)

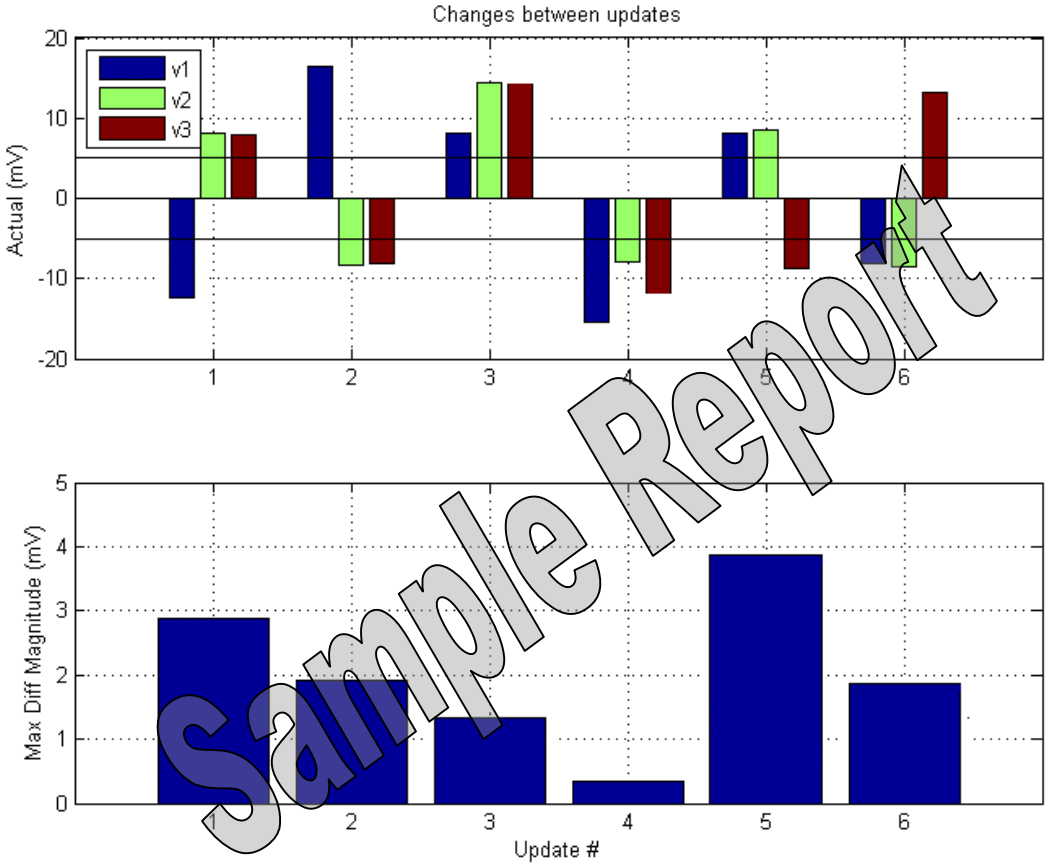

Figure 7: Coefficient statistics (2)

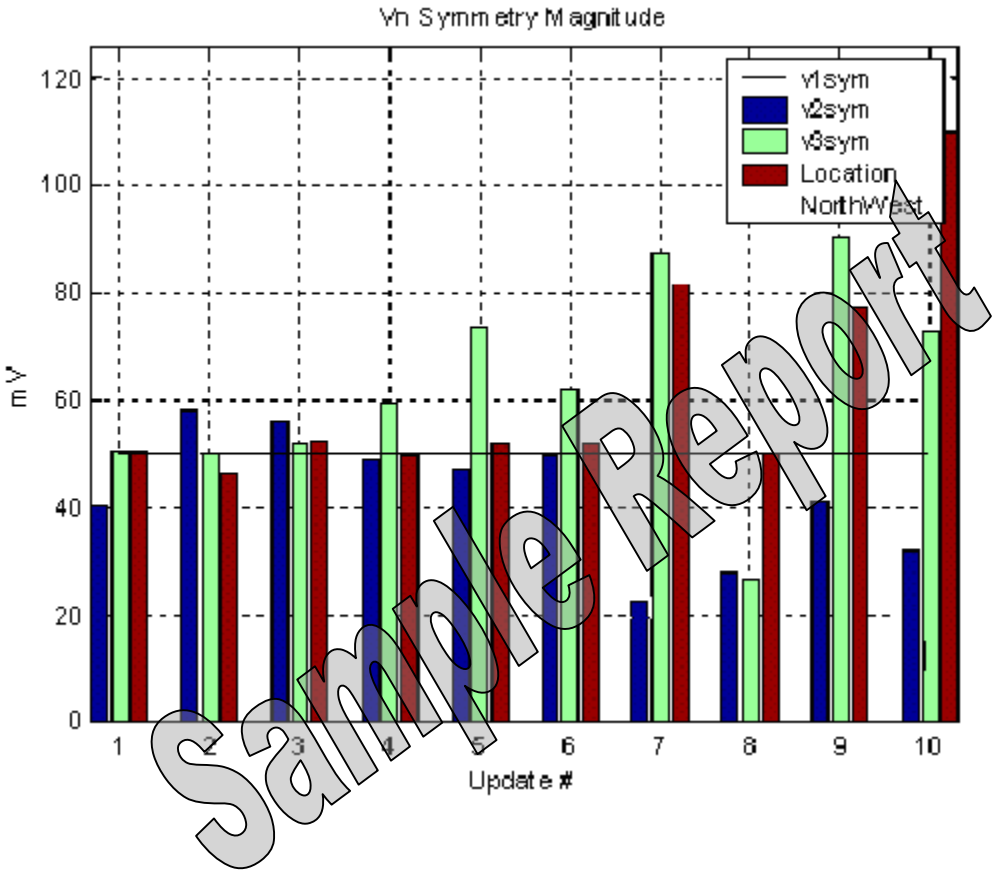

Figure 8: Coefficient statistics (3)

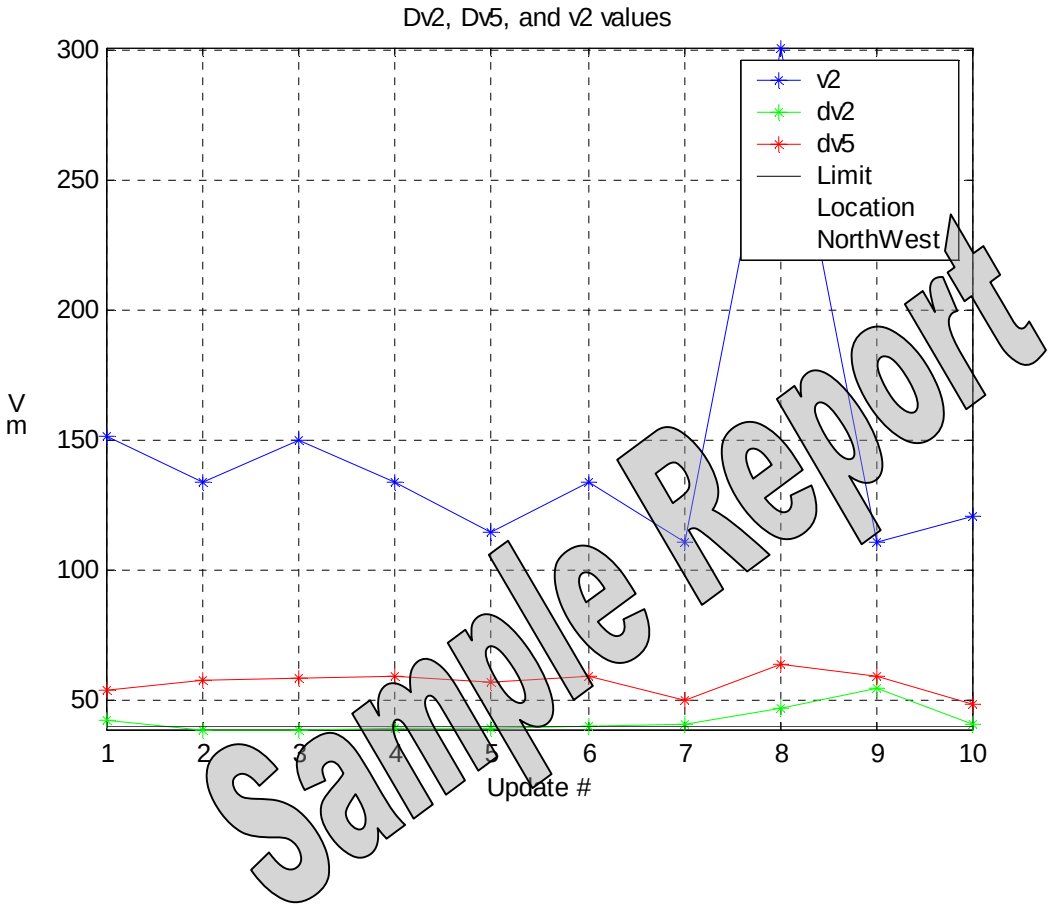

Figure 9: Return Loss