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Vendor X Company Name Street Address City, State, Zip August 21, 2005 Report Rev. 1.0

Enclosed are the results from the Clause 49 10GBASE-R PCS testing performed on:

Device Under Test (DUT):10 GiHardware Version:N/AFirmware Version:N/ASoftware Version:N/AMiscellaneous:Teste

10 Gigabit Ethernet Switch N/A N/A N/A Tested on port 1

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/10gec/testsuites/Clause\_49\_PCS\_Test\_Suite\_v0.4.pdf

**Issues Observed While Testing** 

Test 49.3.2: 64\_GOOD – The DUT was observed to improperly acquire block\_lock upon reception of only 63 consecutive valid sync headers.

Test 49.3.3: 16\_BAD – The DUT was observed to require 17 invalid sync headers in a group of 64 blocks to lose block\_lock.

For specific details regarding issues please see the corresponding test result.

Testing Completed 08/09/2005

John Q. Tester

John Q. Tester johnqtester@iol.unh.edu +1603-862-0205 Review Completed 08/10/2005

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#### **Result Key**

The following table contains possible results and their meanings

Result	Interpretation
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with	The DUT was observed to exhibit conformant behavior however an additional explanation of the
Comments	situation is included, such as flue to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Informative	Results are for informative purposes only and are not judged on a pass or fail basis.
Refer to	From the observations, a valid pass or fail could not be determined. An additional explanation of
Comments	the situation is included.
Not Applicable	The DUT does not support the technology required to perform these tests.
Not Available	Due to testing station or time limitations, the tests could not be performed.
<b>Border</b> line	The observed values of the specified parameters are valid at one extreme, and invalid at the other.
Not Tested	Not tested due to the time constraints of the test period.

## **Test Setup**

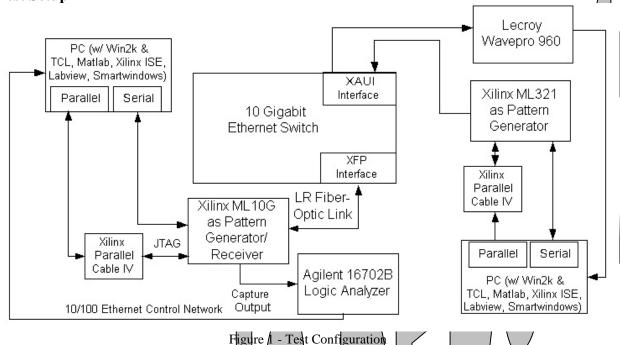


Figure 1 above depicts the test setup employed throughout the testing process. The XFP interface and the XAUI interfaces of the Device Under Test (DUT) were used to provide access to the DUT in all test cases. Control access to the DUT was provided via an Ethernet connection. The test system consists of 2 PCs, an Agilent 16702B, a Wavepro 960 DSO, a Xilinx MI 10G, and a Xilinx ML321.

# Xilinx ML10G system;

• 10GBASE-R signaling is generated by the "ML10G" Testing Station. This system continuously sends valid 10GBASE-R Idle when not instructed to send a programmable transmit pattern. When the transmit pattern is sent, the Logic Analyzer is set to trigger on non-Idle code-blocks.

Labview software controls the generation of the test vectors and programming of the ML10G. Labview software controls the downloading and analysis of the signaling captured on the Agilent 16702B.

• The AGBASE-R signaling from the DUT is captured by the ML10G and then relayed to the Agilent 16702B.

## Xilinx ML321 system

- XAUI signaling is generated by the Xilinx ML321" Testing Station. This system continuously sends valid (though not truly randomized) XAUI Idle when not instructed to send a programmable transmit pattern. When the transmit pattern is sent, a trigger signal is sent to the DSO to capture the response of the DUT.
- Labyiew software controls the generation of the test vectors and programming of the ML321. Labview and Matlab software control the downloading and analysis of the signaling captured on the Lecroy WavePro 960.
- The 4-channel XAUI signaling from the DUT is captured single-endedly on a Lecroy WavePro 960. The positive signals (Tx+) are driven into the 500hm terminations of the DSO, while the negative signals (Tx-) are terminated with 500hm terminations.

The PCs are used for five purposes:

- •/ via the network to control the DSO and download and process the waveforms in Matlab
- via the network to control the Logic Analyzer and download and process the captures signals in Labview
- via an Ethernet connection to control the DUT
- via the parallel ports to download the firmware for the Xilinx ML321 and Xilinx ML10G
- via the Serial ports to control transmissions from the Xilinx ML321 and Xilinx ML10G

#### Section1: Detailed Table of Results GROUP 1: Scrambler/Descrambler and Bit Ordering

GROUP 1: Scrambler/Descrambler and Bit Ordering		
Test # and Label	Part(s)	<b>Result</b> (s)
Test 49.1.1: Transmit Scrambler	а	PASS
Comments on Test Procedure		
Purpose: To verify the transmit scrambler polynomial.		
Procedure: a. The Testing station is set up to capture and analyze a bit str defined scrambler polynomial.	ream from the DUT.	The DUT should use the
Comments on Test Results		
a. The DUT was observed to properly use the defined scrambler	polynomial.	
Test # and Label	<b>Dowt</b> (g)	Result(s)
Test # and Laber Test 49.1.2: Receive Descrambler	Part(s)	PASS
Comments on Test Procedure	a-0	1450
Purpose: To verify the receive descrambler polynomial.		
<ul> <li>Procedure:</li> <li>a. The DUT is sent validly scrambled data. Management incorposerved. The DUT should be able to lock on to and recover</li> <li>b. The DUT is sent invalidly scrambled data that is otherwise van from the DUT are observed. The DUT should not be able to lock on the data that is otherwise van from the DUT are observed. The DUT should not be able to lock on the data that is otherwise van from the dat</li></ul>	validly scrambled data lid. Management indic	cations and transmissions
Comments on Test Results		
a The DUT was observed to properly lock on to and recover va b. The DUT was observed to properly not lock on to and recover	lidly scrambled data, r invalidly scrambled d	lata.
		$\mathbf{D}_{a}$ and $\mathbf{I}_{a}$
Test # and Label	Part(s)	Result(s)
Test 49.1.3: Transmit bit ordening /	a	PASS
Comments on Test Procedure Purpose: To verify the transmit bit ordering. Procedure: a. The Testing station is set up to capture and analyze a bit strea should match with Figures 49-2 and 49-5.	m from the DUT. The	bit ordering of the DUT
Comments on Test Results		
a. The DUT was observed to utilize the proper bit ordering.		

Test # and I abol	<b>Dout</b> (g)	
Test # and Label       Test 49.1.4: Receive bit ordering	Part(s) a	Result(s) PASS
Comments on Test Procedure	a	1 400
Purpose: To verify the receive bit ordering. Procedure:		
<ul><li>a. The DUT is sent a bit stream with the proper bit ordering. The DUT data with the correct bit ordering.</li><li>b. The DUT is sent a bit stream with an improper bit ordering. The D recover data with an incorrect bit ordering.</li></ul>		
Comments on Test Results	<b>\</b>	
a. The DUT was observed to properly lock on to and recover data with b. The DUT was observed to properly not lock on to and recover data		
COMPLEX		

## GROUP 2: Coding Rules

GROUP 2: Coding F	<b>Xuics</b>							
Test # and Label						Part(s	5)	Result(s)
Test 49.2.1: 64B/66B	Transmitter	Block En	coder			a		PASS
Comments on Test <b>F</b>	Procedure						•	
Purpose: To verify that	at the DUT of	can proper	ly transmi	t and enco	de valid 6	6-bit bloc	eks.	
Purpose: a. The DUT is instr $D_0D_1D_2D_3/I$ $C_0C_1C_2C_3/C$ $C_0C_1C_2C_3/C$ $C_0C_1C_2C_3/S$	$D_4D_5D_6D_7$ $b_4C_5C_6C_7$ $D_4D_5D_6D_7$	$\frac{O_0D_1D_2D}{O_0D_1D_2D}$ $\frac{O_0D_1D_2D}{S_0D_1D_2D}$ $\frac{O_0D_1D_2D}{O_0D_1D_2D}$	0 <sub>3</sub> /S <sub>4</sub> D <sub>5</sub> D <sub>6</sub> I 0 <sub>3</sub> /O <sub>4</sub> D <sub>5</sub> D <sub>6</sub> I <sub>3</sub> /D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> I	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\frac{C_2C_3}{C_4C_5}$ $\frac{C_2C_3}{C_4C_5}$ $\frac{C_2C_3}{C_4C_5}$ $\frac{C_2C_3}{C_4C_5}$ $\frac{C_2C_3}{C_4C_5}$	$\begin{array}{c c} C_6 C_7 & I \\ C_6 C_7 & I \end{array}$	$D_0 \overline{D}_1 \overline{D}_2 $ $D_0 \overline{D}_1 \overline{D}_2 $	$D_{3}/T_{4}C_{5}C_{6}C_{7}$ $D_{3}/D_{4}T_{7}C_{6}C_{7}$ $D_{4}/D_{4}D_{5}T_{6}C_{7}$ $D_{3}/D_{4}D_{5}D_{6}T_{7}$
The DUT should prop b. The DUT is instr					ks:	$\left  \right\rangle$		
Sync	Block type			$C_2$ $C_3$		¢5	C <sub>6</sub>	
10	0x1E	0x00		0x33  0x			0x78	
10	0x1E	0x1E	0x1E	TRIE Ox	$1E \mid 0x/E$	0x1E	0x1E	0x1E
c. The DUT is instr Sync 10 10 10 The DUT should prop	Block type 0x55 0x55 0x55 0x55	e D <sub>1</sub> 0x00 0x00 0x00	D2 0x00 0x00 0x00	$\begin{array}{c c} \hline O_{\beta} & O_{1} \\ \hline O_{x}01 & O_{x} \\ \hline O_{x}01 & O_{x} \\ \hline O_{x}00 & O_{x} \\ \hline \end{array}$	0 04 0 0x0 0 0xF F 0xF	D <sub>5</sub> 0x00 0x00 0x00	$ \begin{array}{c c} D_6 \\ \hline 0x00 \\ 0x00 \\ 0x00 \\ \hline 0x00 \\ \hline \end{array} $	$\begin{array}{c} D_7\\ 0x01\\ 0x01\\ 0x0\\ 0x0\\ \end{array}$
Comments on Test H	Results			, ,	R			
a. The DUT was ob The DUT was ob The DUT was ob	served to pr served to pr	operly/en operly en	code and t code and t	rapsmit all	valid con	trol codes	5.	

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DUT: 10 Gigabit Ethernet Swi	itch	
Test # and Label	Part(s)	Result(s)
Test 49.2.2: 64B/66B Transmitter Invalid Block Handling	a	PASS
Comments on Test Procedure	• •	
Purpose: To verify that the DUT does not transmit invalid blocks or con	trol codes.	
Procedure: a. The DUT is instructed to transmit one of the following blocks: $ \frac{C_0C_1C_2C_3/D_4D_5D_6D_7}{T_0C_1C_2C_3/T_4C_5C_6C_7} \frac{D_0D_1D_2D_3/S_4D_5D_6}{T_0C_1C_2C_3/D_4D_5D_6D_7} \frac{T_0C_1C_2C_3/Q_4D_5D_6}{T_0C_1C_2C_3/Q_4D_5D_6D_7} \frac{T_0C_1C_2C_3/Q_4D_5D_6}{T_0C_1C_2C_3/T_4C_5C_6C_7} \frac{S_0D_1D_2D_3/Q_4D_5D_6D_7}{S_0D_1D_2D_3/S_4D_5D_6D_7} $ The DUT should encode all invalid blocks as errors.	$D_7  S_0 D_1 D_2 D_3 / C_2$	$_4C_5C_6C_7$
Comments on Test Results		
a. The DUT was observed to properly encode all invalid blocks as erro	ors.	

τ	University of N D	lew Hampshin UT: 10 Gigab			aboratory	
Fest # and LabelIest 49.2.3: 64B/66B Received	er Block Deco	ding and Con	trol Code I	Aapping	Part(s) a-c	Result(s) PASS
Comments on Test Procedu	re				<b>I</b>	1100
Purpose: To verify that the D	UT can proper	ly receive and	l decode va	alid 66-bit b	olocks.	
Procedure:						$\cap$
a. The testing station is inst	ructed to trans	mit one of the	e following	blocks to t	he DUT:	
			maaa			
$\frac{D_0D_1D_2D_3/D_4D_5D_6}{C_0C_1C_2C_3/C_4C_5C_6C}$		$_{3}/S_{4}D_{5}D_{6}D_{7}$ $_{3}/O_{4}D_{5}D_{6}D_{7}$		$\frac{\sqrt{C_4C_5C_6C_7}}{\sqrt{C_4C_5C_6C_7}}$		$\sqrt{T_4 \mathcal{Q}_5 C_6 C_7}$
$C_0C_1C_2C_3/O_4D_5D_6I$		$_{3}/_{0_{4}}D_{5}D_{6}D_{7}$		$\frac{\sqrt{C_4C_5C_6C_7}}{\sqrt{C_4C_5C_6C_7}}$		$\frac{1}{2} \frac{D_4 T_5 C_6 C_7}{D_4 D_5 T_6 C_7}$
$C_0C_1C_2C_3/S_4D_5D_6D_6$		$_{3}/C_{4}C_{5}C_{6}C_{7}$		$_{3}/C_{4}C_{5}C_{6}C_{7}$		$_{3}/D_{4}D_{6}D_{6}T_{7}$
The DUT should properly rec	eive and deco	de all valid 60	5-bit block		1	
The testing station is inst					he DUT: A	
Corres Direct		0 0				
Sync Block 10 0x1E	type $C_0$ 0x00	$C_1$ $C_2$ 0x2D $0x3$	$\begin{array}{c c} C_3 \\ \hline 3 & 0x4B \end{array}$	$C_4$ C 0x55 02	$\begin{array}{c c} & C_6 \\ \hline \\ 66 & 0x78 \\ \hline \end{array}$	$O_{\mathbf{x}}O0$
10 0x1E	0x1E	Ox1E Ox1				Dx1E
		c.				
The DUT should properly rec I. The testing station is inst					he DUT:	
Sync Block		$\begin{array}{c c} D_2 & D_3 \\ \hline 0x00 & 0x0 \end{array}$	$O_1$	$O_4   D$	$5 \int D_6$	$D_7$
10 0x55 10 0x55	0x00	0x00/ /0x0 0x00 /0x0			$\frac{00}{00}$ $\frac{000}{000}$	0x01 0x01
10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x00					0x01
The DUT should properly rec	eive and deco		codes.		7	
Comments on Test Results						
			1	V		
The DUT was observed	o properly de	code and rece	ive all vali	d 66-bit blo	cks.	
. The DUT was observed . The DUT was observed	1	1	ve all vali	d control co	des.	
				i O coues.		
/						
c. Tine Do T was observed						
$\backslash$ /						
$\checkmark$						

University of New Hampshire – InterOperability Laboratory DUT: 10 Gigabit Ethernet Switch

Test # and Label	_ Part(s)	Result(s)
Test 49.2.4: 64B/66B Receiver Invalid Code Handling	a - d	PASS
	e	Not Tested
Comments on Test Procedure		
<ul> <li>Purpose: To verify that the DUT properly handles the reception of invalue Procedure:</li> <li>a. The testing station is instructed to transmit a frame with one data bloc The DUT should replace the received blocks with EBLOCK_R&lt;71:</li> <li>b. The testing station is instructed to transmit otherwise valid idle block replaced with a reserved block type field. The DUT should replace the EBLOCK_R&lt;71:0&gt;.</li> <li>c. The testing station is instructed to transmit otherwise valid control b replaced with a reserved control field. The DUT should replace the EBLOCK_R&lt;71:0&gt;.</li> <li>d. Instruct the testing station to transmit continuous sequence ordered_code of 0x0, and indicating remote fault. The DUT should replace the EBLOCK_R&lt;71:0&gt;, and should not indicate reception of remote fault have a value of 0x0.</li> <li>e. Instruct the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the testing station to transmit a block containing one of the form the</li></ul>	bock containing a 0>, and should is ks with the 0x11 the received blocks blocks with the contract of the second blocks sets to the DUT he received blocks in the received blocks 1 when r	in invalid sync header, not receive the frame. E block type field ocks with control code fields with , using a 10GBASE-R O cks with ng O codes that do not lings: $(O_4D_5D_6D_7)$
<ul> <li>Comments on Test Results</li> <li>a. The DUT was observed to properly replace the received blocks with "fast 66B frame sync" the DUT was observed to transmit LF in resp The DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks with the DUT was observed to properly replace the received blocks.</li> </ul>	onse to the inva EBLOCKs EBLOCKs BLOCKs with EBLOCKs	ılid sync header.
Test # and Label	Part(s)	Result(s)
Test 49.2 5/ Id/e Control Code Insertion/Deletion	a	Not Performed
Comments on Test Procedure Purpose: To verify that the DUT properly inserts and delete idle Idle control characters (/I/) are transmitted when idle control characters characters may be added or deleted by the PCS to adapt between clock ra in groups of 4//I/s may be added following idle or ordered sets. The received. When deleting /I/s, the first four characters after a /T/ shall not <b>Comments on Test Results</b>	ates. /I/ insertio by shall not be a	n and deletion shall occur
This test is still under development and was not performed.		

Test # and Label	Part(s)	Result(s)
Test 49.2.6: Sequence Ordered_set deletion	a	Not Performed
Comments on Test Procedure	• •	
Purpose: To verify that the DUT properly deletes ordered_sets. Sequence ordered_sets may be deleted by the PCS to adapt between cl when two consecutive sequence ordered sets have been received, and deleted.		
This test is still under development and was not performed.		

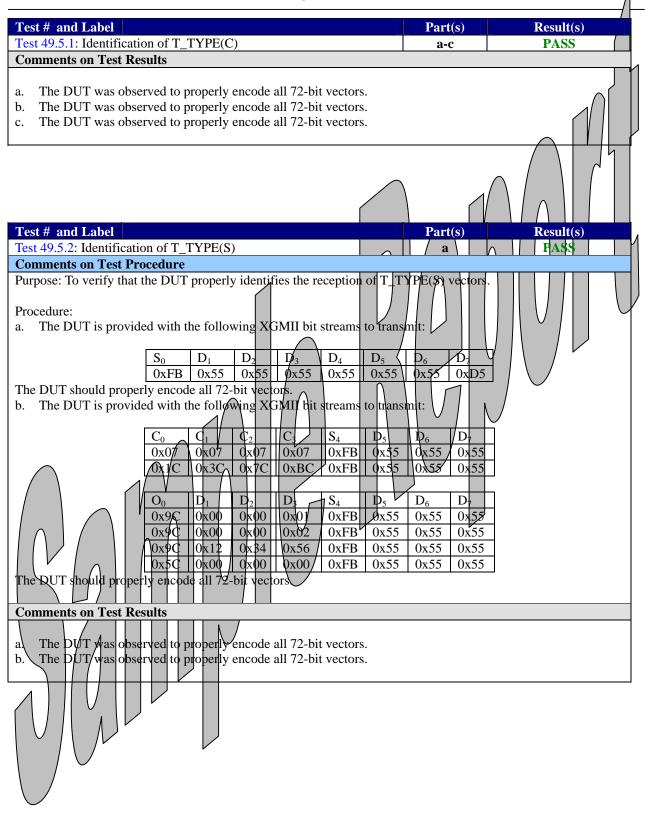
#### GROUP 3: Lock State Machine

Test # and Label	Part(s)	Result(s)
Test 49.3.1: Identification of sync header	a-b	PASS
Comments on Test Procedure	. <b>1 1</b>	
Purpose: To verify that the DUT properly identifies valid and invalid syn Procedure:	ic headers.	
a. The testing station is instructed to transmit a continuous stream of b.	locks with a syn	header of either '01' or
"10". The DUT should achieve block_lock while receiving an incom		
or '10'.	۱.	$\land$ / $\land$ / $\land$
b. The testing station is instructed to transmit a continuous stream of b	locks with a synd	c header of either '00' dr
'11'. The DUT should not achieve block_lock while receiving an ir	coming bit strea	m with sync headers of
'00' or '11'.		
Comments on Test Results		
a. The DUT was observed to properly achieve block_lock while rece	iving a continuo	us stream of blocks with
sync headers of '01' or '10'.		
b. The DUT was observed to properly not achieve block_lock while	receiving a con	tinuous stream of blocks
with sync headers of '00' or '11'.		
Test # and Label	Part(s)	Result(s)
Test 49.3.2: 64 GOOD	$\nabla_{a}$	FAIL
Comments on Test Procedure		-
Purpose: To verify that the DUT needs to see 64 consecutive valid sync 1	headers before a	chieving block_lock.
Procedure:	hand an faile	
a. The testing station is instructed to transmit $n$ blocks with a valid sinvalid sync header. The value of $n$ is increased until the DUT is obtained.		
should achieve block after receiving a continuous looping pattern of	f 64 or more vali	d sync headers, followed
by a single invalid sync header.		
Comments on Test Results		
a. The DUT was observed to improperly achieve block_lock after rece	iving a continuo	us looping pottern of 62
blocks with a valid sync header followed by one block with an inval		
not achieve block_lock after receiving a continuous looping pattern		
followed by one block with an invalid sync header.		

Test # and Label	Part(s)	Result(s)
Test 49.3.3: 16_BAD	а	FAIL
Comments on Test Procedure		
Purpose: To verify that the DUT needs to see 16 out of 64 invalid sync h Procedure:		
a. The testing station is instructed to transmit a set of 64 blocks conta The value of <i>n</i> is increased until the DUT is observed to lose block after receiving 16 invalid sync headers out of a group of 64 sync head	_lock. The DU	
Comments on Test Results		
a. The DUT was observed to improperly maintain block_lock upon a group of 64 blocks. The DUT was observed to lose block_lock upon a group of 64 blocks.		
CONDE		

# **GROUP 4: BER Monitor State Machine** Test # and Label **Result(s)** Part(s) Test 49.4.1: Value of 125us\_timer Not Performed a **Comments on Test Procedure** Purpose: To verify that the value of the 125us timer is between 93.75µs and 126.25µs. The 125us\_timer described in Figure 49-13 must take on a value of $125\mu + 1\%$ , -25%. The timer is used to a. set the hi\_ber flag if more than 16 invalid sync headers are found within the window of $123\mu$ s. The DUT is instructed to send 15 invalid sync headers to the DUT. The transmit station is then instructed to send 1 invalid sync header a specific amount of time later. Indications and transmissions from the DUT are observed. The DUT should set the high\_ber flag if it receives 16 invalid sync headers within 93.75 µs to 126.25µs **Comments on Test Results** This test is still under development and was not performed.

Test # and Label         Part(s)         Result(s)           Test 49.5.1: Identification of T_TYPE(C)         a-c         PASS           Comments on Test Procedure         Purpose: To verify that the DUT properly identifies the reception of T_TYPE(C) vectors.         Procedure:           a.         The DUT is provided with the following XGMII bit streams to transmit:         Image: Comments on the following XGMII bit streams to transmit:           The DUT should properly encode all 72-bit vectors.         Image: Comments on the following XGMII bit streams to transmit:         Image: Comments on the following XGMII bit streams to transmit:           The DUT should properly encode all 72-bit vectors.         Image: Comments on transmit:         Image: Comments on transmit:           Comments on the following XGMII bit streams to transmit:         Image: Comments on transmit:         Image: Comments on transmit:           Comments on the following XGMII bit streams to transmit:         Image: Comments on transmit:         Image: Comments on transmit:           Comments on the following XGMII bit streams to transmit:         Image: Comments on transmit:         Image: Comments on transmit:           Comments on transmit:         Image: Comments on transmit:         Image: Comments on transmit:         Image: Comments on transmit:           Comments on transmit:         Image: Comments on transmit:         Image: Comments on transmit:         Image: Comments on transmit:           Comments on transmit	GROUP 5: Transmit S	tate Ma	chine								/
Test 49.1: Identification of T_TYPE(C)         a-c         PAS           Comments on Test Procedure         Propose: To verify that the DUT properly identifies the reception of T_TYPE(C) vectors.           Purpose: To verify that the DUT properly identifies the reception of T_TYPE(C) vectors.         Image: Commentation of C_TYPE(C) vectors.           Purpose: To verify that the following XGMII bit streams to transmit:         Image: Commentation of C_TYPE(C) vectors.         Image: Commentation of C_TYPE(C) vectors.           The DUT should properly encode all 72-bit vectors.         Image: Commentation of Commentation of C_TYPE(C) vectors.         Image: Commentation of Commentatio Commentation of Commentation of Commentation of Co								Part	(s)	Result	(s)
Comments on Test Procedure Purpose: To verify that the DUT properly identifies the reception of T_TYPE(C) vectors. Procedure: a. The DUT is provided with the following XGMII bit streams to transmit: $ \frac{C_{01}}{0.07} \frac{C_1}{0.007} \frac{C_2}{0.007} \frac{C_3}{0.007} \frac{C_4}{0.007} \frac{C_5}{0.007} \frac{C_6}{0.007} \frac{C_7}{0.007} \frac{C_6}{0.007} \frac{C_6}{0.000} C_$		on of T	TYPE(C	<u></u>							
Purpose: To verify that the DUT properly identifies the reception of T_TYPE(C) vectors. Procedure: a. The DUT is provided with the following XGMII bit streams to transmit: $ \frac{C_0}{0x10} \frac{C_1}{0x07} \frac{C_2}{0x07} \frac{C_3}{0x07} \frac{C_4}{0x07} \frac{C_5}{0x00} \frac{C_6}{0x07} \frac{C_7}{0x07} $ The DUT should properly encode all 72-bit vectors. b. The DUT is provided with the following XGMII bit streams to transmit: $ \frac{C_0}{0x07} \frac{C_1}{0x07} \frac{C_2}{0x07} \frac{C_2}{0x07} \frac{C_4}{0x07} \frac{C_5}{0x00} \frac{C_6}{0x07} \frac{C_6}{0x07} $ The DUT should properly encode all 72-bit vectors. b. The DUT is provided with the following XGMII bit streams to transmit: $ \frac{C_0}{0x07} \frac{C_1}{0x07} \frac{C_2}{0x07} \frac{C_2}{0x07} \frac{C_2}{0x07} \frac{C_2}{0x00} \frac{C_2}{0x$				/			Į_		Į_		
Procedure: <ul> <li>The DUT is provided with the following XGMII bit streams to transmit: <ul> <li></li></ul></li></ul>			properl	y identif	fies the re	eception	of T_TY	PE(C)	vectors.		
a. The DUT is provided with the following XGMII bit streams to transmit:	1 5		1 1			1	_				
$\frac{\left[\frac{1}{0,07},\frac{1}{$	Procedure:									[	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	a. The DUT is provide	ed with t	he follo	wing XO	GMII bit	streams	to transr	nit:		$\frown$	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			1	1	1	1	-	1	1	, / \	14
0x1C $0x3C$ $0x7C$ $0xBC$ $0x07$ $0x07$ $0x07$ The DUT should properly encode all 72-bit vectors.       .					-						$\cap$
The DUT should properly encode all 72-bit vectors. b. The DUT is provided with the following XGMII bit streams to transmit: $ \frac{C_{0}}{0x07} \frac{C_{1}}{0x07} \frac{C_{2}}{0x07} \frac{C_{3}}{0x07} \frac{D_{4}}{0x97} \frac{D_{5}}{0x00} \frac{D_{5}}{0x0$									. /	1 \ / \	
b.       The DUT is provided with the following XGMII bit streams to transmit:						0xDC	0xF7	0x07	0x07/		
$\frac{\left[ \begin{array}{c} 0 \\ 0x07 \\ $							4.5. 4.4.5.4.5.4				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	b. The DUT is provide	ed with t	ne tollo	wing X	JMII Dit	streams	to transr		$\setminus$		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		C	C	C	C		ы			$\lambda \mid l \mid l \mid l \mid l$	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$											
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$											
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		-									
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$										$      \vee   $	
$\frac{0_{0}}{0x9C} \frac{0}{0x00} \frac{0}{0x00} \frac{0}{0x01} \frac{0}{0x07} \frac{0}{$										1   \ /	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		01107	01107	0		0.10 0				,   \ , '	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		<b>O</b> <sub>0</sub>	$D_1$	$D_2$	$\mathbb{D}_3$	$C_{4}$	C <sub>5</sub>	C <sub>6</sub>	C	1/ /	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			-						-		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$										1/	
0x9C $0x00$ $0x00$ $0x1C$ $0x3C$ $0x07$		0x9C								V	
The DUT should proper 6 ercode all 72-bit vectors. The DUT is provided with the following XGMU bit streams to transprit: $0_0 \land D_1 D_2 D_3 O_4 D_5 D_6 D_1 D_2 D_2 D_2 D_2 D_2 D_2 D_2 D_2 D_2 D_2$		0x9C	0x0Ø					0x7C			
c. The DUT is provided with the following XGMIP bit streams to transpir: $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0x5C	0x00	0x00	0x01	0x07	0x07	0x07	0x07		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	The DUT should proper	ly encod	le all 7A	-bit vect	ors.			$\nabla$		-	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	c. / The DUT is provid	d with t	he follo	wing X	GML bit	streams	to transr	nit:			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $						1		1		7	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $			-	2			/			-	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$							-			-	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$					1 1 1		-			-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $					<u> </u>		-			-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $										-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $							-				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $					1		-		1		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				V	1		-			-	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$							-			-	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			/				-			-	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$							-			-	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$							-			-	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$					1		-			-	
The DUT should properly encode all 72-bit vectors. $0x00 0x00 0x00 0x00 0x00$							-		1	-	
The DUT should properly encode all 72-bit vectors.					1		-		1	-	
	The DUT should proper					UNDE	0400	0/100	0.00	1	
<continued next="" on="" page=""></continued>		iy encot	uii 72								
<continued next="" on="" page=""></continued>	$\smile$										
<continued next="" on="" page=""></continued>											
<continued next="" on="" page=""></continued>											
communed on heat pages	<continued next="" on="" pag<="" td=""><td><i>e&gt;</i></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></continued>	<i>e&gt;</i>									



DUT: 10 Gigabit Ethernet		
Test # and Label	Part(s)	Result(s)
Test 49.5.3: Identification of T_TYPE(T)	a	PASS
Comments on Test Procedure		
Purpose: To verify that the DUT properly identifies the reception of	T_TYPE(T) vectors.	J
<ul> <li>Procedure:</li> <li>1. The DUT is instructed to transmit the first of the following 72-to 0x07 for all control characters:</li> </ul>	bit vectors to the testing	g station, and using
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\frac{{}_{3}/T_{4}C_{5}C_{6}C_{7}}{{}_{2}/D_{4}T_{5}C_{6}C_{7}}$ $\frac{{}_{3}/D_{4}D_{5}T_{6}C_{7}}{{}_{3}/D_{4}D_{5}D_{6}T_{7}}$	
Comments on Test Results		
a. The DUT was observed to properly encode all 72-bit vectors.		
Test # and Label	Part(s)	Result(s)
Test 49.5.4: Identification of T_TYPE(D)	a	ASS
Purpose: To verify that the DUT properly identifies the reception of Procedure: a. The DUT is instructed to transmit all valid 72-bit data blocks.		/ perly encode all 72-bit
Comments on Test Results		
a. The DUT was observed to properly encode all 72-bit vectors.		

	Oniversity o	DUT: 10 Giga		1	ility Labora ch	llory	/
Test # and Label					Part(s)		Result(s)
Test 49.5.5: Identificatio	on of T TYPE(E	)			a a a		PASS
<b>Comments on Test Pro</b>		/		I		<b>I</b>	
Purpose: To verify that t	he DUT properly	y identifies the	reception	of T_TY	YPE(E) vec	tors.	
Procedure: a. The DUT is provide The DUT should proper.	C_0       C_1 $0x07$ $0xFE$ $0x07$ $0xFE$ $0x07$ $0x red 0x17 $	wing XGMII bit $C_2$ $C_3$ $0x07$	$\begin{array}{c} C_4 \\ 0x07 \\ 0x07 \\ 0x07 \\ 0x07 \\ 0xFE \\ 0x07 \\ 0x0$	0 transr 0x07 0x07 0x7 0x7 0x07 0x07 0x07 0x07 0x07	nit: C <sub>6</sub> C 0x07 02 0xFE 02 0x07 02		
Comments on Test Res	sults		<u> </u>				
a. The DUT was obser	rved to properly	encode all/72-b	it vectors	as T_B		PE(Ĕ).	
Test # and Label					Part(s)		Result(s)
Test 49.5.6: TX_INIT st	ate /				a		Not Tested
<b>Comments on Test Pro</b>							
Purpose To verify that Procedure: a. The DUT is instruct Comments on Test Res	ed to reset. Wh	en being reset, t	he DUT s			v transmit	local fault blocks.
a. This test was not pe	auring	ine testing perio	Ju.				
		)					

Test # and Label	Part(s)	Result(s)
Test 49.5.7: TX_C state	a-c	PASS
Comments on Test Procedure		
Purpose: To verify that the DUT properly behaves while in the TX_C sta	te.	
<ul> <li>Procedure:</li> <li>a. The DUT is instructed to transmit continuous control blocks such that should properly encode all 72-bit vectors and remain in the TX_C st</li> <li>b. The DUT is instructed to transmit an S control character while in the encode all 72-bit vectors and transition to the TX_D state while transc.</li> <li>c. The DUT is instructed to transmit an S control character while in the transmitting both D and T blocks. The DUT should properly encode TX_E state when transmitting E, D, or T blocks.</li> </ul>	ate while transm TX_C state. T smitting an S bl TX_C state. T	nitting C blocks The DUT should property lock. Mis is repeated
Comments on Test Results		
<ul> <li>a. The DUT was observed to properly remain in the TX_C state.</li> <li>b. The DUT was observed to properly transition to the TX_D state.</li> <li>c. The DUT was observed to properly transition to the TX_E state.</li> </ul>		
Test # and Label	Part(s)	Result(s)
Test 49.5.8: TX D state	are 1	PASS
Comments on Test Procedure		1100
<ul> <li>Purpose: To verify that the DUT properly behaves while in the TX_D state.</li> <li>Procedure: <ul> <li>a. The DUT is instructed to transmit a valid data block while in the TX encode all 72-bit vectors and remain in the TX_D state.</li> <li>b. The DUT is instructed to transmit a valid T block while in the TX_D all 72-bit vectors and transition to the TX_T state.</li> <li>c. The DUT is instructed to transmit a valid E block while in the TX_D d blocks. The DUT should properly encode all 72-bit vectors and transition to the TX_T state.</li> </ul> </li> </ul>	D state. The l state. The DU state. This is r	T should properly encode repeated using valid S and
<ul> <li>a. The DUT was observed to properly remain in the TX_D state.</li> <li>b. The DUT was observed to properly transition to the TX_T state.</li> <li>c. The DUT was observed to properly transition to the TX_E state.</li> </ul>		

		/
Test # and Label	Part(s)	Result(s)
Test 49.5.9: TX_T state	a-c	PASS
Comments on Test Procedure		
<ul> <li>Purpose: To verify that the DUT properly behaves while in the TX_</li> <li>Procedure:</li> <li>a. The DUT is instructed to transmit a valid C block while in the all 72-bit vectors, and transition to the TX_C state.</li> </ul>		T should properly encode
<ul> <li>a. The DUT is instructed to transmit a valid S block while in the T all 72-bit vectors, and transition to the TX_D state.</li> <li>a. The DUT is instructed to transmit a valid E block while in the and T blocks. The DUT should properly encode all 72-bit vect</li> </ul>	e TXT state. This	is repeated using valid D
Comments on Test Results		
<ul> <li>a. The DUT was observed to properly transition to the TX_C state</li> <li>b. The DUT was observed to properly transition to the TX_D state</li> <li>c. The DUT was observed to properly transition to the TX_E state</li> </ul>	e.     /	
Test # and Label	Part(s)	Result(s)
Test 49.5.10: TX_E state	a-d	PASS
Comments on Test Procedure		
<ul> <li>Purpose: To verify that the DUT property behaves while in the TX_Procedure:</li> <li>a. The DUT is instructed to transmit a valid D block while in the TA_D state.</li> <li>b. The DUT is instructed to transmit a valid C block while in the TA_D state.</li> <li>b. The DUT is instructed to transmit a valid C block while in the TA_D state.</li> <li>c. The DUT is instructed to transmit a valid T block while in the TA_D state.</li> <li>d. The DUT is instructed to transmit a valid T block while in the TA_D state.</li> <li>d. The DUT is instructed to transmit a valid T block while in the TA_D state.</li> <li>d. The DUT is instructed to transmit a valid D block while in the all 72-bit vectors and remain in the ITX_E state.</li> <li>d. The DUT is instructed to transmit a valid D block while in the TA_D block while in the TA_D block while in the All 72-bit vectors and remain in the ITX_E state.</li> </ul>	TX_E state. The DU TX_E state. The DU TX_E state The DUT TX_E state The DUT	T should properly encode should properly encode
<ul> <li>a. The DUT was observed to properly transition to the TX_D stat</li> <li>b. The DUT was observed to properly transition to the TX_C state</li> <li>c. The DUT was observed to properly transition to the TX_T state</li> <li>d. The DUT was observed to properly remain in the TX_E state.</li> </ul>	e.	

est # and I								Part(s)	)	Result	
est 49.6.1: I	dentifica	ation of R_TY	PE(C)					a-c		PAS	S
omments o											
rpose: To v	verify the	at the DUT pr	operly ic	lentifies	the rece	eption of	$\mathbf{R}_{TY}$	PE(C) ve	ctors.		
1											
ocedure:	ha tastir	ng station to tr	onemit o	block o	ontoinin	0000	f tha fal	lowing	ncodina	· ·	
Instruct	ine testii	ig station to u	ansnin a	DIOCK C	omanni	ig one of	i the for	lowing e	ncounig	s.	
	Sync	Block type	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	$C_4$	C <sub>5</sub>	C <sub>6</sub>	$C_7$	
	10	0x1E	0x00	0x00	0x00	0x00	ØxQ0	0x00	0x00	0x00	
	10	0x1E	0x2D	0x33	0x4B	0x55	0x66	0x78	ØxØ0	0x00	
ne DUT sho		perly decode a									
		ng station to tr				ig one o	f the fol	lowinge	ncoding	s	
		-									
	Sync	Block type	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	$0_4$	$D_5$	$D_6$	$\mathbf{D}_7$	
	10	0x2D	0x00	0x00	0x00	0x00	0x0	0x00	0x00	0x01	
	10	0x2D	0x00	Øx00	0x00	0x00	0x0	Qx00	0x00	0x02	
	10	0x2D	0x00	0x00	0x00	0x00	Øx0	Øx00	0x00	Ox00	
	10	0x2D	0x00	0x00	0x00	0x00	0xF	<b>\$</b> x00	0x00	0x00	
	10	0x2D	0x2D	0x33	0x4B	0x55	0xØ	0x00	0x00	0x01	
		1	1				$ \land $				
	Sync	Block type	D <sub>1</sub>	$D_2$	D <sub>3</sub>	<b>O</b> <sub>0</sub>	$C_4$	C <sub>5</sub>	$C_6$	$C_7$	
	10	0x4B	0x00	0x00/	0x01	0x0	0x00	0x00	0x00	0x00	
	10	0x4B	$0 \times 00$	0x00	0x02	0x0	0x00	0x00	$0 \times 0 0$	0x00	
	10	0x4B	0x12	0x34	0x56	0x0	0x00	0x00	0x00	0x00	
	10	0x4B	0x00	0x00	0x00	0xF	$0 \times 00$	0x00	$0 \times 00$	0x00	
	10	0x4B	$0 \times 00$	0x00	0x01	0x0	0x2D	0x33	0x4B	0x55	
		perly decode a						1			
mstruct		g station to tr Block type	$\mathbf{D}_1$	$D_2$	D	•	$O_4$	D <sub>5</sub>		<u>D</u> 7	
	Sync 10	$0x55 \land$	$\frac{D_1}{0 \times 00}$	$\mathbf{D}_2$ $0\mathbf{x}00$	0x01	$\frac{O_0}{0x0}$	0x0	0x00	$D_6$ 0x00	0x01	
	10	0x55	0x00	0x00	0x01	0x0	0x0	0x00	0x00	0x01 0x02	
$\left  \right\rangle \right $	10	0x55	0x00	0x00	0x04	0x0	0x0	0x00	0x00	0x02 0x02	
	10	0x55	$0 \times 0 0$	0x00	0x01 0x02	0x0	0x0	0x00	0x00	0x02	
	10	0x55	0x00	V	0x02	0x0	0x0	0x00	0x00	0x56	
		0x55	0x00		0x56	0x0	0x0	0x12 0x00	0x00	0x01	
	$10 \\ 10$	Øx55	0x12	0x34	0x56	0x0	0x0	0x00	0x00	0x02	
	$10 \\ 10$	Øx55	010	0x00	0x02	0x0	0x0	0x12	0x34	0x56	
	$10^{\circ}$	Øx55	0x12	0x34	0x56	0xF	0x0	0x00	0x00	0x01	
	10	Øx55	0x12	0x34	0x56	0xF	0x0	0x00	0x00	0x02	
	10	Øx55	0x00	0x00	0x01	0x0	0xF	0x12	0x34	0x56	
	10	0x55	0x00	0x00	0x02	0x0	0xF	0x12	0x34	0x56	
	10	Øx55	0x12	0x34	0x56	0xF	0xF	0x78	0x9A	0xBC	
	10	0x55	0x12	0x34	0x56	0x0	0x0	0x78	0x9A	0xBC	
ne DUT sho	ould prop	perly decode a	W 66-bit								
omments o	_										
	F was ob	served to pro	perly de	code all	66-bit v	ectors.					
The DU	I was ou										
		served to pro		code all	66-bit v	ectors.					

			) Gigabit			ity Laborato 1		
Test # and Label						Part(s)	D	esult(s)
Test 49.6.2: Identific	ation of R TV	PF(S)						PASS
Comments on Test		1 L(5)				a-c	·	Abb
Purpose: To verify th		operly identifi	es the rece	ention of	R TY	PE(S) vecto	ors	
r dipose. To verify di	lat the DOT pr	openty identified		eption of	K_111			
Procedure:								
a. Instruct the testi	ng station to tr	ansmit a block	containin	ng one of	f the fol	lowing enc	odings:	
	-			-		-	- (	
Sync		C <sub>0</sub> C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>			$D_6 D_7/$	1 1 1 1 1
10	0x33	0x00 0x00		0x00	0x0		0x55 0x55	
10	0x33	0x2D 0x33		0x55	ØxQ	0x55 0	0x55 0x55	
The DUT should pro						(		
b. Instruct the testi	ng station to tr	ansmit a block	containin	ng one o	f the fol	lowing enc	odings:	
<b>C</b>	D11. (		D					
Sync 10		$\begin{array}{c c} D_1 & D_2 \\ \hline 0x00 & 0x00 \end{array}$	D <sub>3</sub> 0x01	$O_0$	0x0		$D_6 \cap D_7$ (x\$5) 0x55	
10	0x66 0x66	0x00 0x00 0x00 0x00		0x0 0x0	0x0		x55 0x55	
10	0x66	0x12 0x34		0x0	0x0		x55 0x55	-
10	0x66	0x12 $0x04$ $0x00$		0x0	$0\mathbf{x}0$		x55 0 x55	
The DUT should pro								
c. Instruct the testi						lowing enc	odingst	
							$\nabla^{a}$	
S	ync Block ty	vpe D <sub>1</sub> I	$\mathbf{D}_1 = \mathbf{D}_3$	$\mathbf{D}_4$	D	$_{5}$ $D_{6}$	$D_7$	
1	0 0x78	0x55 0	\$55 0x	55 Ox	55 Oz	55 0x55	0xD5	
The DUT should pro	perly decode a	ull 6ø-bit vecto	rs and rec	eive the	frame.			
Comments on Test         a.       The DUT was o         b.       The DUT was o         c.       The DUT was o	bserved to pro	perly decode a	ll 66-bit v	vectors a	nd recei	ve the fram	ie.	
				V				
Test # and Label						Part(s)		esult(s)
Test 49.6.3. Identific		PE(T)				a	]	PASS
Comments on Test	Procedure							
Purpose: To verify th	hat the DUT pr	operly identified	es the rece	eption of	$\mathbf{R}_{\mathbf{T}}$	PE(T) vecto	ors.	
Procedure: a Instruct the test block field types					ectors to	o the DUT,	containing t	he appropriate
	ГТ	$_{0}C_{1}C_{2}C_{3}/C_{4}C_{5}$	$C_6C_7$	$D_0 D_1 D_2 D_1$	O <sub>3</sub> /T₄C₅C	$C_6C_7$		
		0010203/0403		$D_0 D_1 D_2 D_1 D_2 D_2$				
		$D_0 D_1 T_2 C_3 / C_4 C_5$		$D_0 D_1 D_2 D_1 D_2 D_2$				
		$D_0 D_1 D_2 T_3 / C_4 C_5$		$D_0 D_1 D_2 D_1$				
						<u> </u>		
The DUT should pro		ill 66-bit vecto	rs and rec	erve the	frame.			
The DUT should pro		ill 66-bit vecto	rs and rec	erve the	frame.			
The DUT should pro Comments on Test	perly decode a	ill 66-bit vecto	rs and rec	erve the	frame.			

DUT: 10 Gigabit Ethernet Sv	vitch	
Test # and Label	Part(s)	Result(s)
Test 49.6.4: Identification of R_TYPE(D)	a	PASS
Comments on Test Procedure		
<ul> <li>Purpose: To verify that the DUT properly identifies the reception of R_</li> <li>Procedure: <ul> <li>a. The testing station is instructed to transmit data blocks to the DUT state. All valid data blocks should be sent to the DUT. The DUT and receive the frames.</li> </ul> </li> </ul>	such that the DUT	
Comments on Test Results		
a. The DUT was observed to properly decode all 66-bit vectors and a		
Test # and Label	Part(s)	Result(s)
Test 49.6.5: Identification of R_TYPE(E)	∩ <b>a</b>	PA\$S
<b>Comments on Test Procedure</b> Purpose: To verify that the DUT properly identifies the reception of B		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$C_7$ 0x1E
Comments on Test Results		
a. The DLT was observed to properly decode all 66-bit vectors as R	_BLOCK_TYPE(E)	

Test # and Label         Test 49.6.6: RX_INIT state		Part(s)a,b,d	Result(s) PASS
Test 49.0.0. KX_INT state		c	Not Tested
Comments on Test Procedure			
Purpose: To verify that the DUT passes local fa	ult across the XGMI	II when in the RX_INI	Γ state.
When the DUT has been reset, is in a test mode remain within the RX_INIT state. While in the XGMII to signify that the receiver is not operation a. When the DUT does not have block_lock, it b. When the DUT has hi_ber, it must pass corr c. When the reset signal is set, the DUT must d. When in the receive test mode, the DUT m	is state, the DUT w ional. it must pass continue tinuous local faulta pass continuous loc	ill be sending local fau ous local fault across f across the XGMII al fault across the XGM	ilt blocks up across the A XGMII.
Comments on Test Results			
<ul> <li>a. When the DUT does not have block_lock, is</li> <li>b. When the DUT has high_ber, it was observed.</li> <li>c. This test was not performed during the test.</li> <li>d. When in the receive test mode, the DUT was put into the receive test mode by</li> </ul>	ed to properly passing period.	local_fault across the X	KGMIII.
Test # and Label		Part(s)	Result(s)
Test 49.6.7: RX_C state		a-c	PASS
Comments on Test Procedure Purpose: To verify that the D/JT\properly behav	1.1.1. to the DW		
<ul> <li>When the receiver of the DUT has achieved sy 56-bit level, the DUT will enter the RX_C state valid idle or sequence ordered_sets are being reported RX_D state. Reception of E, D, or T block.</li> <li>The DUT should properly decode all 66-bit block.</li> <li>The DUT should properly decode all 66-bit block.</li> </ul>	nchronization, and v e in Figure 49-15. ceived, Upon the re eks will force the DU vectors and remain vectors and transiti	when valid C blocks ar The DUT will remain ception of an S block, UT to the RX_E state. in the RX_C state whi on to the RX_D state v	in this state as long as the DUT will transition le receiving C blocks. while receiving an S
Comments on Test Results			
<ul> <li>a. The DUT was observed to properly decode blocks.</li> <li>b. The DUT was observed to properly decode receiving at Sblock.</li> <li>c. The DUT was observed to properly decode E, D, or T blocks.</li> </ul>	ode all 66-bit vect	ors and transition to	the RX_D state while

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Test # and Label	Part(s)	<b>Result</b> (s)
Test 49.6.8: RX_D state	a-d	PASS
Comments on Test Procedure Purpose: To verify that the DUT properly behaves while in the RX_D s		
When the receiver of the DUT has achieved synchronization, and whe 66-bit level, the DUT will enter the RX_D state in Figure 49-15 upon to remain in the RX_D state as long as valid D blocks are being received state upon reception of a T block, provided that the block following th combinations of received blocks, the DUT will transition to the RX_E a. The DUT should properly decode all 66-bit vectors and remain in b. The DUT should properly decode all 66-bit vectors and transition c. The DUT should properly decode all 66-bit vectors and transition d. The DUT should properly decode all 66-bit vectors and transition	the reception of an S ed. The DUT will e T is either an S or state. the RX_D state. to the RX_T state. to the RX_E state.	S block. The DUT will transition to the RX_T
Comments on Test Results		
<ul> <li>a. The DUT was observed to properly decode all 66-bit vectors and r</li> <li>b. The DUT was observed to properly decode all 66-bit vectors and t</li> <li>c. The DUT was observed to properly decode all 66-bit vectors and t</li> <li>d. The DUT was observed to properly decode all 66-bit vectors and t</li> </ul>	ransition to the RX	_T state. _E state.
Test # and Label	Part(s)	Result(s)
Test 49.6.9: RX_T state	a-b/	PASS
<b>Comments on Test Procedure</b> Purpose: To verify that the DVT properly behaves while in the RX_T s When the receiver of the DWT has achieved synchronization, and whe 66-bit level, the DUT will enter the RX_T state in Figure 49-15 upon to remain in the RX_D state as long as valid D blocks are being received state upon reception of a T block, provided that the block following RX_T state is entered, the DUT will transition to either the RX_C or R a. The DUT should properly decode all 66-bit vectors, and transition b. The DUT should properly decode all 66-bit vectors, and transition <b>Comments on Test Results</b>	n valid D blocks are the reception of an S ed. The DUT will the T is either an S X_D state, dependin to the RX_C state.	S block. The DUT will transition to the RX_T or C block. Once the
Comments on Test Results		
a. The DUT was observed to properly decode all 66-bit vectors and t b. The DUT was observed to properly decode all 66-bit vectors and t		

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Test # and Label		Part(s)	Result(s)
Test 49.6.10: RX_E state		a-e	PASS
Comments on Test Procedure			
Purpose: To verify that the DUT properly behaves while in the R	X_E state.		
When the receiver of the DUT encounters some sort of error, it we state. While in this state, regardless of the 66-bit words coming and passed up to the XGMII. If errors are received in the midd state when it receives a valid D block, or transition to the RX_T are received, the DUT will transition to the RX_C state. The continue to be received or if an S block is encountered. a. The DUT should properly decode all 66-bit vectors and transite. The DUT should properly decode all 66-bit vectors and transite. The DUT should properly decode all 66-bit vectors and transite. The DUT should properly decode all 66-bit vectors and transite. The DUT should properly decode all 66-bit vectors and transite. The DUT should properly decode all 66-bit vectors and transite. The DUT should properly decode all 66-bit vectors and transite.	g into the le of a fran State at the DUT will sition to the sition to the sition to the	receiver, error bl me, the DUT ma ne end of the fran Il remain in the e RX_D state. e RX_C state. e RX_T state. RX_E state.	ocks will be decoded y return to the RX_D ne. If valid C blocks
Comments on Test Results			
a. The DUT was observed to properly decode all 66-bit vectors b. The DUT was observed to properly decode all 66-bit vectors c. The DUT was observed to properly decode all 66-bit vectors e. The DUT was observed to properly decode all 66-bit vectors all 66-bit vectors of the DUT was observed to properly decode all 66-bit vectors all 66-bit vectors of the DUT was observed to properly decode all 66-bit vectors all 60-bit vectors of the DUT was observed to properly decode all 60-bit vectors of th	and trans and trans and rema	ition to the RV_0 ition to the RX_7 in in the RX_E s	state. state. tate.

#### **GROUP 7: Test Pattern Verification**

Yest # and Label	Part(s)	Result(s)
est 49.7.1: Pseudo-random test pattern transmission	a-b	Not Available
Comments on Test Procedure		
urpose: To verify that the DUT generates the correct pseudo-rar Clause 49 defines a pseudo-random test pattern generator and unctionality allows the tester to not only verify BER over a cha he appropriate signals used for testing. When the PCS mplementation of the generator and checker is mandatory. The	checker to be implem nnel, but also to force t offers a direct conne	he DUT into transmittin ction to the PMA, th
sing specific seeds that are regularly loaded through the MDI atterns to be scrambled. Every 128 blocks, the scrambler is lo he following pattern: Seed A, Seed A Invert, or Seed B, Seed E clause 52, and shown in Table 52-20. The data patterns fed to ncoding of two Local Fault ordered_sets, and the data pattern we sed. Register 3.42 controls the different test patterns that can be the DUT should properly generate Pseudo-Random Test Pa	oregisters, and using aded with one of two s Invert. The values of rough the scrambler a vill be inverted when the transmitted and check ttern 1.	one of two possible dat eeds, or their inverses, i f the seeds are defined i re either all zeros, or th inverted seeds are bein
. The DUT should properly generate Pseudo-Random Test Pa	ttertrí 2.	
. This test was not completed during the testing period due to . This test was not completed during the testing period due to		
est # and Label	Dort(c)	<b>D</b> ogult(c)
est 49.7.2: PRBS31 test/pat/ern/transmission	Part(s)	Result(s) Not Available
Comments on Test Procedure	/a	Not Available
proses To verify that the DUT generates the correct PRBS31 te	at not from	
Plause 49 defines an optional PRBS31 test pattern mode that anismission and checking of the pattern. When selected, the geown to the PMA, bypassing the scrambler. The pattern generated with the following polynomial: $G(x) = 1 + x^{24}$ atterns that can be transmitted and checked.	can be implemented nerator sends 16 bits of rator implements an in	f the test pattern at a time everted version of the bi
. The DUT should properly generate the PRBS31 test pattern.		
Comments on Test Results		
. This test was not completed during the testing period due to	test station limitations.	
VILL		

Test # and Label	Part(s)	Result(s)
Test 49.7.3: Square wave test pattern transmission	a	Not Available
Comments on Test Procedure		
Purpose: To verify that the DUT generates the correct square wave test p		
Certain PMD tests that need to be performed require that the PCS general necessarily needs to bypass the encoder and scrambler, and does not of wave pattern is selected, the PCS will send a repeating pattern of <i>n</i> ones	contain any synd	c bits. When the square
number between 4 and 11, inclusive. The value of $n$ is and implementation value in some devices. Register 3.42 controls the different test patterns to	tion choice, and	may be a programmable
a. The DUT should properly generate the square wave test pattern for	all values of <i>p</i> .	
Comments on Test Results		
a. This test was not completed during the testing period due to test stat	ion/limitations.	
Test # and Label	Part(s)	Result(s)
Test 49.7.4: Pseudo-random test pattern reception	<b>Part(s)</b>	Not Available
Comments on Test Procedure		
Purpose: To verify that the DUT generates the correct pseudo-random te	st patterns.	
Clause 49 defines a pseudo-random test pattern generator and checker to functionality allows the tester to not only verify BER over a channel, but	be implemented	d in the PCS. This e DUT into transmitting
the appropriate signals used for testing. When the PCS offers a direct co- implementation of the generator and checker is mandatory. The jitter test	nnection to the last pattern is gene	PMA, the scrambler,
using specific seeds that are regularly loaded through the MDIO register patterns to be scrambled. Every 128 blocks, the scrambler is loaded with the following pattern: Seed A, Seed A Invert, or Seed B, Seed B Invert	1 one of two see	ds, or their inverses, in
Clause 52, and shown in Table 52-20. The data patterns fed through the encoding of two Local Fault ordered_sets, and the data pattern will be in	scrambler are ei	ther all zeros, or the inverted seeds are being
used Register 3.42 controls/the different test patterns that can be transm The pseudo-random checker utilizes the lock state machine and d		
operations. However, the hi_ber state machine is disabled when the poutput of the descrambler is the data pattern or its inverse, a match is de is loaded with a seed value every 128 blocks and the receiver's descram	test pattern mod tected. Since th	le is enabled. When the transmitter's scrambler
be detected once every 128 blocks in the absence of errors. Therefore windows and ignore the first block within a window that contains a mi	re, the receiver	will count in 128-block
a. The DUT should lock on and receive Pseudo-Random Test Pattern 1	l, and all mismat	tches apart from the first
<ul> <li>in every 128-blocks, should be counted.</li> <li>The DUT should lock on and receive Pseudo-Random Test Pattern 2 in every 128-blocks, should be counted.</li> </ul>	2, and all mismat	tches apart from the first
Comments on Test Results		
a This test was not completed during the testing period due to test stat b. This test was not completed during the testing period due to test stat		

Test # and Label	Part(s)	Result(s)
Test 49.7.5: PRBS31 test pattern reception	а	Not Available
Comments on Test Procedure		
<b>Comments on Test Procedure</b> Purpose: To verify that the DUT generates the correct PRBS31 test patt Clause 49 defines an optional PRBS31 test pattern mode that can be transmission and checking of the pattern. When selected, the generator down to the PMA, bypassing the scrambler. The pattern generator is stream generated with the following polynomial: $G(x) = 1 + x^{28} + x^{31}$ patterns that can be transmitted and checked. When the receive chann PRBS31 pattern checker checks the bits received from the PMA, by relative to the PRBS31 test pattern. The pattern error checker is se received to the result of the PRBS31 generator based on the prior 31 pattern error signal will be zero. When an isolated bit error occurs, the three times, and the test-pattern error counter will increment once for e signal is high. a. The DUT should properly receive the PRBS31 test pattern, and pro-	be implemented or sends 16 bits o implements an in . Register 3.42 nel is operating is passing the descri- ell synchronizin bits received e PRBS/31 patter each bit time that	f the test pattern at a time nverted version of the bit controls the different test in PRBS31 test mode, the rampler, and checks them g, and compares each bit when no errors occur, the n error signal will go high the PRBS31 pattern error
Comments on Test Results		
a. This test was not completed during the testing period due to test sta	ation limitations.	