Preamble modifications for 1000BASE-PX networks

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1. INTRODUCTION

Currently, the IEEE 802.3ah Task Force is in the final stages of completing a set of specifications for Ethernet in the First Mile (EFM). Included in this documentation are extensions of the Clause 35 Reconciliation Sublayer (RS), which are specified in the new Clause 65. Some of the extensions that have been made to the RS contain modifications to the traditional Ethernet frame structure, specifically in the preamble field. This paper seeks to describe these preamble changes and provide examples that may be followed in order to understand how a proper implementation could be designed.

2. PREAMBLE DESCRIPTION

Even though an Ethernet Passive Optical Network (EPON) device uses a Physical Coding Sublayer (PCS) and Media Access Control (MAC) sublayer that are identical to the ones used by 1000BASE-X devices, extensions have been added to the RS in order to allow for point-to-point emulation. Figure 1 shows the fields of the EPON frame. Although most of the fields are identical to that of a 1000BASE-X frame, there is a significant difference in the contents of the first part of the frame, the preamble. In a traditional device, this field would contain seven bytes of 0x55 and a single eighth byte of 0xD5. The preamble was traditionally used for clock synchronization and to inform a device that a frame was on the way, and has been kept on with additions to IEEE 802.3 primarily for backwards compatibility issues.

For EPON devices, the preamble contains a significant amount of information. As shown in Figure 1, four bytes of the preamble have been left unaltered and will still be transmitted as 0x55. The third byte of preamble contains a Start of Packet Delimiter (SPD) that is transmitted as 0xD5. The sixth and seventh bytes are replaced with a Logical Link ID (LLID) that contains the LLID and mode bit associated with either an ONU or the OLT. A unique LLID is assigned by the OLT to each ONU once the registration process is complete. The RS of the ONU will filter frames based on the value of the LLID field in the preamble. This was a necessary feature to add to the EFM specifications in order to allow for the architecture of the PON. For example, in a typical shared ethernet network, a device that transmits a frame will not receive the exact frame that it transmitted. A repeater or switch will forward a frame out all ports other than the port on which it was received. The nature of the PON makes this impossible. The OLT can be placed in a mode that will force it to forward all frames it receives from one ONU to all other ONU's. Doing this will mean that the initiating ONU will receive its own frame. Whereas this could potentially cause problems in a traditional ethernet network, the filtering that takes place in the RS using the modified preamble will prevent the originating MAC from receiving its own frames.

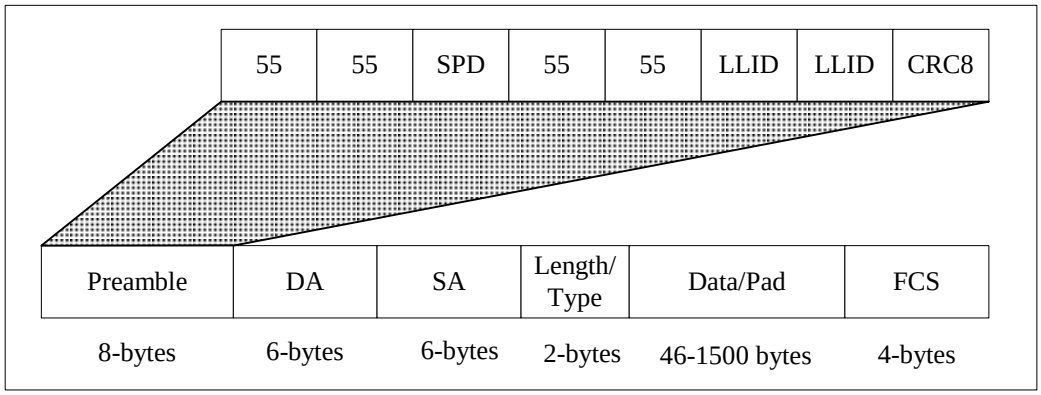

Figure 1. 1000BASE-PX frame structure

Table 1 shows the values that are to be transmitted in the preamble fields. The mode bit is assigned to be a 1 for an Optical Line Terminal (OLT) MAC and a 0 for an Optical Network Unit (ONU) MAC. The 15-bit logical_link_id value is set to a broadcast value of 0x7FFF for the ONU before it has registered with the OLT and it is assigned a value other than 0x7FFF after the registration process has completed. The OLT may use any value for this variable. Finally, the CRC8 field contains an 8-bit value that is computed as a function of the preamble from the first bit of the SPD through the last bit of the LLID.

Preamble field	**Value**
SPD	0xD5
LLID[15:8]	<mode, logical_link_id[14:8]>
LLID[7:0]	<logical_link_id[7:0]>
CRC8	Calculated 8-bit CRC

Table 1. Values for preamble fields

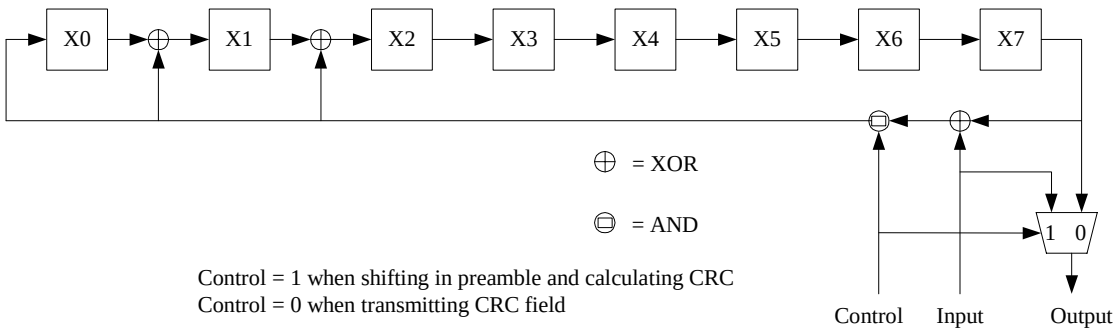

Figure 2. Serial implementation of CRC8 generator

Figure 2 shows a serial implementation of the CRC8 generator using an 8-bit shift register a few other logic gates and a multiplexer. The register is initialized to the value 0x00 every time a new frame is being transmitted. The calculation takes place on the 40 bits from the SPD to the end of the LLID fields and then the result is attached to the end of the preamble before the frame is passed on to the PCS.

3. PREAMBLE EXAMPLE

The preamble is defined in IEEE Std. 802.3-2002 Clause 35.2.3.2.1 for 1000BASE-X devices. It is a seven-octet pattern, followed by a one-octet Start of Frame Delimiter (SFD), which indicates that the next bit following the SFD is the first bit of data in the frame. When transmitted serially from left to right the preamble and SFD take on the following pattern:

10101010 10101010 10101010 10101010 10101010 10101010 10101010 10101011

If we assume that we are dealing with an OLT that is using the LLID value of 0x7FF, then the following would be the 1000BASE-PX preamble pattern, with the x's representing the currently unknown CRC8 value:

10101010 10101010 10101011 10101010 10101010 11111111 11111111 xxxxxxxx

The CRC8 calculation takes place beginning with the third byte of preamble and continues through the seventh byte. The preamble bits will enter the shift register shown in Figure 2 from left to right, exactly as they are shown here:

10101011 10101010 10101010 11111111 11111111

After 40 clock cycles, assuming the calculation is being done in a serial fashion. the following values will be in the shift register:

X0	X1	X2	X3	X4	X5	X6	X7
0	0	1	0	0	0	1	1

These bits will then leave the shift register serially from X7 down to X0 so that the CRC8 value to be transmitted is:

11000100

Putting all of the preamble fields back together, the transmitted preamble will look like this (remember that each byte is transmitted LSB to MSB):

Binary (MSB LSB)	Hex
01010101	0x55
01010101	0x55
01010111	0xD5
01010101	0x55
01010101	0x55
11111111	0xFF
11111111	0xFF
00100011	0x23