## Deficit Idle Count

Examples and Explanation of how the RS aligns the Start control character

# Start Character Alignment

- Start character needs to be aligned to lane 0
- Frames can terminate on any lane
- Nominal minimum gap of 12 bytes of Idle
- RS may need to modify length of <interframe> to do this alignment with 2 methods
  - Always add Idle
  - Maintain Deficit Idle Count (DIC)

# Adding Idle

- There is no maximum amount of idle specified between frames
- Allowed to insert as much as you want
- Adding idle reduces effective data rate
  - Lots of wasted bandwidth
  - For frames that end on lane 1, you need to add
     3 extra bytes of idle if another frame is waiting,
     to align to lane 0.

## Deficit Idle Count

- Sometimes insert and sometimes delete idle to align Start to lane 0
- DIC maintains count of characters deleted or inserted
- Increment for every idle character deleted
- Decrement for every idle character inserted
- Minimum value of 0, Maximum value of 3

## Results of DIC

- Possible to transmit a frame with up to 3 bytes less than minimum inter-frame gap
- DIC also mandates transmission greater than minimum inter-frame gap on occasion
- Average inter-frame gap remains at 12 bytes of idle

# DIC Algorithm

	Current DIC = 0		Current DIC = 1		Current DIC = 2		Current = 3	
Packet Length Modulo 4	IPG Length	New DIC value	IPG Length	New DIC value	IPG Length	New DIC value	IPG Length	New DIC value
n+0	12	0	12	1	12	2	12	3
n+1	11	1	11	2	11	3	15	0
n+2	10	2	10	3	14	0	14	1
n+3	9	3	13	0	13	1	13	2

# Deficit Idle Count Examples

Example of sending frames with and without implementing DIC

Lane0	Lane1	Lane2	Lane3
I	_		- 1
~	~	٧	~
ı	_		I
S	D	D	D
D	D	D	D
~	2	2	~
D	D	D	D
Т	_		I
ı	_	- 1	I
	_		I
S	D	D	D
D	D	D	D
~	2	2	~
D	D	D	D
D	D	D	T
_	_		I
	_		I
-	_		I (extra)
S	D	D	D
D	D	D	D
~	?	2	~
D	D	D	D
D	T		
	_		- 1
	_		- 1
	I (extra)	I (extra)	I (extra)
S	D	D	D
D	D	D	D

The frames on the left are sent without implementing DIC. This means that extra idle must be inserted to align Start to Lane0.

Lane0	Lane1	Lane2	Lane3	7
	1	I	ı	
~	~	~	~	
I	ı	I	ı	
S	D D	D	D	
D	D	D	D	
~	~	~	~	
D	D	D	D	
T	ı		I	
I	ı	_	I	
		I		DIC=0
S	D D	D	D	
D	D	D	D	
~	~	~	~	
D	D D	D	D	
D		D	Т	
I			I	
I	ı	I	ı	DIC=3
S	D	D	D	
D	D	D	D	
~	~	~	~	
D	D T	D	D	
D	T	I	I	
I	I	1	I	
I		I	I	
I	I	I	I	DIC=0
~ I S D T I I S D D D D D D D D D D D D D D D D D	D	D	D	
D	D	D	D	

The frames on the right implement DIC. This means that fewer than 12 bytes of Idle can be sent some of the time, and that greater than 12 bytes must be sent some of the time.

#### Deficit Idle Count

# Deficit Idle Count Examples

D T I I I DIC=1  I I I I I I DIC=1  S D D D D  D D D D  C C C C C C C C C C C	Lane0	Lane1	Lane2	Lane3	
	D	T			
	I	I	I	I	
S D D D D D D D D D D D D D D D D D D D			I	I	DIC=1
D D D D D D D D D D D D D D D D D D D	S				
~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	D	D	D	D	
D D D D D D D D D D D D D D D D D D D	~	~		~	
D T I I I D DIC=2    I	D	D	D		
	D	T	I	1	
	I		I	I	
S D D D D D D D D C C C C C C C C C C C C	I	I	I	I	DIC=2
D D D D D D D D D D D D D D D D D D D	S	D		D	
~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	D	D	D	D	
D D D D D D D D D D D D D D D D D D D	~	~	~	~	
D T I I I I DIC=3  I I I I I I DIC=3  S D D D D D  D D D D D  T I I I I I I I I I I I I I I I I I I	D	D	D	D	
	D	Τ	I	I	
	I	I		I	
S D D D D D D C C C C C C C C C C C C C C	I	I		I	DIC=3
D D D D  ~ ~ ~ ~ ~ ~ ~ ~  D D D D D  D T I I I  I I I I I  I I I I I  S D D D D  D D D  D D D  D D D  D D D  D D D  T I I I I  I I I I I I I  I I I I I I	S	D	D	D	
~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	D	D	D	D	
D D D D D D D D D D D D D D D D D D D	~	~	~	~	
D T I I I I I I I I I I I I I I I I I I	D	D	D	D	
	D	T	I	I	
				I	
	I			I	
S D D D D D D ~ ~ ~ ~ ~ ~ D D D D D D T I I I I I I I ~ ~ ~ ~ ~ ~	I			I	DIC=0
D D D D D D D D D D D D D D D D D D D	S	D	D	D	
~ ~ ~ ~ ~ ~ D D D D D D D D D D D D D D	D	D	D	D	
D D D D D D D D D D D D D D D D D D D	~	2		?	
D T I I I I I I I I I I I I I I I I I I	D	D	D	D	
	D	T		I	
~ ~ ~ ~	I	I	l l	I	
	~	~	~	~	
	I		l l	I	

This shows several frames of the same size being sent while implementing DIC. Note that the average amount of Idle being sent remains at 12 bytes.

## Conclusion

- DIC gives the RS an efficient mechanism to align Start control characters to lane 0 without always inserting extra idle
- DIC allows for minimum inter-frame gap to vary from 9 to 15 bytes with the average gap value remaining at 12 bytes

#### To Learn More

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