UNH-IOL MIPI Alliance Test Program
D-PHY TX Conformance Test Report

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22-Jul-2016

Engineer Name
Sample Company, Inc.
1010 Mobile Way
San Jose, CA 95101

Mr. Engineer:

Enclosed are the test results from the D-PHY TX Physical Layer Conformance testing performed on the:

Sample Company 1234 Camera Sensor 1-Lane CSI-2 Transmitter

The testing was performed according to v1.2r13 of the MIPI Alliance D-PHY Physical Layer Conformance Test Suite, which is available to MIPI Alliance Members at:

https://members.mipi.org/wg/D-PHY/document/folder/8817

Also note that most of the measurements in this report were performed on captured DSO waveform data using the freely available DPHYGUI physical layer conformance software tool, which is available to all MIPI members, and may be downloaded at the URL above. The raw waveform data files used for this report may be obtained upon request, if duplication of results or further analysis of the data is desired. (Contact UNH IOL for assistance.)

Any issues observed during testing are listed below:

- **NO CONFORMANCE ISSUES WERE OBSERVED DURING TESTING**

Please feel free to contact me at kerry.munson@iol.unh.edu with any questions you may have regarding this report.

Sincerely,

Kerry A Munson

Kerry Munson

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Table 1: Test Setup and DUT Configuration Information

DUT Details	
Week testing was performed	20160722
Manufacturer	Sample Company
Model	1234 Camera Sensor
Number of HS Data Lanes	1
Max. Supported HS Bit Rate	2500 Mbps
Tested HS Bit Rate	2500 Mbps
Mfr. Serial Number	9876543210
Firmware Version	v1.0
Process Speed	v0.10
Supply Voltage	Vnom
Environmental Temperature	25 C (Tnom)
Test Pattern	UNH Test Pattern
UNH-IOL ID Number	99999
Test System Hardware	
Real-time DSO	Tektronix MSO73304DX, 33 GHz 100 GS/s Mixed-signal Oscilloscope with three Tektronix P7513A 13 GHz Differential Probes (Groups 2-5)
Termination Fixture	UNH-IOL D-PHY Reference Termination Board (RTB) v3.3
Temperature Forcing System	Temptronic ThermoStream, Model TPO4100A-1

Additional Comments/Notes

All test results marked 'N/A' are considered Not Applicable, due to the DUT not implementing these lanes.

Conformant (i.e., passing) results are indicated in **green** text. Conformant results that are close to the failure limits are indicated in **yellow** text. Failing results are indicated in **red** text.

Table 2: (Section 1, Groups 1+2): Clock/Data Lane LP-TX Signaling Requirements:

Test/Parameter	Conf. Range	Clk Lane Measured	Lane 0 Measured	Lane 1 Measured	Lane 2 Measured	Lane 3 Measured	Units	Fig.
Test 1.2.1/1.1.1: Clock/Data Lane LP-TX Thevenin Output High Level Voltages (V_{OH}) (50pF C_{LOAD})								
Measured V_{OH} for V_{DP}	950 / 1300	**1170.9**	**1165.5**	N/A	N/A	N/A	mV	1
Measured V_{OH} for V_{DN}	950 / 1300	**1171.1**	**1161.6**	N/A	N/A	N/A	mV	2
Test 1.2.2/1.1.2: Clock/Data Lane LP-TX Thevenin Output Low Level Voltages (V_{OL}) (50pF C_{LOAD})								
Measured V_{OL} for V_{DP}	-50 / +50	**3.0**	**-5.9**	N/A	N/A	N/A	mV	1
Measured V_{OL} for V_{DN}	-50 / +50	**6.9**	**2.6**	N/A	N/A	N/A	mV	2
Test 1.2.3/1.1.3: Clock/Data Lane LP-TX 15%-85% Rise Time (T_{RLP}) (50pF C_{LOAD})								
Measured T_{RLP} for V_{DP}	< 25	**17.3**	**24.4**	N/A	N/A	N/A	ns	3, 4
Measured T_{RLP} for V_{DN}	< 25	**20.4**	**23.5**	N/A	N/A	N/A	ns	5, 6
Test 1.2.4/1.1.4: Clock/Data Lane LP-TX 15%-85% Fall Time (T_{FLP}) (50pF C_{LOAD})								
Measured T_{FLP} for V_{DP}	< 25	**18.2**	**24.0**	N/A	N/A	N/A	ns	7, 8
Measured T_{FLP} for V_{DN}	< 25	**17.1**	**20.8**	N/A	N/A	N/A	ns	9, 10
Test 1.2.5/1.1.5: Clock/Data Lane LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$) (50pF C_{LOAD})								
V_{DP} Falling Edges:								
MAX $\delta V/\delta t_{SR}$	< 150	**109.6**	**89.3**	N/A	N/A	N/A	mV/ns	7, 8
MIN $\delta V/\delta t_{SR}$	> 25	**35.1**	**26.0**	N/A	N/A	N/A	mV/ns	7, 8
V_{DN} Falling Edges:								
MAX $\delta V/\delta t_{SR}$	< 150	**97.8**	**106.1**	N/A	N/A	N/A	mV/ns	9, 10
MIN $\delta V/\delta t_{SR}$	> 25	**40.2**	**26.5**	N/A	N/A	N/A	mV/ns	9, 10
V_{DP} Rising Edges:								
MAX $\delta V/\delta t_{SR}$	< 150	**87.9**	**70.4**	N/A	N/A	N/A	mV/ns	3, 4
MIN $\delta V/\delta t_{SR}$	> 25	**49.1**	**36.0**	N/A	N/A	N/A	mV/ns	3, 4
MIN $\delta V/\delta t_{SR}$ margin	> 0	**16.1**	**5.2**	N/A	N/A	N/A	mV/ns	3, 4
V_{DN} Rising Edges:								
MAX $\delta V/\delta t_{SR}$	< 150	**78.8**	**76.7**	N/A	N/A	N/A	mV/ns	5, 6
MIN $\delta V/\delta t_{SR}$	> 25	**54.1**	**39.3**	N/A	N/A	N/A	mV/ns	5, 6
MIN $\delta V/\delta t_{SR}$ margin	> 0	**13.3**	**5.3**	N/A	N/A	N/A	mV/ns	5, 6
Test 1.1.6: Data Lane LP TX Pulse Width of Exclusive-OR Clock ($T_{LP\text{-}PULSE\text{-}TX}$) (50pF C_{LOAD})								
930mV Trip Level:								
Width of first XOR pulse	> 40	N/A	**61.6**	N/A	N/A	N/A	ns	12
Min of all other pulses	> 20	N/A	**47.1**	N/A	N/A	N/A	ns	12
500mV Trip Level:								
Width of first XOR pulse	> 40	N/A	**67.0**	N/A	N/A	N/A	ns	13
Min of all other pulses	> 20	N/A	**62.3**	N/A	N/A	N/A	ns	13
Test 1.1.7: Data Lane LP TX Period of Exclusive-OR Clock ($T_{LP\text{-}PER\text{-}TX}$) (50pF C_{LOAD})								
930mV Trip Level:								
Min XOR Clock period	> 90	N/A	**117.1**	N/A	N/A	N/A	ns	12
500mV Trip Level:								
Min XOR Clock period	> 90	N/A	**135.6**	N/A	N/A	N/A	ns	13

Table 3: (Section 1, Groups 3+4): Clock/Data Lane HS-TX Burst Signaling Requirements:

Test/Parameter	Conformance Range	Clk Lane Measured	Lane 0 Measured	Lane 1 Measured	Lane 2 Measured	Lane 3 Measured	Units	Fig.
Test 1.4.1/1.3.1: Clock/Data Lane HS Entry: T_{LPX} Value								
Measured T_{LPX}	> 50	**61.72**	**65.05**	N/A	N/A	N/A	ns	14, 15
Test 1.4.2/1.3.2: Clock/Data Lane HS Entry: $T_{PREPARE}$ Value								
Measured $T_{PREPARE}$	40+4*UI/ 85+6*UI (Data) 38/95 (Clock)	**60.41**	**63.35**	N/A	N/A	N/A	ns	14, 15
Test 1.4.3/1.3.3: Clock/Data Lane HS Entry: $T_{PREPARE}$ + T_{ZERO} Value								
Measured $T_{PREPARE+ ZERO}$	>145+10*UI (Data) > 300 (Clock)	**302.22**	**224.66**	N/A	N/A	N/A	ns	14, 15
Test 1.4.4/1.3.4: Clock/Data Lane HS-TX Differential Voltages ($V_{OD(1)}$, $V_{OD(0)}$)								
(Z_{ID}=100): $V_{OD(1)}$	140 / 270	**202.7**	**217.7**	N/A	N/A	N/A	mV	16, 17
(Z_{ID}=100): $V_{OD(0)}$	-140 / -270	**-202.3**	**-196.1**	N/A	N/A	N/A	mV	18, 19
(Z_{ID}=125): $V_{OD(1)}$	140 / 270	**177.2**	**208.8**	N/A	N/A	N/A	mV	20, 21
(Z_{ID}=125): $V_{OD(0)}$	-140 / -270	**-213.2**	**-221.5**	N/A	N/A	N/A	mV	22, 23
(Z_{ID}=80): $V_{OD(1)}$	140 / 270	**200.6**	**171.8**	N/A	N/A	N/A	mV	24, 25
(Z_{ID}=80): $V_{OD(0)}$	-140 / -270	**-218.7**	**-188.7**	N/A	N/A	N/A	mV	26, 27
Test 1.4.5/1.3.5: Clock/Data Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})								
(Z_{ID}=100): ΔV_{OD}	< 14	**11.6**	**10.6**	N/A	N/A	N/A	mV	-
(Z_{ID}=125): ΔV_{OD}	< 14	**9.2**	**13.1**	N/A	N/A	N/A	mV	-
(Z_{ID}=80): ΔV_{OD}	< 14	**13.0**	**12.9**	N/A	N/A	N/A	mV	-
Test 1.4.6/1.3.6: Clock/Data Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$, $V_{OHHS(DN)}$)								
(Z_{ID}=100): $V_{OHHS(DP)}$	< 360	**311.5**	**310.2**	N/A	N/A	N/A	mV	28, 29
(Z_{ID}=100): $V_{OHHS(DN)}$	< 360	**313.1**	**310.8**	N/A	N/A	N/A	mV	30, 31
(Z_{ID}=125): $V_{OHHS(DP)}$	< 360	**311.9**	**308.9**	N/A	N/A	N/A	mV	32, 33
(Z_{ID}=125): $V_{OHHS(DN)}$	< 360	**308.7**	**311.7**	N/A	N/A	N/A	mV	34, 35
(Z_{ID}=80): $V_{OHHS(DP)}$	< 360	**313.2**	**314.2**	N/A	N/A	N/A	mV	36, 37
(Z_{ID}=80): $V_{OHHS(DN)}$	< 360	**309.2**	**312.0**	N/A	N/A	N/A	mV	38, 39
Test 1.4.7/1.3.7: Clock/Data Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)								
(Z_{ID}=100): $V_{CMTX(1)}$	150 / 250	**187.0**	**185.7**	N/A	N/A	N/A	mV	40, 41
(Z_{ID}=100): $V_{CMTX(0)}$	150 / 250	**188.1**	**186.3**	N/A	N/A	N/A	mV	40, 41
(Z_{ID}=125): $V_{CMTX(1)}$	150 / 250	**187.1**	**185.8**	N/A	N/A	N/A	mV	42, 43
(Z_{ID}=125): $V_{CMTX(0)}$	150 / 250	**187.4**	**186.1**	N/A	N/A	N/A	mV	42, 43
(Z_{ID}=80): $V_{CMTX(1)}$	150 / 250	**187.6**	**187.7**	N/A	N/A	N/A	mV	44, 45
(Z_{ID}=80): $V_{CMTX(0)}$	150 / 250	**187.9**	**186.8**	N/A	N/A	N/A	mV	44, 45
Test 1.4.8/1.3.8: Clock/Data Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)								
(Z_{ID}=100): $\Delta V_{CMTX(1,0)}$	< 5	**-1.6**	**-0.4**	N/A	N/A	N/A	mV	-
(Z_{ID}=125): $\Delta V_{CMTX(1,0)}$	< 5	**-1.6**	**-0.2**	N/A	N/A	N/A	mV	-
(Z_{ID}=80): $\Delta V_{CMTX(1,0)}$	< 5	**-2.2**	**-0.7**	N/A	N/A	N/A	mV	-
Test 1.4.9/1.3.9: Clock/Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($V_{CMTX(LF)}$)								
(Z_{ID}=100): $V_{CMTX(LF)}$	< 25	**11.0**	**14.3**	N/A	N/A	N/A	mVpk	46, 47
Test 1.4.10/1.3.10: Clock/Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($V_{CMTX(HF)}$)								
(Z_{ID}=100): $V_{CMTX(HF)}$	< 15	**7.1**	**5.7**	N/A	N/A	N/A	mV_{RMS}	46, 47
Test 1.4.11/1.3.11: Clock/Data Lane HS-TX 20%-80% Rise Time (t_R)								
(Z_{ID}=100): t_R	0 / 0.40*UI	**121.5**	**137.2**	N/A	N/A	N/A	ps	48, 49
(Z_{ID}=125): t_R	0 / 0.40*UI	**131.6**	**128.4**	N/A	N/A	N/A	ps	50, 51
(Z_{ID}=80): t_R	0 / 0.40*UI	**122.9**	**93.4**	N/A	N/A	N/A	ps	52, 53
Test 1.4.12/1.3.12: Clock/Data Lane HS-TX 80%-20% Fall Time (t_F)								
(Z_{ID}=100): t_F	0 / 0.40*UI	**123.3**	**111.1**	N/A	N/A	N/A	ps	54, 55
(Z_{ID}=125): t_F	0 / 0.40*UI	**139.4**	**142.5**	N/A	N/A	N/A	ps	56, 57
(Z_{ID}=80): t_F	0 / 0.40*UI	**110.8**	**79.7**	N/A	N/A	N/A	ps	58, 59

Table 3: (continued)

Test 1.4.13/1.3.13: Clock/Data Lane HS Exit: T_{TRAIL} Value								
(Z_{ID}=100): T_{TRAIL}	> 60+4*UI (Data) > 60 (Clock)	**74.27**	**73.49**	N/A	N/A	N/A	ns	60, 61
Data: Trail state is inverted from the last HS data bit Clock: Trail state is always 0	N/A	**HS-0**	**Flipped**	N/A	N/A	N/A	-	60, 61
Test 1.4.14/1.3.14: Clock/Data Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})								
(Z_{ID}=100): T_{REOT}	< 35	**15.40**	**19.99**	N/A	N/A	N/A	ns	60, 61
Test 1.4.15/1.3.15: Clock/Data Lane HS Exit: T_{EOT} Value								
(Z_{ID}=100): T_{EOT}	< 105+12*UI	**88.35**	**94.46**	N/A	N/A	N/A	ns	60, 61
Test 1.4.16/1.3.16: Clock/Data Lane HS Exit: $T_{HS-EXIT}$ Value								
(Z_{ID}=100): $T_{HS-EXIT}$	> 100	**PASS**	**PASS**	N/A	N/A	N/A	ns	-
Test 1.4.17: Clock Lane HS Clock Instantaneous (UI_{INST})								
Maximum UI_{INST}	< 12500	**440.1**	N/A				ps	-
Mean UI_{INST}	Informative	**388.1**	N/A				ps	-
Test 1.4.18: Clock Lane HS Clock Delta UI (ΔUI)								
(Z_{ID}=100): Maximum ΔUI	N/A	**-235**	N/A				mUI	-

Table 4: (Section 1, Group 5): HS-TX Clock-to-Data Lane Timing Requirements

Test/Parameter	Conformance Range (Formula)	Conformance Range (Numeric)	Lane 0 Measured	Lane 1 Measured	Lane 2 Measured	Lane 3 Measured	Units	Fig.
Test 1.5.1: HS Entry: $T_{CLK-PRE}$ Value								
(Z_{ID}=100): $T_{CLK-PRE}$	> 8*UI	N/A	**23.21**	N/A	N/A	N/A	ns	15
Test 1.5.2: HS Exit: $T_{CLK-POST}$ Value								
(Z_{ID}=100): $T_{CLK-POST}$	> 60ns+52*UI	N/A	**206.40**	N/A	N/A	N/A	ns	61
Test 1.5.3: HS Clock Rising Edge Alignment to First Payload Bit								
First Data Lane payload bit of the HS burst aligns with a rising edge of the HS clock	N/A	Pass/Fail	**PASS**	N/A	N/A	N/A	-	62
Test 1.5.4: Data-to-Clock Skew ($T_{SKEW(TX)}$)								
Maximum observed Data-to-Clock Lane skew	0.30*UI / 0.70*UI	N/A	**71.1**	N/A	N/A	N/A	mUI	63
Mean Data-to-Clock Lane skew	0.35*UI / 0.65*UI	N/A	**20.7**	N/A	N/A	N/A	mUI	64
Minimum observed Data-to-Clock Lane skew	0.30*UI / 0.70*UI	N/A	**-42.2**	N/A	N/A	N/A	mUI	63
Test 1.5.5: Initial HS Skew Calibration Burst ($T_{SKEWCAL-SYNC}$, $T_{SKEWCAL}$)								
$T_{SKEWCAL-SYNC}$	15.75*UI / 16.25*UI	N/A	**16.04**	N/A	N/A	N/A	UI	-
$T_{SKEWCAL}$	0 / 32768*UI	N/A	**16384**	N/A	N/A	N/A	UI	-
Test 1.5.6: Periodic HS Skew Calibration Burst ($T_{SKEWCAL-SYNC}$, $T_{SKEWCAL}$)								
$T_{SKEWCAL-SYNC}$	15.75*UI / 16.25*UI	N/A	**16.03**	N/A	N/A	N/A	UI	-
$T_{SKEWCAL}$	0 / 4096*UI	N/A	**2048**	N/A	N/A	N/A	UI	-

Table 5: (Section 1, Group 6): LP-TX INIT, ULPS, and BTA Requirements

Test/Parameter	Conformance Range (Formula)	Conformance Range (Numeric)	Measured	Units	Fig.
Test 1.6.1: INIT: LP-TX Initialization Period ($T_{INIT,MASTER}$)					
(Clock Lane): $T_{INIT,MASTER}$	N/A	> 0.100	**PASS**	ms	-
(Data Lane 0): $T_{INIT,MASTER}$	N/A	> 0.100	N/A	ms	-
(Data Lane 1): $T_{INIT,MASTER}$	N/A	> 0.100	N/A	ms	-
(Data Lane 2): $T_{INIT,MASTER}$	N/A	> 0.100	N/A	ms	-
(Data Lane 3): $T_{INIT,MASTER}$	N/A	> 0.100	N/A	ms	-
Test 1.6.2: ULPS Entry: Verification of Clock Lane LP-TX ULPS support					
Verify DUT Clock Lane transmits proper LP-11/10/00 Clock Lane ULPS Entry sequence	N/A	Pass/Fail	**PASS**	-	-
Test 1.6.3: ULPS Exit: Transmitted T_{WAKEUP} Interval					
(Clock Lane): T_{WAKEUP}	N/A	> 1	**PASS**	ms	-
(Data Lane 0): T_{WAKEUP}	N/A	> 1	N/A	ms	-
(Data Lane 1): T_{WAKEUP}	N/A	> 1	N/A	ms	-
(Data Lane 2): T_{WAKEUP}	N/A	> 1	N/A	ms	-
(Data Lane 3): T_{WAKEUP}	N/A	> 1	N/A	ms	-
Test 1.6.4: BTA: TX-Side T_{TA-GO} Interval Value					
Measured T_{TA-GO}	>= $4*T_{LPX}$	N/A	N/A**	ns	-
Test 1.6.5: BTA: RX-Side $T_{TA-SURE}$ Interval Value					
Measured $T_{TA-SURE}$	$1*T_{LPX}$ / $2*T_{LPX}$	N/A	N/A**	ns	-
Test 1.6.6: BTA: RX-Side T_{TA-GET} Interval Value					
Measured T_{TA-GET}	> $5*T_{LPX}$	N/A	N/A**	ns	-

** Tests are Not Applicable for this DUT type, as it does not support bi-directional communication.