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SFF-8431 SFP+ Cable Assembly Conformance Test Suite
Version 1.0

Technical Document

Last Updated: April 8, 2014

10 Gigabit Ethernet Consortium

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MODIFICATION RECORD

August 21, 2013 Version 0.1

Christopher Bridges: Initial preliminary draft.

April 8, 2014 Version 0.1

Michael Klempa: Minor edits.

May 19, 2014 Version 1.0

Michael Klempa: Initial version

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Christopher Bridges	UNH InterOperability Laboratory
Michael Klempa	UNH InterOperability Laboratory
AJ McQuade	UNH InterOperability Laboratory
Jeff Lapak	UNH InterOperability Laboratory
Curtis Donahue	UNH InterOperability Laboratory

INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the standards conformance of SFP+ cable assemblies to the SFF-8431 Standard.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent test

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross-references to the SFF-8431 standards and other documentation that might be helpful in understanding and evaluating the test and results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the configuration of the test environment. Small changes in the configuration should not be included here, but rather included in the procedure section below.

Procedure

The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

The observable results section lists observations that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

Group 1: 10GSFP+ Cu CABLE ASSEMBLY SPECIFICATIONS

Overview:

The tests defined in this section verify the characteristics of the 10GSFP+ Cu cable assembly defined in Appendix E of SFF-8431.

Test 1.1 – Output AC Common Mode Voltage

Purpose: To verify that the AC Common Mode Voltage is within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C
[2] SFF-8431 Rev. 4.1 Appendix D.15 – AC Common Mode Voltage
[3] SFF-8431 Rev. 4.1 Table 12–Host Transmitter Output Jitter and Eye Mask Specifications at B
[4] IEEE Std. 802.3-2012, subclause 52.9.1.1 – Test-Pattern Definition

Resource Requirements: See Appendix I

Last Modification: May 20, 2014

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ Cu cable assemblies. This specification includes conformance requirements for the maximum Output AC Common-Mode Voltage defined in [2].

In this test, the differential amplitude is measured while the DUT is connected to the DSO. The common mode voltage can be found by averaging the signal+ and signal- at any time. RMS AC common-mode voltage may be calculated by applying the histogram function over 1 UI to the common mode signal.

Test Setup: See Appendix I.

Test Procedure:

1. Configure the BERT to send test pattern 3 (PRBS31) [4].
2. Connect the DUT's transmitter to the DSO.
3. Measure the common mode amplitude.
4. Apply a histogram function over 1 UI of the signal.

Observable Results:

a. The maximum output AC common-mode voltage should not exceed 13.5 mV RMS

Possible Problems: None.

Test 1.2 – Difference Waveform Distortion Penalty

Purpose: To verify that the DWDP is within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C
[2] SFF-8431 Rev. 4.1 Appendix E.4.1 – SFP+ Direct Attach Cable Test Setup
[3] SFF-8431 Rev. 4.1 Appendix E.4.2 – Cable dWDP Test Procedure
[4] SFF-8431 Rev. 4.1 Appendix D.14.2 – Linear Module Receiver Distortion Penalty Compliance Test

Resource Requirements: See Appendix III.

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ Cu cable assemblies. This specification includes conformance requirements for the maximum dWDP defined in [2], [3], and [4].

WDP is the simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device. WDP is a waveshape metric for waveform filtering and/or nonlinear distortion. Conceptually the WDP measurement is an example of what the DUT's transmitted signaling would 'look like' to a receiver device, after passing through an interconnect (i.e., channel, backplane, cable, etc), and being received and processed by an equalizer circuit inside the receiver device.

Because it is not typically possible to observe the signal at this point (as it is conceptually located inside the actual receiver IC, post-equalization) it is not possible to practically measure this signal, however it can be mathematically computed, based on a reference model of an interconnect, and a reference receive equalizer. This mathematical modeling is performed by a set of MATLAB code that is included as part of the Standard [3].

For this test the dWDP is defined as:

$$dWDP_c = WDP_o - WDP_i$$

Where WDP_i is the signal of a compliance waveform generator measured at the output of a host compliance board. WDP_o is the signal measured at the output of the Cu cable assembly (DUT).

It is important to carefully calibrate the input compliance signal. The target WDP_i can be achieved by adjusting DDJ and/or DDPWS through use of a pre-emphasis generator.

Test Setup: See Appendix III.

Test Procedure:

1. Configure the compliance signal generator to send a PRBS9 test pattern and such that it meets the target requirements found in [1].
2. Connect the host compliance board to the module compliance board and measure WDP_i
3. Connect the DUT between the module compliance boards and measure WDP_o
4. Calculate $dWDP_c$

Observable Results:

a. The calculated $dWDP_c$ value should not exceed 6.75 dBe

Possible Problems: None.

Test 1.3 – Voltage Modulation Amplitude Loss and VMA Loss to Crosstalk Ratio

Purpose: To verify that the VMA Loss and VMA Loss to Crosstalk Ratio are within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C
[2] SFF-8431 Rev. 4.1 Appendix D.7 – Voltage Modulation Amplitude (VMA)
[3] SFF-8431 Rev. 4.1 Appendix E.4.1 – SFP+ Direct Attach Cable Test Setup
[4] SFF-8431 Rev. 4.1 Appendix E.4.4 – VMA to Crosstalk Ratio

Resource Requirements: See Appendix I.

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ Cu cable assemblies. This specification includes conformance requirements for the VMA defined in [2], [3], and [4].

For the purpose of this test, VMA loss is defined by the equation:

$$L(dBe) = 20\log\left(\frac{VMA_i}{VMA_o}\right)$$

Where VMA_i is the measurement of VMA at B" and VMA_o is the VMA measured at C' as defined in [3].

VCR is defined by:

$$VCR(dBe) = VNA - L - K - 20\log_{10}(1 + C)$$

$$C = 0.3 * 10^{\left(-\frac{2L}{20}\right)}$$

$$VNR = 20\log_{10}\left[\frac{\frac{(NEXTaggressorVMA)}{2}}{NEXT}\right]$$

$$k(dBe) = 7.36$$

Test Setup: See Appendix I.

Procedure:

1. Set the compliance signal generator to transmit an eight ones eight zeroes pattern and such that it meets the requirements in [1].
2. Connect the host compliance board to the module compliance board and measure VMA_i.
3. Connect the DUT between the module compliance boards and measure VMA_o.
4. Calculate VMA loss.
5. Set the compliance signal generator to transmit PRBS31 and such that it meets the requirements in [1].
6. Connect the compliance signal generator as the NEXTaggressor and terminate the far end.
7. Measure the NEXT.
8. Calculate VCR.

Observable Results:

a. The VMA loss should not exceed 4.4 dBe.
b. The VCR should exceed 32.5 dB.

Possible Problems: None.

Test 1.4 – Differential Output/Input Reflection Coefficients

Purpose: To verify that the Differential Output/Input Reflection Coefficients are within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C'

Resource Requirements: See Appendix II.

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ Cu cable assemblies. This specification includes conformance requirements for the differential output/input reflection coefficients.

For the purpose of this test, the differential output return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 10 MHz to 11.1 GHz, the differential return loss of the driver should not exceed the limit given in the equation below:

$$\begin{Bmatrix} -12 + 2\sqrt{f} & 0.01 \le f < 4.1GHz \\ -6.3 + 13log_{10}\left(\frac{f}{5.5}\right) & 4.1GHz < f \le 11.1GHz \end{Bmatrix} (dB)$$

Test Setup: See Appendix II.

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's transmitter to the VNA.
3. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
4. Compute the differential return loss from the reflection coefficient values.

Observable Results:

a. The differential output return loss should exceed the limits described by [1].
b. The differential input return loss should exceed the limits described by [1].

Possible Problems: None.

Test 1.5 – Common Mode Output/Input Reflection Coefficients

Purpose: To verify that the Common Mode Output/Input Reflection Coefficients are within the conformance limits.

References:

[1] SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C'

Resource Requirements: See Appendix II.

Last Modification: September 23, 2013

Discussion:

Reference [1] specifies the transmitter characteristics for SFP+ Cu cable assemblies. This specification includes conformance requirements for the common mode output/input reflection coefficients.

For the purpose of this test, the common mode output return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 10 MHz to 11.1 GHz, the differential return loss of the driver should not exceed the limit given in the equation below:

$$\begin{Bmatrix} -7 + 1.6f & 0.01 \leq f < 4.1GHz \\ -3 & 4.1GHz < f \leq 11.1GHz \end{Bmatrix} \ (dB)$$

Test Setup: See Appendix II.

Procedure:

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Connect the DUT's transmitter to the VNA.
3. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
4. Compute the common mode return loss from the reflection coefficient values.

Observable Results:

a. The common mode output return loss should exceed the limits described by [1].
b. The common mode input return loss should exceed the limits described by [1].

Possible Problems: None.

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Appendix I - Setup for Electrical signaling measurements

Purpose: To specify the setup for electrical based tests in this test suite

References:

[1] SFF-8431 Rev. 4.1 Subclause 3.6.1 - Module Input Electrical Specifications at B' and B"
[2] SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C'

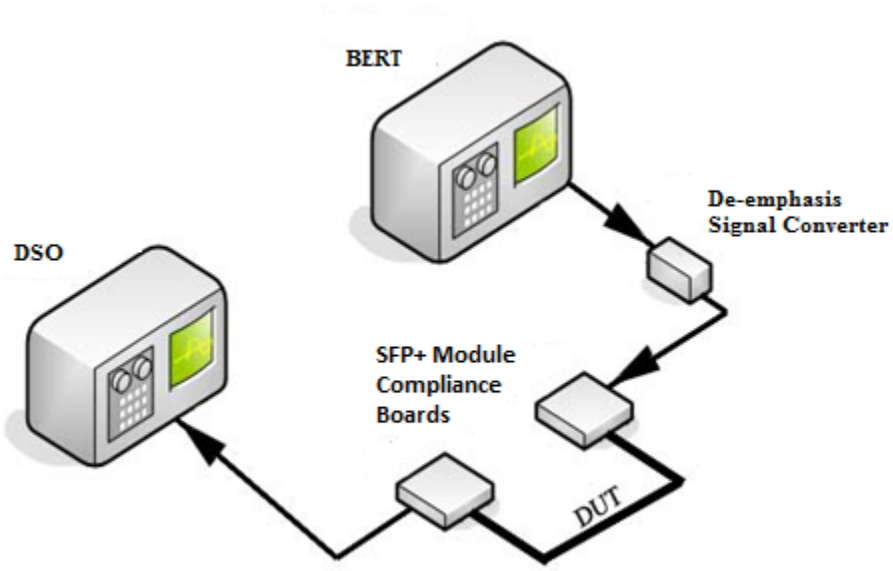
Resource Requirements:

- DSO
- BERT
- De-emphasis Signal Converter
- Two SFP+ Module Compliance Boards

Last Modification: August 21, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The BERT is setup to transmit a valid signal and jittered clock into the de-emphasis signal converter. The output of the de-emphasis signal converter is attached to the TX lane of the SFP+ Breakout card. The same RX lane on the other breakout card is attached to the DSO channels.

The BERT and De-emphasis signal converter should be configured so that the jitter values as read by the DSO are in reference [2].

Appendix II - Setup for VNA measurements

Purpose: To specify the setup for VNA based tests in this test suite

References:

[1] SFF-8431 Rev. 4.1 Subclause 3.6.1 Table 17 - Module Input Electrical Specifications at B' and B"

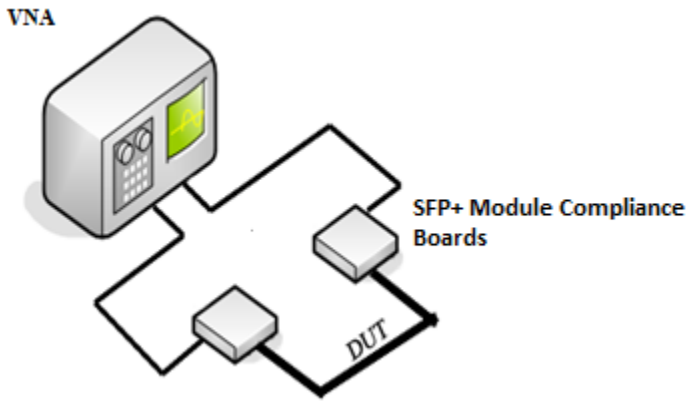
Resource Requirements:

- VNA
- Two SFP+ Module Compliance Boards

Last Modification: August 21, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The VNA is setup so that channels 1 and 2 are connected to the RX side of one card while channels 3 and 4 are attached to the TX side on the other card.

The VNA should be properly calibrated before use.

Appendix III – 10GSFP+ Cu Difference Waveform Penalty Test Setup

Purpose: To specify the setup for the difference waveform distortion penalty for 10GSFP+ Cu test.

References:

[1]SFF-8431 Rev. 4.1 Table 37 – 10GSFP+ Cu Cable Assembly Specifications at B' and C'
[2]SFF-8431 Rev. 4.1 Appendix E.4.1 – SFP+ Direct Attach Cable Test Setup
[3]SFF-8431 Rev. 4.1 Appendix E.4.2 – Cable dWDP Test Procedure

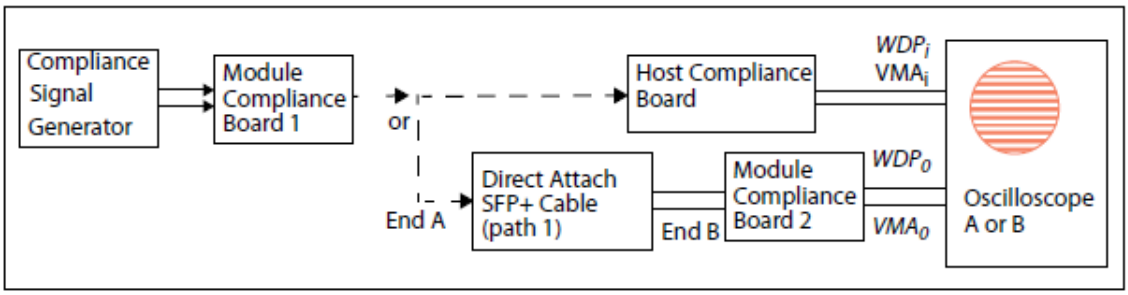
Resource Requirements:

- Compliance Signal Generator
- Two SFP+ Module Compliance Boards
- DSO
- Host Compliance Board

Last Modification: September 23, 2013

Discussion:

For the purpose of these tests, the testing equipment should be set up in the following manner:



The compliance signal generator should be set to the PRBS9 test pattern. Averaging should be used on the DSO to reduce noise. Signal rise and fall times should match those specified in [1].