

UNH-IOL IEEE 1588 Consortium Engineering Notes

The IEEE 1588 Consortium at the UNH-IOL is the premier place to have conformance and interoperability testing performed on your 1588 implementation. We will work with your engineers to find issues before they are found by your customers, and also provide a 3rd party report with technical details.

Interoperability testing

The following are examples of interoperability issues in ordinary clocks that we have discovered.

- With three clocks together on a network, product M1 is the grandmaster. Disconnecting M1 results in the other two products M2 and S establishing a new hierarchy with M2 as the new grandmaster. **S loses synchronization, falls silent and must be manually reset before synchronization can be re-established.**
- In the previous three-clock configuration, when M1 is reconnected it becomes grandmaster again, but under some conditions M2 does not relinquish its master status, so the network sees Announce and Sync messages from **two masters at the same time.**
- When product M is master and product S is slave, M sends Delay_Resp messages with logMessageInterval equal to -2 (“Respond to my Syncs every ¼ second.”) S treats the negative number as an unsigned byte, misinterpreting the -2 as 254, and so **waits 2²⁵⁴ seconds between Delay_Reqs.**
- When product M1 is master and has its portDS.logMinDelayReqInterval set to 3 (“Respond to my Syncs every 8 seconds.”), product M2 behaves accordingly, sending Delay_Reqs every 8 seconds. If product M2 then becomes master with its portDS.logMinDelayReqInterval set to -2 (“Respond to my Syncs every ¼ second.”), product M1 behaves accordingly. However, if M1 then becomes master again its portDS.logMinDelayReqInterval remains at -2, even if its logSyncInterval is higher, say 0. This results in M1 **sending Sync messages once per second and yet inviting slaves to respond to those Syncs every ¼ second,** which clutters the network with redundant Delay_Reqs.

